

# ABT Advanced BiCMOS Technology A High-Performance Line of 5-V and 3.3-V Products

# Data Book

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1992

A High-Performance Line of 5-V and 3.3-V Products



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### INTRODUCTION

As the operating frequencies of microprocessors increase, the period of time allotted for memory access, arithmetic computation, or similar operations decreases. With this in mind, a new series of advanced bus interface products, developed with Texas Instruments' submicron Advanced BiCMOS (ABT) process technology, assumes a prominent role as the key high-performance logic needed in today's workstation, personal and portable computer, and telecom systems. The goal of this family of products is to provide to system designers a bus interface solution combining high drive capability, lower power consumption, signal integrity, and propagation delays fast enough to appear transparent with respect to overall system performance. Fine-pitch package options simplify layout, reduce required board space, and decrease overall system costs. Novel circuit design techniques add value over competitive solutions.

Welcome to the new Texas Instruments ABT Advanced Bus Interface Data Book. Included herein is the broadest line of advanced bus products in the industry. Some of the products can be considered general purpose, while others are designed to offer specific compatibility to IEEE standard specifications. For the first time, 3.3-V products have been included along with traditional 5-V offerings. However, the one feature common to all the products is performance in the form of the EPICIIB™ submicron ABT process. It is part CMOS and part bipolar, but it is all performance.

The products described in this data book have been designed specifically to help system engineers meet the varied and stringent requirements of their end equipments. Products range from the extremely simple and popular octal buffer/transceiver to the extremely complex 36-bit universal bus transceiver (UBT™). For midscale integration, a whole series of 16-bit Widebus™ products exist. Because board costs also affect system costs, it is desirable for chips to be housed in a variety of packaging options to save space. Each of the products in the data book are offered in a number of different surface-mount and fine-pitch package options such as the shrink small-outline package (SSOP) and the thin shrink small-outline package (TSSOP). Finally, circuit design techniques built into the silicon such as mixed mode, power on demand, and bus hold offer enhanced parametrics and save having to discretely implement these enhancements.

Most of the products in the data book are available in production quantities. Please contact your local authorized distributor or Texas Instruments representative for details on any of these devices. Some of the devices in this data book are not yet available in production quantities; information on these devices is included in Product Previews. Texas Instruments is also evaluating many other devices for market introduction. Some of these are listed along with a description of their function in tables at the front of each section. Please contact our hotline at 214-997-5202 if you are interested in learning more about our plans for these devices.

Finally, in addition to specific information on the products, the data book contains other useful sections including mechanical data, application notes, and characterization information.

We hope you agree that Texas Instruments has the most complete line of high-performance bus-interface logic in the industry. We hope that these products will meet your system and design needs.

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### INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

### **OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)**

C<sub>i</sub> Input capacitance

The internal capacitance at an input of the device.

C<sub>o</sub> Output capacitance

The internal capacitance at an output of the device.

C<sub>pd</sub> Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):  $P_D = C_{od} V_{CC}^2 f + I_{CC} V_{CC}$ .

f<sub>max</sub> Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I<sub>CC</sub> Supply current

The current into\* the V<sub>CC</sub> supply terminal of an integrated circuit.

ΔI<sub>CC</sub> Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

I<sub>CEX</sub> Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition  $V_{\rm O} = 5.5$  V.

I<sub>IH</sub> High-level input current

The current into\* an input when a high-level voltage is applied to that input.

I<sub>IL</sub> Low-level input current

The current into\* an input when a low-level voltage is applied to that input.

Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and  $V_{CC} = 0 \text{ V}$ .

I<sub>OH</sub> High-level output current

The current into\* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I<sub>OL</sub> Low-level output current

The current into\* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I<sub>OZ</sub> Off-state (high-impedance-state) output current (of a 3-state output)

The current flowing into\* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

<sup>\*</sup>Current out of a terminal is given as a negative value.



### t<sub>a</sub> Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

### t<sub>dis</sub> Disable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs,  $t_{dis} = t_{PHZ}$  or  $t_{PLZ}$ . Open-collector outputs will change only if they are low at the time of disabling so  $t_{dis} = t_{PLH}$ .

### t<sub>en</sub> Enable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g.,  $\overline{OE}$ ). For 3-state outputs,  $t_{en} = t_{PZH}$  or  $t_{PZL}$ . Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them  $t_{en} = t_{PHL}$ .

### th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

### t<sub>pd</sub> Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ( $t_{pd} = t_{PHL}$  or  $t_{PLH}$ ).

### t<sub>PHL</sub> Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

### t<sub>PHZ</sub> Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state.

### t<sub>PLH</sub> Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

### t<sub>PLZ</sub> Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state.

### t<sub>PZH</sub> Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level.

### t<sub>PZL</sub> Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level.



### t<sub>su</sub> Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
  - 2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

### t<sub>w</sub> Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

### V<sub>IH</sub> High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is quaranteed.

### V<sub>IL</sub> Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

### V<sub>OH</sub> High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

### V<sub>OL</sub> Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

# $V_{T+}$ Positive-going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage,  $V_{T-}$ .

### V<sub>T</sub>... Negative-going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage,  $V_{T+}$ .



### **EXPLANATION OF FUNCTION TABLES**

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level ↓ = transition from high to low level

= value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)

Z = off (high-impedance) state of a 3-state output

a..h = the level of steady-state inputs A through H respectively

Q<sub>0</sub> = level of Q before the indicated steady-state input conditions were established

 $\overline{Q}_0$  = complement of  $Q_0$  or level of  $\overline{Q}$  before the indicated steady-state input

conditions were established

 $Q_n$  = level of Q before the most recent active transition indicated by  $\downarrow$  or  $\uparrow$ 

= one high-level pulse
= one low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active

transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with  $\uparrow$  and/or  $\downarrow$ , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q<sub>0</sub>, or  $\overline{Q}_0$ ), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  $\neg \neg \neg \neg \neg$ , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

**FUNCTION TABLE** 

				INPUTS							OUTI	PUTS	
CLEAR	MODE		СГОСК	SEI	RIAL		PARALLEL						)
CLEAN	S1	So	CLUCK	LEFT	RIGHT	Α	В	С	D	QA	QB	QC	Q <sub>D</sub>
L	X.	X	Х	X	X	Х	Х	Х	Х	L	L	L	L
н	Х	Х	L	x	Х	×	Х	X	Х	Q <sub>AO</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
H	Н	Н	Ť	×	X	а	b	С	d	a	b	С	d
н	L	Н	t	x	Н	н	Н	н	Н	lн	$\mathbf{Q}_{An}$	$\mathbf{Q}_{Bn}$	$Q_{Cn}$
н	L	Н	t	×	L	L	L	L	L	l L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
н	Н	L	1	н	X	x	X	X	X	Q <sub>Bn</sub>	$Q_{Cn}$	$Q_{Dn}$	Н
н	Н	L	t	L	X	x	X	X	Х	Q <sub>Bn</sub>	$\mathbf{Q}_{Cn}$	$\mathbf{Q}_{Dn}$	L
Н	L	L	Х	Х	Х	Х	Х	Х	Х	Q <sub>A0</sub>	Q <sub>B0</sub>	$Q_{C0}$	$Q_{D0}$

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output  $Q_A$ , data entered at B will be at  $Q_B$ , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at  $Q_A$  is now at  $Q_B$ , the previous levels of  $Q_B$  and  $Q_C$  are now at  $Q_C$  and  $Q_D$ , respectively, and the data previously at  $Q_D$  is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at  $Q_B$  is not at  $Q_A$ , the previous levels of  $Q_C$  and  $Q_D$  are now at  $Q_B$  and  $Q_C$ , respectively, and the data previously at  $Q_A$  is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

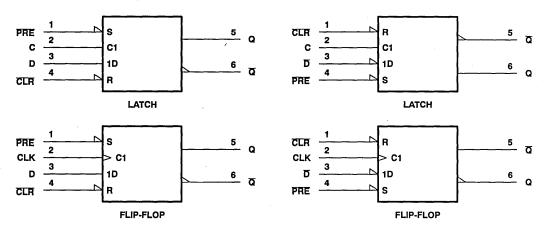


### D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called  $\overline{Q}$ . An input that causes a Q output to go high or a  $\overline{Q}$  output to go low is called preset (PRE). An input that causes a  $\overline{Q}$  output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits  $\overline{D}$  and  $\overline{Q}$ .

In some applications, it may be advantageous to redesignate the data input from D to D or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and  $\overline{Q}$  exchange names, the preset and clear pins also exchange names. The polarity indicators ( $\triangleright$ ) on PRE and CLR remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or  $\overline{D}$ ), Q, and  $\overline{Q}$ . Pin 5 (Q or  $\overline{Q}$ ) is still in phase with the data input (D or  $\overline{D}$ ); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_{.1} = R_{0.1A} \times P_T + T_A \tag{1}$$

where:

virtual junction temperature

thermal resistance, junction to free air total power dissipation of the device

 $P_T = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_i \times V_{CC}^2 \times f_o)$ 

free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

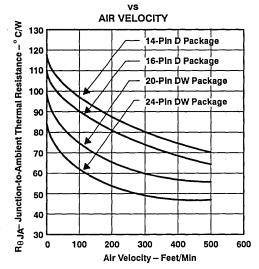


Figure 1

(2)

(3)

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

 $V_{CC}$ supply voltage (5 V for typical, 5.5 V for maximum) (see Note 1)

quiescent supply current (specified on device data sheet) lcc power dissipation capacitance (from the device data sheet) =

input frequency

output load capacitance

output frequency

fo N number of inputs driven by a TTL device

dc duty cycle

increase in supply current (specified on device data sheet) Δlcc

NOTE 1: In system applications, I<sub>CC</sub> can be minimized by keeping input voltage levels less than 1 V for V<sub>IL</sub> and greater than V<sub>CC</sub>-1 V for V<sub>IH</sub> and input rise and fall times less than 15 ns.

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type and list all available or planned options of that function. The technology columns identify the appropriate family and a particular data book where more information can be found. The applicable literature number, composed of either seven or eight alphanumeric characters, can be found at the lower right-hand corner on the back cover of each publication.

List of additional General Purpose Logic data books:

AC and ACT Devices	Advanced CMOS Logic Data Book	SCAD001C
Advanced Logic Devices	Advanced Logic and Bus Interface Logic Data Book	SCYD001
ALS and AS Devices	ALS/AS Logic Data Book	SDAD001B
BCT Devices	BiCMOS Bus Interface Logic Data Book	SCBD001A
F Devices	F Logic (54/74F) Data Book	SDFD001B
FIFO Devices	High-Performance FIFO Memories Data Book	SCAD003
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
SCOPE™ Devices	SCOPE™ Product Information	SSYV001
Std TTL, LS, and S Devices	TTL Logic Data Book	SDLD001A

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### **GATES**

### **Positive-NAND Gates**

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
DESCRIPTION	OUIPUI		ALS	AS	F	НС	нст	AC	ACT	вст	ABT
8-Input		'30	~	~	~	~	1				
8-input		'11030			,		1	~	~	ļ —	
13-input	L	'133	~			V					
Dual 2-Input		'8003	V				1		Ţ	1	1
Dual 4-Input		'11013						V	Ţ		
		'20	V	~	V	~					
		'40	V		~						
		'11020						~	~		
Triple 3-Input		'10	~	V	~	~					
		'1010	~								
		'11010						V	~		
		'00	~	~	V	V	~				
		'11000						~	~		
		'37	~								
Quad 2-Input	ос	'38	~		V						
		'132				V					
		'11132						~	V		
•		'1000		~							
Llau O launt		'804	~	~							
Hex 2-Input		'1804		~					1		
Over d.O. leaved	00	'01	~			~					
Quad 2-Input	ос	'03	V			V		}			

### **Positive-AND Gates**

DESCRIPTION	ОИТРИТ	7/05	TECHNOLOGY								
		TYPE	ALS	AS	F	НС	нст	AC	ACT	BCT	ABT
Triple 3-Input	ос	'15	~								
0	ос	'09	~			~					
Quad 2-input		'7001				~					
Dual 4-Input		'21	~	~	V	~					
		'11021						~	~		
Talala O lanas		'11	~	V	V	V					
Triple 3-Input		'11011					1	V	V		
		'08	~	~	~	~	V				
Quad 2-Input		'1008		~							
•		'11008						~	1		
		'808		V		V					
Hex 2-Input		'1808		V	<u> </u>						

 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated



# **GATES** (continued)

### Positive-OR/NOR Gates

DECODINE	CUITDUIT	700				Т	ECHNOLO	ΒY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	нс	нст	AC	ACT	ВСТ	ABT
Triple 3-Input		'4075				V					
		'32	~	~	V	V	V				]
Ound Olemen		'1032		~							
Quad 2-Input		'11032		-				V	V :		
		'7032				V					
Llau O la aut		'832	~	~		V					
Hex 2-Input		'1832		~							
Dual 5-Input		'260			V						
		'27	~		V	V					
Triple 3-Input		'11027						V	V		
		'02	~	~	V	V	~				
	ос	'33	~								
Quad 2-Input		'36			~	~					
		7002				~					
		'11002						V	V		
Nov. O. Immust		'805	~	~							
ex 2-Input		'1805		V				l			

### **OR/NOR Gates**

DESCRIPTION	OUTPUT	TYPE				TE	CHNOLO	GY			-
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	нс	нст	AC	ACT	вст	ABT
8-Input		'4078				~			Ţ		
Quad 2-Input		'86	~	~	~	~					
Exclusive-OR Gates		'11086						1	~		
With Totem-Pole Outputs		'386				~					
Quad 2-Input Exclusive-OR Gates	ос	'136	~								
	OD	'266				V			1		
		'810	V			T	T				
Quad 2-Input Exclusive-NOR Gates		'11810						~	V		
LXCIUSIVO-INOTI GALOS		'7266				V			1		
	ОС	'811	V								

### **AND-OR Gates**

DESCRIPTION	OUTPUT	TYPE				TE	CHNOLO	GY			
DESCRIPTION	COIPOI	ITPE	ALS	AS	F	HC	HCT	AC	ACT	вст	ABT
Quad 4-2-3-2-Wide Input		'64			~						
Dual 2-Wide 2-Input, 3-Input		'51			~	V					

 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated



### **INVERTING/NONINVERTING BUFFERS**

### Hex Inverters/Noninverters

DECORPORION	OUTDUT	700					TECHN	OLOGY				
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	НСТ	HCU	AC	ACT	вст	ABT
		'04	~	~	V	V	V	V		T		
		'11004							V	V		
	ос	'05	~			V						
Hex Inverters		'14				V						
		'11014							~	V		
		'1004	~	~								
		'1005	~									
		'34	~									
		'11034							~	~		
dex Noninverters	ос	'35	~									
		'1034	~	~								
	ОС	1035	V			1	1			1		

### NOTES:

 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated

### **BUFFERS/DRIVERS AND BUS TRANSCEIVERS**

## **Buffers/Drivers**

DESCRIPTION	ОИТРИТ	TYPE					TECHN	OLOGY				
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	HC	нст	AC	ACT	вст	ABT	LVT
Quad Buffers/Drivers	38	'125			V	~	1			V	+	~
Quad Bullers/Drivers	35	'126			~	V	~			V	+	
Naminusting How Buffers / Drivers	38	'365				~						
Noninverting Hex Buffers/Drivers	35	'367				V						
Inverting Hex Buffers/Drivers	38	'368				~			]			
		'241	V	~	~	~	V			V	+	
	İ	'11241	]					1	~			
	ı	'25241								+	+	
		'244	~	~	V	1	V		1	V	+	V
	38	'11244						~	~			
Namida ada Catal Barran Barran	1	'1244	~									
Noninverting Octal Buffers/Drivers		'25244								V	+	
		'465	~									
		'541	V		V	V	~			V	V	
•		'757		V						V		
	oc	'760	~	V						V		
		'25760								+		
		'240	~	1	V	V	1	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		V	V	+
	į	'11240	-					V	V			
		'1240	V									
	38	'25240								V		
Inverting Octal Buffers/Drivers	Ĭ	'466	1									
	it .	'540	~			1	V			~	+	
		'756	~	~						1		
	ос	'763	V	1			<u> </u>					
Inverting and Noninverting	38	'230		1								
Octal Buffers/Drivers	ОС	'762		~								
Triple 4-Input AND/NAND Drivers		'11800						+	+			
Triple 4-Input OR/NOR Drivers		'11802			j				1			
		'827					ļ				+	
Noninverting 10-Bit Buffers/Drivers	38	'11827				_		~	V			
	ļ	'29827	V				<del>                                     </del>			V		
. <del></del>	1	'828	<u> </u>				<del>                                     </del>				+	
Inverting 10-Bit Buffers/Drivers	38	'11828			<b> </b>	<del>                                     </del>	<u> </u>	~	V	<del>                                     </del>	†	
• • • • • • • • • • • • • • • • • • • •		'29828	V				<del>                                     </del>	<u> </u>	<u> </u>	~		<del>                                     </del>
	<del> </del>	'16241	<del>                                     </del>				<del>                                     </del>		V	<del>                                     </del>	V	<del>                                     </del>
Noninverting 16-Bit Buffers/Drivers	38	16244	<u> </u>				<del>                                     </del>	1	1		V	+
The second secon		16541					-		1		V	<del>                                     </del>

### NOTES:

 <sup>✔</sup> Product available in technology indicated
 + New product planned in technology indicated



## **Buffers/Drivers (continued)**

DESCRIPTION	ОИТРИТ	TVDE					TECHN	OLOGY				
DESCRIPTION	COIPOI	TYPE	ALS	AS	F	НС	нст	AC	ACT	вст	ABT	LVT
Inverting 16-Bit Buffers/Drivers	38	'16240						~	~		V	
Inverting 16-bit bullers/Drivers	33	'16540					I		V		V	
Noninverting 18-Bit Buffers/Drivers	38	'16825					T -		~		+	
Inverting 18-Bit Buffers/Drivers	38	'16826						+	+		+	
Noninverting 20-Bit Buffers/Drivers	38	'16827							1		+	
Inverting 20-Bit Buffers/Drivers	38	'16828							+		+	
Octal Buffers/Drivers		'746	~									
With Input Pullup Resistors		'747	~									

### Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DECORIDEION	OUTDUT	7/05					TECHN	OLOGY	,			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	нс	HCT	AC	ACT	вст	ABT	LVT
		'16500										+
		'16500A									~	
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	38	'16501									V	+
ominoreal due transcorrere (ed.)		'16600									+	1
		'16601									+	
Noninverting 36-Bit	38	'32500									+	
Universal Bus Transceivers (UBT ™)	33	'32501	}								+	
Noninverting 16-Bit Tri-Port Universal Bus Exchangers (UBE ™)	38	'32316									+	
Noninverting 18-Bit Tri-Port Universal Bus Exchangers (UBE™)	38	'32318								]	+	
		'162500									+	
18-Bit Universal Bus Transceivers	38	'162501					]				+	
(UBT™) With Series Resistors on B Port	35	'162600									+	
•		'162601									+	
SCOPE™ 18-Bit Universal Bus Transceivers (UBT ™)	38	'18502								1	+	
SCOPE™ 20-Bit Universal Bus Transceivers (UBT ™)	38	'18504						4			+	

NOTES:

✔ Product available in technology indicated

+ New product planned in technology indicated

UBT, UBE, and SCOPE are trademarks of Texas Instruments Incorporated.



### **Bus Transceivers**

Noninverting Quad Transceivers   3S   243   V   V   V   V   V   V   V   V   V	PEGGDIPTION	0.170117						TECHN	OLOGY		***		
Inverting Quad Transceivers    OC   758	DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	нс	HCT	AC	ACT	вст	ABT	LVT
Inverting Qual Transceivers    1245	Noninverting Quad Transceivers	38	'243	V	~	V							
SS   242	Investiga Count Transactions	ос	'758	1									
1245	inverting Quad Transceivers	38	'242		~	V							
Noninverting Octal Transceivers   Section			'245	~	~	~	V	V			V	V	V
Noninverting Octal Transceivers    1645			'1245	1									
25841			'11245						V	V			
Noninverting Octal Transceivers    645		38	'25245								V	+	
1645		}	'25641								+		
1645   V	Naminus ation Ostal Transcrius		'645	~	~		1	V					
CC	Noninverting Octal Transceivers		'1645	~									
OC   11623			'621	V		V							
11623		00	'623	~	~	V	1	V			V	V	
OC/3S   639		00	'11623						V	1			
11620			'641	~	~								
11620		OC/3S	'639	V	~								
1/25620			'620	V			ļ				V	V	
1		1	'11620						1	V			
1640		1	'25620	T		-					+		
11640		38	'640	V	V		1	V			V	V	
25640			'1640	V									
OC   '642   V   V   V   V   V   V   V   V   V	Inverting Octal Transceivers		'11640	1					1	~			
OC   '642   V   V		1	25640								+		
'25642			'622	V									
OC/3S   '638   V   V		ос	'642	V	1								
True and Inverting		Ì	'25642								V	<b></b>	
Octal Transceivers		OC/3S	'638	V	V								
Noninverting 9-Bit Transceivers   3S   1863   1863   1863   1863   1863   1863   1863   1863   1863   1863   1863   1863   1864   186	True and Inverting	38	'11643						V	V			
19863   19864   1986	Octal Transceivers	ОС	'644		1		1			ļ —			
1/29863   1/29864   1/29864   1/29861   1/29861   1/29861   1/29861   1/29862   1/29			'863									+	
Noninverting 10-Bit Transceivers   3S   1861	Noninverting 9-Bit Transceivers	38	'29863	1							1		
Noninverting 10-Bit Transceivers   3S   1861	Inverting 9-Bit Transceivers	38	'29864				<b></b>	-				<u> </u>	$\vdash$
11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   11862   118623   11			'861	<u> </u>								+	$\vdash$
10-Bit Transceivers   3S   129862   16245   16623   16640	Noninverting 10-Bit Transceivers	38	'29861	~				<b> </b>			1		<u> </u>
10-Bit Transceivers   3S   129862   16245   16623   16640			'11862				<u> </u>	<del>                                     </del>	1				
Noninverting 16-Bit Transceivers   3S   16245	Inverting 10-Bit Transceivers	38	'29862			<u> </u>		<b></b> -	<del></del>	-	V	<del></del>	<u> </u>
Noninverting 16-Bit Transceivers 3S 16623		1	'16245					<del>                                     </del>	~	V	<u> </u>	1	+
Inverting 16-Bit Transceivers 3S 116640	Noninverting 16-Bit Transceivers	38		<u> </u>				<del>                                     </del>			<b></b>		
nverting 16-Bit Transceivers 3S		<u> </u>		<u> </u>									
	Inverting 16-Bit Transceivers	38	16620	<u> </u>				<b></b>		<del></del>	<b>†</b>		

- ✓ Product available in technology indicated
   + New product planned in technology indicated



### **Bus Transceivers (continued)**

DESCRIPTION	ОИТРИТ	TYPE					TECHN	OLOGY				
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	НС	HCT	AC	ACT	вст	ABT	LVT
Noninverting 18-Bit Transceivers	38	'16863							V		+	
Inverting 18-Bit Transceivers	38	'16864							+		÷	
Noninverting 20-Bit Transceivers	38	'16861							V		+	
Inverting 20-Bit Transceivers	38	'16862									+	
	T	'11470							V			
	1	'543			V					V	+	+
	l	'11543							V			
		'646	1	~		V	V			V	V	V
	1	'646A									V	
	38	'11646						~	V			
	35	'25646								+		
Noninverting Octal Registered Transceivers	1	'652	V	~		V	~			V	V	+
riogisterou rransceivers		'11652						~	V			
	1	'25652				1				+		
		'2952								V	+	+
	}	'2952A									V	
	ОС	'647	V			1				ļ		
	00/00	'653	V									
	OC/3S	'654	V									
		'544								V	+	
	1	'11544							V		-	
	1	'648	V	V						V	+	
Inverting Octal Registered Transceivers	38	'11648						V	V			
negistered Transcervers		'651	V	V						V	+	
		'11651						V	V			
	1	'2953								V	+	
		'16470							V		V	
	]	'16543						~	V		V	+
Noninverting 16-Bit	38	'16646						~	V		+	+
Registered Transceivers		'16652						V	V		+	+
		'16952							V	1	V	+
		'16471							<b> </b>		+	
		'16544	<u> </u>		<u> </u>	†			1		+	
Inverting 16-Bit	38	'16648							V		+	
Registered Transceivers	1	'16651				$\vdash$			+		+	
	}	'16953					1				+	



 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated

## **Bus Transceivers (continued)**

DESCRIPTION	ОПТРИТ	TYPE					TECHN	OLOGY				
DESCRIPTION	JUIPUI	ITPE	ALS	AS	F	нс	нст	AC	ACT	вст	ABT	LVT
		'16472						V				
		'16474							V			
Noninverting 18-Bit	38	'16500									~	+
Registered Transceivers	33	'16501					<u> </u>				V	+
		'16600									+	
		'16601									+	
Inverting 18-Bit	38	'16473						+	+			
Registered Transceivers	33	'16475							V			
Noninverting 36-Bit Transceivers	38	'32245									+	
		'32500					<u> </u>				+	
Noninverting 36-Bit Registered Transceivers	38	'32501									+	
		'32543									+	
		'657			V					V	+	
		'659					~					
		'833									+	
	38	'834									+	
0 (0 D) D T	İ	'853									+	
8-/9-Bit Bus Transcelvers With Parity Checkers/Generators	1	'854									+	
Than I amy Chockers, action and		'899								V		
		'29833	~							V		
	3S/OC	'29834					L			V		
	33/00	'29853	~							~		
		'29854	V							V		
		'16833						l	1		~	
Dual 8-/9-Bit Bus Transceivers With Parity Checkers/Generators	38	'16657							1		~	
		'16853									V	
Universal	38	'856		~								
Transceivers/Port Controllers	35	'877		~								
Noninverting 16-Bit Tri-Port Registered Bus Exchangers	38	'32316									+	
Noninverting 18-Bit Tri-Port Registered Bus Exchangers	38	'32318									+	



 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated

## **MOS Memory Drivers/Transceivers**

DECORPTION	QUEDUE	TYPE				TE	CHNOLO	GY			
DESCRIPTION	OUTPUT	IYPE	ALS	AS	F	нс	HCT	AC	ACT	ВСТ	ABT
		'2623		~							
Octal Transceivers With Series Resistors on Output	38	'2640		V							
Colles resistors on Cutput		'2645		~							
		'2240	~							~	V
		'2241								V	+
Octal Buffers/Drivers With Series Resistors on Output	38	'2244								V	V
Cerics resistors on Cutput	}	'2540	1			1					
		'2541	~								
Octal Transceivers With Series Resistors on B Port	38	'2245								~	+
Octal Latches With Series Resistors on Output	38	'2574								~	
10-Bit Buffers/Drivers With	00	'2827								~	
Series Resistors	38	'2828								1	
		'2410								V	
11-Bit Buffers/Drivers With	38	'2411								+	
Series Resistors	35	'5400				1					V
		'5401					1			[	V
12-Bit Buffers/Drivers With	38	'5402									V
Series Resistors	35	'5403									V
16-Bit Buffers/Drivers With	00	'162240		-							+
Series Resistors	38	'162244	1								+
		'162500									+
18-Bit Universal Bus Transceivers	00	'162501									+
(UBT ™) With Series Resistors on B Port	38	'162600									+
		'162601									+
12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port	38	'162260									+

### NOTES:

✓ Product available in technology indicated
 + New product planned in technology indicated

### **TESTABILITY BUS-INTERFACE CIRCUITS**

# SCOPE™ Testability Circuits

DECODIDATION	NO. OF	OUTPUT	7/05				TE	CHNOLO	GY		÷.,	
Transparent Latches Flip-Flops	BITS	COIPOI	TYPE	ALS	AS	F	НС	нст	AC	ACT	вст	ABT
D. #/D:		-00	'8240A								V	
Butters/Drivers	8	38	'8244A								+	
,	8	38	'8245									~
Transceivers		33	'8245A							]	~	
	18	38	'18245									+
Transparent Latches	8	38	'8373A								~	
Flip-Flops	8	38	'8374A								~	
			'8543									~
		38	'8646							1		V
	8	35	'8652									~
Builder Immunistration			'8952									~
Registered Transceivers			'18502				_			· · · · · ·		+
	18	38	'18646									+
	•	}	'18652									+
	20	38	'18504									+
Test Bus Controllers		38	'8990	i						V		
Digital Bus Monitors		38	'8994							~		
Scan Path Linkers	4	38	'8997							1		
With Identification Buses	8	38	'8999							~		

- ✓ Product available in technology indicated
   + New product planned in technology indicated

### **FLIP-FLOPS AND LATCHES**

## Flip-Flops

DESCRIPTION	ОПТРИТ	TYPE	TECHNOLOGY											
DESORIF HOR	301501	1176	ALS	AS	F	нс	HCT	AC	ACT	вст	ABT	LVT		
		73				~								
		'76				1	ļ		<u> </u>					
		'107				1	<u> </u>							
		'109	1	~	1	V				ļ	<u></u>			
Dual J-K Edge-Triggered		'11109						~	V					
		'112	V		V	1	<u> </u>			<u> </u>		<u> </u>		
•		'11112						~	<b>'</b>		<u> </u>			
		'113	1		~	1								
		'114	~		~									
Dual D-Type		74	~	~	V	V	~		i					
Dual D-Type		'11074						1	V					
		7074				V								
Dual D-Type With 2-Input NAND/NOR Gates		7075				~								
17415/1611 Gales		'7076	,			1								
		'874	~	~										
		'11874						V	1					
Dual 4-Bit D-Type Edge-Triggered	38	'876	V	V										
		'878	~	V										
	1	'879	V	V										
		'173				V								
Quad D-Type		'175	~	V	V	V								
•		'11175						V	~					
Quad D-Type With Clock Enable	<u> </u>	'11379					1	V	V	-				
		'174	1	V	V	V								
Hex D-Type		'11174						V	V					
1		'378			V	~								
Hex D-Type With Clock Enable	T	'11378						V	V					
		'374	V	V	V	V	V			V	V			
Octal D-Type True Data	38	'11374						V	V					
••	-	'574	~	~	~	V	1			V	V	V		
	T	'273	~			~	V		-		+	1		
		'11273			<del> </del>	<b> </b>	<del> </del>	V	V					
Octal D-Type True Data		'575	V	V			T				<u> </u>			
With Clear	38	'874	V	V										
		'878	V	~			<del>                                     </del>		l	<del> </del>	<del>                                     </del>			
Octal D-Type True Data	<del> </del>	'377		Ť	V	1	1				V			
With Clock Enable	<b></b>	11377			ĻŤ	Ť	+	V	V	<b></b>	<del></del>			
	1		1		I	1	L		1	L	L	L		

NOTES:



 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated

## **FLIP-FLOPS AND LATCHES (continued)**

# Flip-Flops (continued)

DESCRIPTION	ОПТРИТ	TYPE	TECHNOLOGY										
DESCRIPTION	GOIPOI	TTPE	ALS	AS	F	НС	HCT	AC	ACT	вст	ABT	LVT	
		'534	~	1	~	1				1	+		
		'11534						~	V				
Octob D Trans Investiga	38	'564	1			V							
Octal D-Type Inverting	35	'576	V	V									
		'826		V									
		'29826								V			
Octal Dual-Ranked True Data	38	'4374		~			T .						
Octai Duai-Hanked True Data	35	'11478						~	~				
Catal law at a Mills Olars	-00	'577	V	V									
Octal Inverting With Clear	38	'879	~	V									
Octal Inverting With Preset	38	'876	V	~									
		'825		~			,						
Octal True Data	38	'11825							~				
	1	'29825								+ - - - - - - - - - - - -			
8-Bit Diagnostic Pipeline Register	38	'29818	V										
	38	'823		~							+		
-Bit True Data		'11823						+	+				
		'29823	~							~	+		
		'824		V									
9-Bit Inverting	38	'29824	~										
		'821		~							+		
10.00.		'1821		V									
10-Bit True Data	38	'11821						+	~				
	'	'29821	V							~			
40.00		'822		V									
10-Bit Inverting	38	'29822								~	+ + + + + + + + + + + + + + + + + + + +		
16-Bit D-Type True Dáta With Clock Enable		'16377									+		
16-Bit Noninverting	38	'16374						~	V		~	+	
16-Bit Inverting	38	'16534									+		
18-Bit Noninverting	38	'16823						+	V		+		
18-Bit Inverting	38	'16824						+	+				
20-Bit Noninverting	38	'16821	-						V		+		
20-Bit Inverting	38	'16822			ļ ——			+	+				

### NOTES:

✔ Product available in technology indicated
 + New product planned in technology indicated

## FLIP-FLOPS AND LATCHES (continued)

### Latches

Bits   Bits	DESCRIPTION	NO. OF	OUTPUT	TYPE	TECHNOLOGY										
Bistable   4   1975	DESCRIPTION	BITS	OUIPUI	ITPE	ALS	AS	F	нс	нст	AC	ACT	вст	ABT	LVT	
D-Type Edge-Triggered   8   996   V	Ristable	۱ ,		75				~							
Inverting and Noninverting	Distable	7		'375				<b>'</b>							
D-Type Transparent Readback Latch, True   9   3S   3992   V		8		'996	~									ļ	
Second Second		8	38	'990	~										
10   3S   994   V	D-Type Transparent Readback Latch, True	9	38	'992	~										
Peadback Latch, Inverting		10	38	'994	~										
D-Type Transparent With Clear, True Outputs  8	D-Type Transparent	8	38	'991	~										
Clear, Inverting Outputs	Readback Latch, Inverting	9	38	'993	~										
Clear, Inverting Outputs	D-Type Transparent With Clear, True Outputs	8	38	'666	~										
D-Type Transparent True    8		8	38	'667	~										
D-Type Transparent True	D-Type Transparent True			'373	~	V	~	V	V			~	V		
16   3S   16373		8	38	'11373						~	V				
D-Type Dual 4-Bit Transparent True				'573	~	V	~	V	V			V	V	V	
D-Type Dual 4-Bit Transparent True  8 3S   1873	į	16	38	'16373						~	V		V	+	
Transparent True    8   38   11873		32	38	'32373									+		
Transparent True  8 35 11873	D-Type Dual 4-Bit			'873	V	V									
D-Type True Inputs  8 38 38 38 38 38 40 4 4 4 5 5 5 6 6 7 5 6 7 5 6 7 6 7 6 7 6 7 6 7		. 8	33	'11873						V	V	·			
D-Type   S   S   S   S   S   S   S   S   S		8		'533	V	V	i					V	+		
16   3S   16533	. '		38	'11533						~	V				
16   3S   16533				'563	V			~							
Dual 4-Bit Transparent Inverting   8   3S   '880   V   V   V	Transparent inverting			'580	~	V									
Transparent Inverting 8 3S 880		16	38	'16533	1					-			+		
Addressable 8 28 '259		8	38	'880	~	~									
Addressable 8 Q '4724 V	2-Input Multiplexed	8	38	'604				V	1						
D-Type True Inputs  8 3S 11845	<b>A.1.1</b>		28	'259	~			V							
D-Type True Inputs  8 3S '11845	Addressable	8 -	Q	'4724				V							
D-Type True Inputs  9 3S 1843				'845	1										
D-Type True Inputs  9 3S		8	38	'11845							+	+			
D-Type True Inputs  9 3S '1843				'29845	~							İ	<u> </u>		
10   3S   '841   \( \subset \text{ \sqrt{29843}} \)				'843	~	~							+		
10   3S   '841   \( \subset \text{ \sqrt{29843}} \)		9	38	'1843		~									
10 3S '29841 V	D-Type True Inputs			'29843		<u> </u>	<u> </u>	<del></del>	T			1			
10 3S '29841 V				'841	V	V						<u> </u>	+		
18 3S '16843 +		10	. 38	'29841	<del></del>		<del> </del>	l				V			
		18	38	'16843	T								+		
		20	38	'16841							V				

 <sup>✓</sup> Product available in technology indicated
 + New product planned in technology indicated



## FLIP-FLOPS AND LATCHES (continued)

### Latches (continued)

DECORIDEION	NO. OF	оитрит	TYPE	TECHNOLOGY									
DESCRIPTION	BITS			ALS	AS	F	HC	нст	AC	ACT	вст	ABT	LVT
	Τ.	38	'846	V									
	8		'29846								~		
	9	38	'844	~									
D Time Investigation Inc. to	9		'29844								~		
D-Type Inverting Inputs	40	38	'842	V	V					I			
<u> </u>	10		'29842	V									
	18	38	'16844						+	+			
	20	38	'16842						+	+			

### **REGISTERS**

## **Shift Registers**

PERCEIPTION	NO. OF	OUTDUT	7/05				TECHN	IOLOGY			
DESCRIPTION	BITS	OUTPUT	TYPE	ALS	AS	F	нс	нст	AC	ACT	ВСТ
			'194		~						
Parallel-In	4		'11194		,				~	~	
Parallel-Out Bidirectional			'299	~		~					
	8		'323	V		~	T				+
Parallel-In Parallel-Out	4		'195		V						
Serial-In Parallel-Out	8		'164	~			~				
Develop to Contact Cont	T		'165	~			~				
Parallel-In Serial-Out	8		'166	~		+	1				
Serial-In Parallel-Out		00	'594				~				
With Output Latches	8	38	'595				~				
Parallel-Out	10		'11898						~	V	
Al-alamatan	8	38	'299	~							
Noninverting	9	38	'29823	~							

### **Register Files**

DESCRIPTION	ОИТРИТ	TOUDE				TE	CHNOLO	GY			
		TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Dual 16 Word × 4 Bits	its 3S	'870	~								
		'871		/						1	

- ✓ Product available in technology indicated
   + New product planned in technology indicated



# **COUNTERS**

# Synchronous Counters - Positive-Edge-Triggered

DECODIDATION	PARALLEL	7/05				TECHN	OLOGY			
DESCRIPTION	LOAD	TYPE	ALS	AS	F	HC	нст	AC	ACT	ВСТ
		'160	~							
4-Bit Decade	Sync	'11160						V	~	
		'11162						V	~	
	Cuma	'168			V					
4-Bit Decade Up/Down	Sync	'568	~							
	Async	'190			V					
		'161	~	V	V	~				
4-Bit Binary	Sync	'163	~	~	~	V				
		'561	V							
		'169	~	V	V					
	Sync	'569	~	-						
4 Dit Diagon Ha /Dans		'8169	~							
4-Bit Binary Up/Down		'191	~			~				
	Async	'11191						V	~	
		'193	~			V				
	Sync Clear	'869	~	~						
8-Bit Up/Down	Anuna Class	'867	V	~						
	Async Clear	'11867							~	
Divide-by-10 Counter	Sync	'4017				V				

# Asynchronous Counters (Ripple Clock) - Negative-Edge-Triggered

	PARALLEL	7/25				TECHN	IOLOGY			
DESCRIPTION	LOAD	TYPE	ALS	AS	F	нс	HCT	AC	ACT	ВСТ
Dual 4-Bit Decade	None	'390				~				
Dual 4-Bit Binary	None	'393				~				
12-Bit Binary	Sync	'4040				~				
		'4020				V				
14-Bit Binary	Sync	'4060				~				
	}	'4061				~				Ì

# 8-Bit Binary Counters With Registers

DESCRIPTION	PARALLEL	TYPE				TECHN	IOLOGY			
DESCRIPTION	LOAD	ITPE	ALS	AS	F	нс	нст	AC	ACT	BCT
D	00	'590				~			T	
Parallel Register Outputs	38	'11590						~	V	
Parallel Register Inputs	38	'11593						~	~	

# NOTES:

✔ Product available in technology indicated



<sup>+</sup> New product planned in technology indicated

# DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

# **Encoders/Data Selectors/Multiplexers**

DESCRIPTION	OUTPUT	TYPE				Ti	ECHNOLO	GY			
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
		'157	~	~	~	~	~				
		'11157						~	~	}	
		'158	7	~	~	V					
		'11158						~	~		
Quad 2-to-1		'298		~							
		'257	>	V .	~	~	~				
	38	'11257				ļ		V	~		
	35	'258	V	1	V	V					
		'11258						~	1		
		'153	~	~	~	1					
		'11153						~	~		
-		'352	~	V							
Dual 4-to-1		'11352						~	V		
Dual 4-10-1		'253	~	~	V	~				-	
	38	'11253						V	V		
•	35	'353		~							
		'11353						~	V		
Hex 2-to-1 Universal Multiplexer	38	'857	~	~							
		'151	~	V	~	V					
		'11151						V	~		
8-to-1		'251	~		~	~					
	38	'11251					1	~	V		
		'354				V					
		'250		~							
16-to-1	38	'850		V							
		'851		~							
Full BCD		'147				~					
Cascadable Octal		'148				~					

# NOTES:

✔ Product available in technology indicated

<sup>+</sup> New product planned in technology indicated

# DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS (continued)

# **Decoders/Demultiplexers**

DECORIDETON	OUTDUT	7/05				TE	CHNOLO	GY	,		
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	нс	нст	AC	ACT	вст	ABT
Dual 2-to-4		'239				~	1				
		'11239				1		V			
Dural O to A		'139	~			~	V				
Dual 2-to-4		'11139						V	V		
	ос	'156	~								
		'138	~	~	~	~	~				
		'11138						V	V		
3-to-8		'238				V	~				
		'11238						V	V		
3-to-8 With		'131	~	~							
Address Registers		'137	~			~					
3-to-8 With Address Latches		'237				~					
4-to-10 BCD-to-Decimal		'42				V					
4-to-16		'154				~					
4-to-16 With		'4514				~					
Address Latches		'4515				V	1				
Dual 2-to-4 for Battery Backed-Up Memories		'2414								~	

# **Shifters**

DESCRIPTION	OUTDUT	TYPE				TE	CHNOLO	GY			
DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	HC	HCT	AC	ACT	вст	ABT
4-Bit Shifter	38	'350			V						

# NOTES:

✔ Product available in technology indicated

+ New product planned in technology indicated

# **COMPARATORS AND PARITY GENERATORS/CHECKERS**

# **Comparators**

			DESC	RIPTIO	N			7/0-				TECHN	OLOGY	,		
INPUT	P=Q	P=Q	P>Q	P>Q	P <q< th=""><th>OUTPUT</th><th>ENABLE</th><th>TYPE</th><th>ALS</th><th>AS</th><th>F</th><th>нс</th><th>нст</th><th>AC</th><th>ACT</th><th>вст</th></q<>	OUTPUT	ENABLE	TYPE	ALS	AS	F	нс	нст	AC	ACT	вст
4-Bit/8-Bit	Yes	No	Yes	No	Yes	2S	No	'85				1				
	Yes	No	No	No	No	ОС	Yes	'518	~							
8-Bit With	No	Yes	No	No	No	28	Yes	'520	7		~					
20-kΩ	INO	165	140	140	140	23	162	'11520						~	~	
Pullup	No	Yes	No	No	No	ОС	Yes	'522	1							
	No	Yes	No	Yes	No	2S	No	'682				~				
	Yes	No	No	No	No	ОС	Yes	'519	~							
	No	Yes	No	No	No	28	Yes	'521	<		1	Ī				
8-Bit	INO	105	INO	NO	110	25	Tes	'11521						V	1	
Standard	No	Yes	No	Yes	No	28	No	'684				V				
1.	No	Yes	No	No	No	28	Yes	'688	V			V				
,	No	Yes	No	No	No	oc	Yes	'689	~							
8-Bit Latched P	No	No	Yes	No	Yes	28	Yes	'885		~						
8-Bit Latched P and Q	Yes	No	Yes	No	Yes	L	Yes	'866		V						

# Address Comparators

DESCRIPTION	ОИТРИТ	TYPE				TE	CHNOLO	GΥ			
DESCRIPTION	ENABLE	ITPE	ALS	AS	F	нс	нст	AC	ACT	BCT	ABT
16-Bit to 4-Bit	Yes	'677	~			1					
12-Bit to 4-Bit	Yes	'679	~								

# Parity Generators/Checkers

DESCRIPTION	NO. OF	OUTDUT	TVDE				TE	CHNOLO	GY			
DESCRIPTION	BITS	OUTPUT	TYPE	ALS	AS	F	нс	нст	AC		ABT	
Odd/Even Generators/Checkers			'280	~	>	~	~					
			'11280						~	~		
	9		'286		~							
			'11286						~	V		

### NOTES:

- ✔ Product available in technology indicated
- + New product planned in technology indicated

# **ARITHMETIC CIRCUITS AND FIFO MEMORIES**

# **Parallel Binary Adders**

DESCRIPTION	ОИТРИТ	TYPE				TE	CHNOLOG	3Y			
DESCRIPTION	OUIFUI	ITPE	ALS	AS	F	НС	нст	AC	ACT	ВСТ	ABT
4-Bit		'283			~	V					

# Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DESCRIPTION	OUTPUT	TYPE				TE	CHNOLO	GY			
DESCRIPTION	COIPOI	1175	ALS	AS	F	HC	нст	AC	ACT	ВСТ	ABT
		'181		~							
4-Bit Arithmetic Logic Units:		'11181						~	~		
Function Generator		'381			~					BCT	
		'881		V							
4-Bit Arithmetic Logic Units With Ripple Carry		'382			V						
32-Bit Look-Ahead Carry Generators		'882		V		-					

# First-In, First-Out Memories (FIFOs)

DESCRIPTIO	N							TE	CHNOL	OGY				
SIZE	TYPE	OUTPUT	TYPE	LS	S	ALS	AS	F	нс	нст	AC	ACT	ВСТ	ABT
16 Words × 4 Bits	U	38	'232B			~								
,			'225		~									
16 Words x 5 Bits	U	38	'229B			V								
		• '	'233B			~								
32 Words × 9 Bits	В	38	'2238			~								
CAMPANA A Dia		38	'234			~								
64 Words × 4 Bits	U		'236			V								
64 Words × 5 Bits	U	38	'235			~								
64 Words × 8 Bits	U	38	'2232A			~								
64 Words × 9 Bits	U	38	'2233A			V								
0414/	U, C	38	7813									~		
64 Words x 18 Bits	U	38	7814									~		
			'7815	-										+
04145 de 00 DV	В, С	B, C 3S	'7816			1								+
64 Words × 36 Bits	1 11 0 36	'7817											+	
	U, C	38	'7818									+		+
D .104 .4			'2226							<b> </b>		+		
Dual 64 × 1	C	38	'2227									+		

# NOTES:

- † U = Unidirectional
- B = Bidirectional
- C = Clocked
- ✔ Product available in technology indicated
- + New product planned in technology indicated



# FIFO MEMORIES AND CLOCK DRIVER CIRCUITS

First-In, First-Out Memories (FIFOs) (continued)

DESCRIPTION	N							TE	CHNOL	OGY				
SIZE	TYPE†	OUTPUT	OUTPUT TYPE L	LS	S	ALS	AS	F	HC	нст	AC	ACT	ВСТ	ABT
D 1050 4			'2228									+		1
Dual 256 x 1	С	38	'2229									+		ļ
05014/-   10.00	U, C	38	7805									V		
256 Words × 18 Bits	U	38	'7806									V		
	U, C	38	'7803									V		T.
540.W 40.Dh.	U	38	7804									~		
512 Words × 18 Bits	B, C	38	7819								i			V
	В	38	'7820											V
512 Words × 32 Bits	B, C	38	7821									+		
512 Words × 36 Bits	B, C	38	7822									+		
	5	в зѕ	'2235									1		
	"	35	'2236									1		
1K Words × 9 Bits		-00	'7801									1		
	U, C	38	'7811									1		
	U	38	'7802									V		
1K Words × 36 Bits	U, C	38	'7823									+		
OK Wards . O Bit-	U, C	38	'7807									~		
2K Words x 9 Bits	U	38	'7808									V		

<sup>†</sup> U = Unidirectional

# **Clock Drivers**

DESCRIPTION	TYPE	TECHNOLOGY									
DESCRIPTION	ITPE	ALS	AS	F	нс	нст	AC	ACT	ВСТ	ABT	
Hex Inverting Clock Drivers/Buffers	'11204						V				
Dual 1-to-4 Clock Drivers/Buffers	'11208						~	~			
Octal Divide-by-2 Clock Drivers (6 Inverting, 2 Noninverting)	'303		V								
Octal Divide-by-2 Clock Drivers (8 Noninverting)	'305		V								
Octal Divide-by-2 Clock Drivers (4 Inverting, 4 Noninverting)	'304	-	~								
4.000-1.00-	'328										
1-to-6 Clock Drivers	'329									~	
4	'337									+	
1-to-8, Divide-by-2 Clock Drivers	'339	-								+	
Phase-Locked Loop (4-1x, 1-1/2x, 1-2x)	'338									+	

# NOTES:



B = Bidirectional

C = Clocked

<sup>✔</sup> Product available in technology indicated

<sup>+</sup> New product planned in technology indicated

# **ECL TRANSLATORS**

# **ECL-to-TTL or TTL-to-ECL Translators**

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE
		ос	10KHT5538
	ECL-to-TTL		100KT5538
Octol Buo Driver Investing	ECL-10-11L	38	10KHT5540
Octal Bus Driver, Inverting		35	100KT5540
	TTL-to-ECL	OE -	10KHT5542
<u> </u>	111-10-201	OE	100KT5542
		ос	10KHT5539
	501 to TT1	00	100KT5539
Octol Bus Driver Noninvesting	ECL-to-TTL	38	10KHT5541
Octal Bus Driver, Noninverting		35	100KT5541
	TTL-to-ECL	OE .	10KHT5543
	171-10-201		100KT5543
Octol D Type Letch True	ECL-to-TTL	38	10KHT5573
Octal D-Type Latch, True	ECL-10-11L	35	100KT5573
	ECL-to-TTL	38	10KHT5574
Octal D-Type Flip-Flop, True	ECL-10-11L	33	100KT5574
Octai D-Type Filp-Fi0p, 11de	TTL-to-ECL	OE	10KHT5578
	112-10-ECL		100KT5578

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	Mechanical Data

# **ABT OCTALS**

### **Features**

- EPICIIB™ BiCMOS process
- 0.8-μm CMOS core logic
- Bipolar output transistors
- Industry-standard corner-pin V<sub>CC</sub> and GND pinout
- -40/85° characterization
- DIP, SOIC, and EIAJ SSOP package options
- TI has established two alternate sources

### **Benefits**

- Sub-5-ns maximum propagation delays for improved cycle time and performance
- Very low standby power consumption
- –32-/64-mA drive capability for high fanout and advanced backplane interface
- Drop-in replaceable to existing layouts and designs for easy upgradeability
- Industrial temperature range for field applications
- Flexible approaches for many board-space-saving needs
- Standardization that comes from a common product approach

The following table lists ABT octal devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the General Purpose Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT563	20	Octal D-Type Transparent Latch
'ABT564	20	Octal D-Type Flip-Flop
'ABT648	24	Octal Registered Bus Transceiver
'ABT825	24	Octal Register
'ABT834	24	Octal Registered Bus Transceiver
'ABT845	24	Octal Latch
'ABT854	24	Octal Registered Bus Transceiver
'ABT864	24	9-Bit Transceiver

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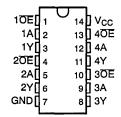
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, B = 0)
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

# description

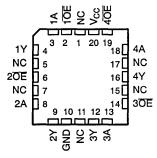
The 'ABT125 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT125 . . . J PACKAGE SN74ABT125 . . . D, DB, OR N PACKAGE (TOP VIEW)



SN54ABT125...FK PACKAGE (TOP VIEW)



NC-No internal connection

The SN74ABT125 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT125 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT125 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

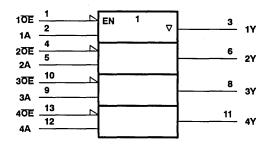
# FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
ŌE	Α	Y
L	Н	Н
L	L	L
н	X	Z



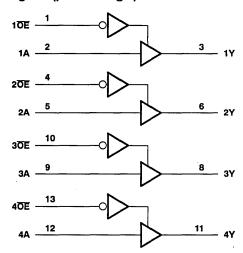
D3767, FEBRUARY 1991-REVISED OCTOBER 1992

# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



Pin numbers shown are for D, DB, J, and N packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the h	igh state or power-off state, VO	–0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT125	96 mA
•	SN74ABT125	128 mA
Input clamp current, $I_{iK}$ ( $V_i < 0$ )		
Output clamp current, IOK (VO < 0)		50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in	n still air): D package	
, , , , , , , , , , , , , , , , , , , ,		
	N package	
Storage temperature range	· · · · · · · · · · · · · · · · · · ·	-65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# recommended operating conditions (see Note 2)

		SN54	SN54ABT125		BT125	UNIT
		MIN	MAX	MIN	MAX	וואט
V <sub>CC</sub>	Supply voltage	4.5	5 5.5	4.5	5.5	V
VIH	High-level input voltage		2	2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
VI	Input voltage		V <sub>CC</sub>	0	Vcc	V
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
TA	Operating free-air temperature	-59	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST CONDITIO	NO.	1	A = 25°C	;	SN54A	BT125	SN74ABT125		UNIT
PARAMETER	Ì	TEST CONDITIONS			TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5		-	2.5		2.5		
Wass	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2	_			•
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -32 \text{ mA}$		2‡					2		
VoL	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 48 mA				0.55		0.55			<b>V</b>
VOL.	$V_{CC} = 4.5 \text{ V},$	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	•
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	$V_1 = V_{CC}$ or GND	V <sub>I</sub> = V <sub>CC</sub> or GND		-	±1		±1		±1	μΑ
l <sub>OZH</sub>	$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 2.7 V	V <sub>O</sub> = 2.7 V			50	Ĺ <u>.</u>	50		50	μΑ
lozL		V <sub>O</sub> = 0.5 V				-50		50		-50	μA
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±100				±100	μΑ
ICEX	$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>§</sup>	$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	l 0	Outputs high		1	250		250		250	μΑ
Icc	$V_1 = V_{CC}$ or GN		Outputs low		24	30		30		30	mA
	1 100 51 51		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V, One input at	Data inputs	Outputs enabled			1		1.5		1	
Δlcc¶	3.4 V, Other inputs		Outputs disabled			0.05		0.05		0.05	mA
	at V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
C <sub>o</sub>	$V_0 = 2.5 \text{ V or } 0$	).5 V			7						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54A	BT125	SN74A	BT125	UNIT	
	(INFOI)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	Δ	V	1	2.9	4.1	1	5.4	1	4.6	-Ins	
t <sub>PHL</sub>	Α	Y	1	2.5	4.6	1	5	1	4.9		
t <sub>PZH</sub>	ŌĒ	Y	1	2.9	4.2	1	5.2	1	5.1		
t <sub>PZL</sub>	OE		1	2.5	6.2	1	6.9	1	6.8	ns	
t <sub>PHZ</sub>	ŌĒ			1	3.8	5.4	1	6.3	1	6.2	
t <sub>PLZ</sub>	OE.	Y		3.5	5	1.5	6	1.5	5.5	ns	

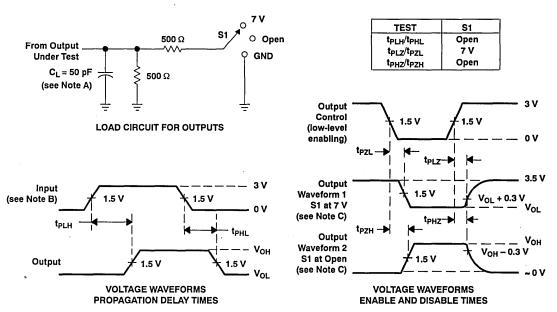


<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.





NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

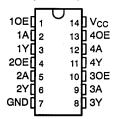
# description

The 'ABT126 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

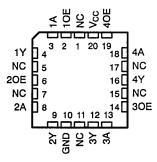
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT126 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT126 is characterized for operation from -40°C to 85°C.

### SN54ABT126...J PACKAGE SN74ABT126...D OR N PACKAGE (TOP VIEW)



# SN54ABT126...FK PACKAGE (TOP VIEW)



NC-No internal connection

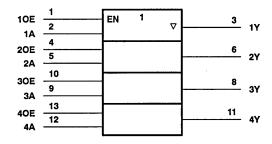
# FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT						
OE	Α	Y						
H.	Н	Н						
Н	L	L						
L	X	z						



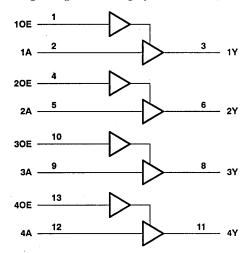
D3768, FEBRUARY 1991-REVISED OCTOBER 1992

# logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	–0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT126	
, SN74ABT126	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): D package	0.7 W
N package	
Storage temperature range	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# recommended operating conditions (see Note 2)

		SN54ABT126		6 SN74ABT126		UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
Vi	Input voltage	0	Vcc	0	Vcc	٧
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	ŝ

NOTE 2: Unused or floating inputs must be held high or low.



D3768, FEBRUARY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS			A = 25°C	;	SN54A	BT126	SN74ABT126		דואט
PARAMETER				TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},  I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
\ \v.	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		. 3			3		3		<sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		2			2				
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55	,	0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	
l <sub>i</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$		-		±1		±1		±1	μА
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
lozL	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μA
loff	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μА
ICEX	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μА
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high		1	250		250		250	μA
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	1 1 2 1 2 2 3 4 4 1 2	Outputs disabled		0.5	250		250		250	μА
Δlcc <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,	Outputs enabled			1.5		1.5		1.5	mA
	Other inputs at V <sub>CC</sub> or GND	Outputs disabled		,	50		50		50	μΑ
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	V,	<sub>CC</sub> = 5 V <sub>A</sub> = 25°C	;	SN54A	BT126	SN74A	BT126	UNIT
	(1141-01)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tpLH	Α	^	v	1	2.9	4.2	1		1	4.4	ns
t <sub>PHL</sub>		•	1	2.5	4.3	1		1	4.6	115	
<sup>t</sup> PZH	OE		1.9	4.4	5.8	1.9		1.9	6.5	ns	
t <sub>PZL</sub>	OL.	1	1.9	4.4	5.9	1.9		1.9	6.5	120	
t <sub>PHZ</sub>	OE Y	V	1	3	5.2	1		1	5.8	ns	
t <sub>PLZ</sub>		1	3	4.9	1		1	5.5	115		



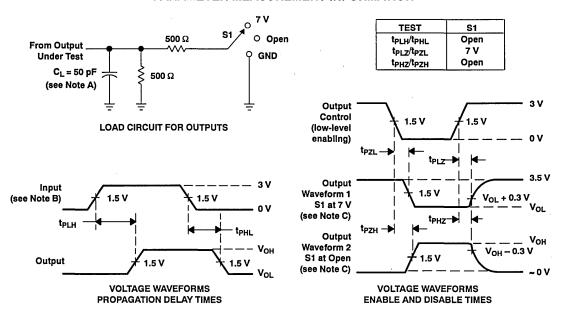
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

D3768, FEBRUARY 1991-REVISED OCTOBER 1992

### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS098B-D3702, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

# description

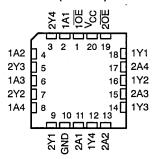
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT241 and 'ABT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary  $\overline{OE}$  and  $\overline{OE}$  inputs.

The 'ABT240 is organized as two 4-bit buffers/line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

SN54ABT240 . . . J PACKAGE SN74ABT240 . . . DB, DW, OR N PACKAGE (TOP VIEW)

10E [ 1A1 [ 2Y4 [ 1A2 [ 2Y3 [ 1A3 [ 2Y2 [	2 3 4 5 6 7	20 V <sub>CC</sub> 19 20E 18 1Y1 17 2A4 16 1Y2 15 2A3 14 1Y3
1A3 [	6 7	<sub>15</sub> ] 2A3

# SN54ABT240 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT240 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

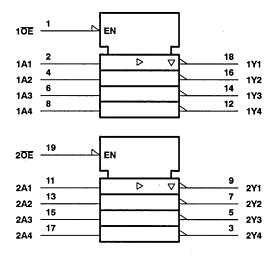
The SN54ABT240 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT240 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

# FUNCTION TABLE (each buffer)

	•	
INP	JTS	OUTPUT
OE	Α	Y
L,	Н	L
L	L	н
Н	X	z

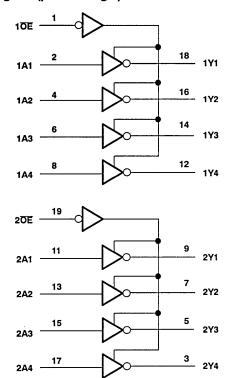


# logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT240	96 mA
SN74ABT240	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	0.85 W
N package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SCBS098B-D3702, JANUARY 1991-REVISED OCTOBER 1992

# recommended operating conditions (see Note 2)

			SN54A	BT240	SN74A	BT240	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5:5	4.5	5.5	V
VIH	High-level input voltage		2	(4)	2		V
V <sub>IL</sub>	Low-level input voltage			<i>44</i> 0.8		0.8	V
Vı	Input voltage		0,4		0	Vcc	V
loн	High-level output current		Ş	-24		-32	mA
loL	Low-level output current		ŞÕ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Æ	5		5	ns/V
TA	Operating free-air temperature		<b>~</b> –55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			ד	' <sub>A</sub> = 25°C	;	SN54A	BT240	SN74ABT240		TINU
PARAMETER	'-	1E31 CONDITIONS			TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	ONII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA	•			-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5	•	•	2.5		2.5		
W	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				1 °
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -32 \text{ mA}$		2‡		•			2		]
Vol	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	ľ
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V <sub>1</sub>	V <sub>I</sub> = V <sub>CC</sub> or GN	1D			±1		#L		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$				50		<b>₹</b> 50		50	μΑ
lozL	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50		<i>≲</i> ⊬50		-50	μΑ
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100	, A	ξ.		±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	.Q	50		50	μА
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	<b>∠5</b> 0	-180	-50	-180	mA
	V 55V		Outputs high		1	250	Ş€"	250		250	μΑ
lcc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0,$	Outputs low		24	30	*	30		30	mA
	11 = VCC 5/ GIVE		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data innuta	Outputs enabled			1.5		1.5		1.5	
ΔICC	One input at 3.4 V, Other inputs at	Outputs disabled			0.05		0.05		0.05	mA	
	V <sub>CC</sub> or GND	Control inputs	Control inputs			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3					·	pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V	•			8						рF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54ABT240		SN74ABT240		UNIT
	(INFO1)	(0011-01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	^	· ·	1	2.9	4.1	0.8	5.5	1	4.8	ns
t <sub>PHL</sub>	^	A Y	1.6	3.1	4.3	15	\$5.5	1.6	4.8	113
t <sub>PZH</sub>	ŌĒ	Y	1.1	3.1	4.7	0:8	₹ 7.5	1.1	5.2	ns
t <sub>PZL</sub>	OE		1.1	2.7	5.8	<b>∱0.8</b> ≾	7.7	1.1	6.2	115
t <sub>PHZ</sub>	ŌE	V .	1.8	4.6	5.7	1.7	7	1.8	6.4	ns
t <sub>PLZ</sub>		OE   Y	1.6	4	5.4	1.3	7.2	1.6	5.8	115

### PARAMETER MEASUREMENT INFORMATION TEST S1 O Open 500 $\Omega$ tplH/tpHL Open From Output 7 V tpLz/tpzL GND **Under Test** t<sub>PHZ</sub>/t<sub>PZH</sub> Open C<sub>L</sub> = 50 pF 500 $\Omega$ (see Note A) 3 V Output Control 1.5 V 1.5 V LOAD CIRCUIT FOR OUTPUTS (low-level enabling) 3.5 V Output Input Waveform 1 V<sub>OL</sub> + 0.3 V (see Note B) S1 at 7 V $v_{ol}$ (see Note C) tpH7 Output $V_{OH}$ Waveform 2 V<sub>OH</sub> $V_{OH} - 0.3 V$ S1 at Open Output (see Note C) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES**

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{<}$  10 MHz,  $Z_{0}$  = 50  $\Omega$ ,  $t_{f}$   $_{<}$  2.5 ns,  $t_{f}$   $_{<}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



# SN54ABT241, SN74ABT241 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

D3703, JANUARY 1991-REVISED OCTOBER 1992

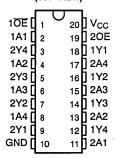
- Space-Saving Package Option:
   Shrink Small-Outline Package (DB) Features
   EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

# description

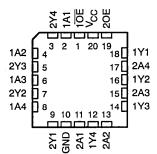
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT241 and 'ABT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary  $\overline{OE}$  and  $\overline{OE}$  inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.  $\overline{OE}$  should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

SN54ABT241 ... J PACKAGE SN74ABT241 ... DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT241 . . . FK PACKAGE (TOP VIEW)



The SN74ABT241 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT241 is characterized for operation from –40°C to 85°C.



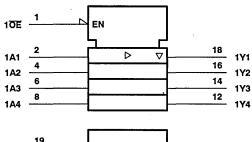
### **FUNCTION TABLES**

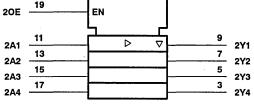
INPL	JTS	OUTPUT
10E	1A	1Y
L	Н	Н
L	L	L
Н	Х	z

INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
н	L	L
L	X	z

# logic symbol†

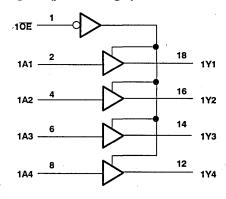
**PRODUCT PREVIEW** 

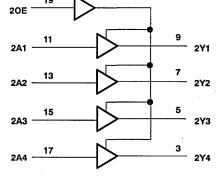




<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)





D3703, JANUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwis	ie noted)!
Supply voltage range, V <sub>CC</sub>	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_0 \ldots -0$	.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT241	96 mA
SN74ABT241	128 mA
Input clamp current, $I_{ K }(V_{ } < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	0.5 W

Storage temperature range .......—65°C to 150°C

# recommended operating conditions (see Note 2)

			SN54A	BT241	SN74A	BT241	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vi	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# SN54ABT241, SN74ABT241 **OCTAL BUFFERS/DRIVERS** WITH 3-STATE OUTPUTS D3703, JANUARY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD 4445750	TEGT COMPLETIONS		T	A = 25°C	;	SN54A	BT241	SN74ABT241			
PARAMETER	TEST CONDITIONS			MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA	*		· · · · · · · · · · · · · · · · · · ·	-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3	-		3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -24 \text{ mA}$					2				ľ
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m/	\	2‡					2		
V.	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA					0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	, v
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or G	= V <sub>CC</sub> or GND			±1		±1		±1	μΑ
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μA
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	٧			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V	1 0	Outputs high		1	250		250		250	μА
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low		24	30		30		30	mΑ
	11 - 100 or and		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data issuta	Outputs enabled			1.5		1.5		1.5	
ΔICC	One input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND Control inputs					1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V				8						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

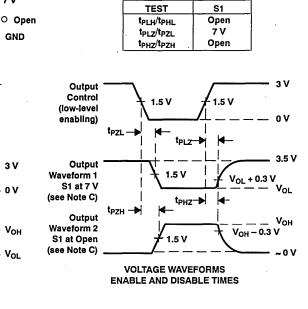
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT241	SN74ABT241		UNIT
İ			MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
t <sub>PLH</sub>	Α	Y	1	2.6	4.1	0.8	5.3	1	4.6	ns
t <sub>PHL</sub>	^		1	2.9	4.2	0.8	5	1	4.6	
t <sub>PZH</sub>	OE or OE	Y	1.1	4.8	6.3	1	7	1.1	6.8	no
t <sub>PZL</sub>	OE OF OE		1.3	4.3	5.8	1	7	1.3	6.8	ns
t <sub>PHZ</sub>	U7	V	1.6	4.6	6.1	0.8	7.9	1.6	7.1	ns
t <sub>PLZ</sub>	OE OF OE	Y	1	3.9	5.4	0.8	6.2	1	5.9	

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

Q GND



NOTES: A. C. includes probe and jig capacitance.

From Output

Input

Output

(see Note B)

**Under Test** 

C<sub>L</sub> = 50 pF

(see Note A)

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

1.5 V

**tPHL** 

500 Ω

**500** Ω

LOAD CIRCUIT FOR OUTPUTS

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES

Figure 1. Load Circuit and Voltage Waveforms

SCBS099B-D3655, JANUARY 1991-REVISED OCTOBER 1992

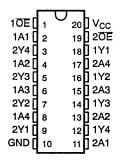
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (–32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

# description

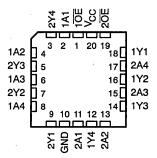
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT240 and 'ABT241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical OE (active-low output- enable) inputs, and complementary OE and OE inputs.

The 'ABT244 is organized as two 4-bit buffers/line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

SN54ABT244... J PACKAGE SN74ABT244... DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT244...FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

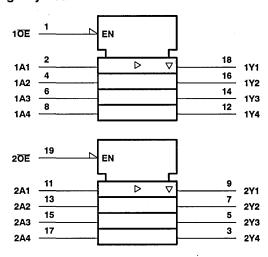
The SN74ABT244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT244 is characterized for operation from -40°C to 85°C.

# FUNCTION TABLE (each buffer)

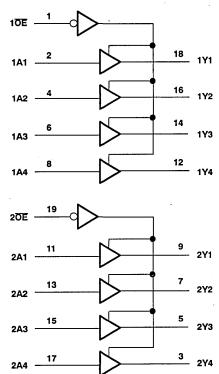
	`	
INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	H
L	L	Н
н	Х	l z

# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		0.5 V to 7 V
Voltage applied to any output in the high state or	power-off state, V <sub>O</sub>	0.5 V to 5.5 V
Current into any output in the low state, Io: SN5	4ABT244	96 mA
SN7	4ABT244	128 mA
Input clamp current, $I_{IK}(V_I < 0)$		
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still a	air): DB package	0.5 W
, , , , , , , ,	DW package	0.85 W
	N package	1.3 W
Storage temperature range		65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# recommended operating conditions (see Note 2)

		SN54ABT244	SN74ABT244	-I UNIT
		MIN MAX	MIN MAX	וואט
Vcc	Supply voltage 4	4.5 5.	4.5 5.5	V
VIH	High-level input voltage	2	2	V
VIL	Low-level input voltage	0.0	0.8	V
Vı	Input voltage	0 V <sub>C</sub>	0 V <sub>CC</sub>	V
loн	High-level output current	-24	-32	mA
loL	Low-level output current	41	64	mA
Δt/Δν	Input transition rise or fall rate		5	ns/V
TA	Operating free-air temperature	-55 129	-40 85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETIONS		Т	A = 25°C	;	SN54A	BT244	SN74ABT244		UNIT	
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
, , , , , , , , , , , , , , , , , , ,	V <sub>CC</sub> = 5 V,	5 V, I <sub>OH</sub> = – 3 mA				····	3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				· ·
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA		2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	/ <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	· •
11	V <sub>CC</sub> = 5.5 V,	VI = VCC or GI	ND			±1		±1		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	,	50		50	μΑ
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
			Outputs high		1	250		250		250	μА
lcc	$V_{CC} = 5.5 \text{ V},$ $V_{L} = V_{CC} \text{ or GND}$	$I_{O}=0,$	Outputs low		24	30		30		30	mA
	AI = ACC OL GIAD		Outputs disabled		0.5	250		250		250	μА
	V <sub>CC</sub> = 5.5 V,	D-1	Outputs enabled			1.5		1.5		1.5	
Δlcc	One input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND					1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	•			3						pF
C <sub>o</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$				8			-			pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

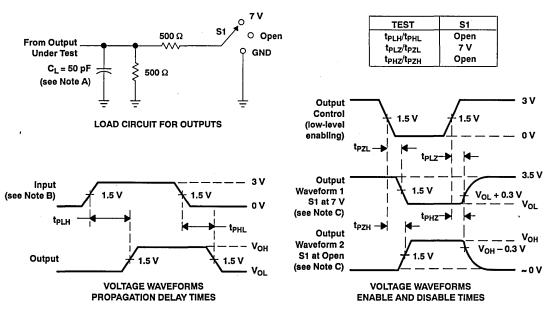
This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT244	SN74ABT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	, , [
t <sub>PLH</sub>	^	V	1	2.6	4.1	1	5.3	1	4.6	ns
t <sub>PHL</sub>	A	ī	1	2.9	4.2	1	5	1	4.6	
t <sub>PZH</sub>	OE	V	1.1	3.1	4.6	0.8	5.7	1.1	5.1	
t <sub>PZL</sub>	""	, ,	2.1	4.1	5.6	1.2	7.9	2.1	6.1	ns
t <sub>PHZ</sub>	OE	. Y	2.1	4.1	5.6	1.2	7.6	2.1	6.6	ns
t <sub>PLZ</sub>	)		1.7	3.7	5.2	1	7.9	1.7	5.7	

# PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



# SN54ABT245, SN74ABT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

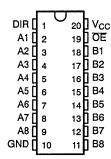
SCBS081B-D3656, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA IOH, 64-mA IOL)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

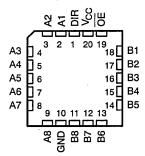
# description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

SN54ABT245...J PACKAGE SN74ABT245...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT245 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT245 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT245 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

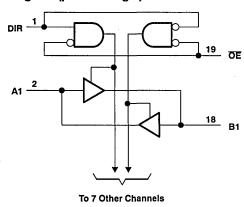
### **FUNCTION TABLE**

INP	UTS	OPERATION
Œ	OE DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

# logic symbol<sup>†</sup>

### 3EN1[BA] 3EN2[AB] 18 В1 2∇ 17 **A2 B2** 16 **B3** АЗ 15 A4 **B4** 14 **B**5 A5 13 A6 **B6** 12 **B7** Δ7 11 **B8 A8**

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	to 7 V
Voltage applied to any output in the high state or power-off state, V <sub>O</sub>	5.5 V
Current into any output in the low state, Io: SN54ABT245	
SN74ABT245	28 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	18 mA
Output clamp current, $I_{OK}(V_O < 0)$	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package 0	.85 W
N package	1.3 W
Storage temperature range65°C to	150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# recommended operating conditions (see Note 2)

		SN54A	BT245	SN74AI	BT245	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	Vcc	0	Vcc	V
Гон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T	A = 25°C	;	SN54A	BT245	SN74ABT245		UNIT
PARAMETER	'5	SICONDITION	15	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5	1,000	2.5		
1 1	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA	2			2				<b>'</b>	
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$		2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 64 \text{ mA}$					0.55‡				0.55	v
11	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА
l ''	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΛ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	$V_0 = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 V$		-50	-140	-180	-50	-180	-50	180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		5	250		250		250	μA
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		22	30		30		30	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		1	250		250		250	μΑ
	$V_{CC} = 5.5 \text{ V},$	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
Δlcc#	One input at 3.4 V, Other inputs at	Data iliputs	Outputs disabled			50		50		50	μΑ
	V <sub>CC</sub> or GND Control inp					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT245		SN74ABT245	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	2.6	4.1	1	4.8	1	4.6	ns
t <sub>PHL</sub>			. 1	2.9	4.2	1	4.8	1	4.6	
t <sub>PZH</sub>	ŌĒ	A or B	1.3	3.3	4.8	1	5.9	1.3	5.3	ns
t <sub>PZL</sub>			2.3	4.3	5.8	2	7.5	2.3	6.3	
t <sub>PHZ</sub>	OE	A or B	1.7	4.7	6.2	2.2	7.4	1.7	7.2	–l ns
t <sub>PLZ</sub>			1.7	4.3	5.8	2	6.5	1.7	6.3	

Il This data sheet limit may vary among suppliers.

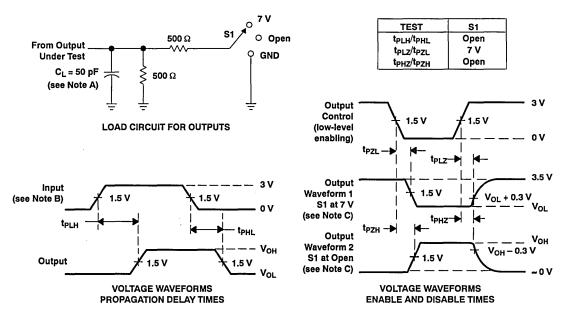
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

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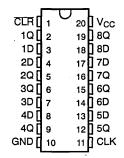
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

# description

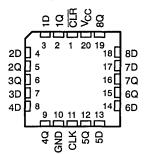
The 'ABT273 is an 8-bit positive edge-triggered D-type flip-flop with a direct clear (CLR) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

SN54ABT273...J PACKAGE SN74ABT273...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT273...FK PACKAGE (TOP VIEW)



The SN74ABT273 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT273 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT273 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

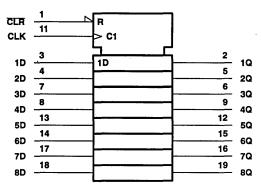
# FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT				
CLR	CLR CLK D		Q			
L	Х	Х	L			
Н	Ť	Н	н			
Н	Ť	L	L			
Н	L	_X	$Q_0$			



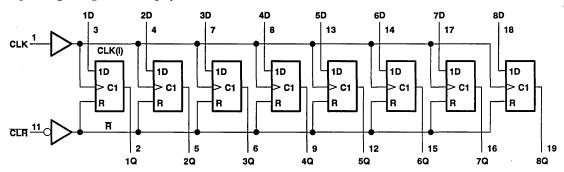
D3769, FEBRUARY 1991-REVISED OCTOBER 1992

#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT273	96 mA
SN74ABT273	128 mA
Input clamp current, $I_{IK}$ ( $V_1 < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	0.85 W
N package	1.3 W
Storage temperature range	65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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#### recommended operating conditions (see Note 2)

			SN54A	BT273	SN74A	BT273	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	•	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
loн	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	1	5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	10	٦	A = 25°C	;	SN54A	BT273	SN74A	BT273	UNIT
PANAMEIER	lesi condition	15	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
ViK	$V_{CC} = 4.5 \text{ V},  I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
Voh	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		3			3		3		v
VOH	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$		2			2				·
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		
V	V <sub>CC</sub> = 4.5 V, 1 <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	V
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μΑ
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ
loff	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
l <sub>O</sub> \$	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0	Outputs high		1	250		250		250	μА
lcc	V <sub>L</sub> = V <sub>CC</sub> or GND	Outputs low		24	30		30		30	mA
	1, 168 91 9115	Outputs disabled		0.5	250		250		250	μΑ
Δlcc	$V_{CC} = 5.5 \text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V									pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V									pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> =		SN54ABT273		SN74ABT273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			150		150		150	MHz
		CLK high	3.3		3.3		3.3		
tw	Pulse duration	CLK low	3.3		3.3		3.3		ns
		CLR low	3.5		3.5		3.5		
		Data high	1		1		1		ns
t <sub>su</sub>	Setup time before CLK†	Data low	1.5		1.5		1.5		
		CLR high			i				ns
th	Hold time after CLK↑	Data high or low	2†		2†		2†		ns

<sup>†</sup> This data sheet limit may vary among suppliers.

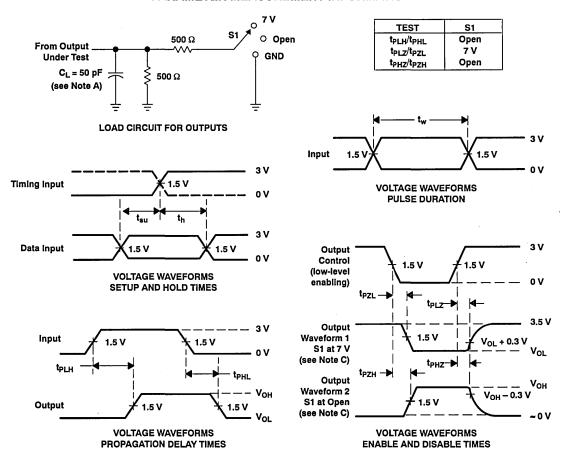
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT273	SN74A	UNIT	
	( 5.)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150	200		150		150		MHz
t <sub>PLH</sub>	CLK	Q	2.2	4.2	5.7	2.2		2.2	6.2	ns
t <sub>PHL</sub>	OLK	l '	3.1	5.1	6.6	3.1		3.1	7.1	115
t <sub>PHL</sub>	CLR	Q	2.4	4.1	6.2	2.4		2.4	6.7	ns



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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

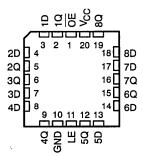
The eight latches of the 'ABT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT373...J PACKAGE SN74ABT373...DB, DW, OR N PACKAGE (TOP VIEW)

		T	_	ì
OE [		O	20	] v <sub>cc</sub>
1Q [			19	] 8Q
1D [	3		18	] 8D
2D [				] 7D
2Q [				] 7Q
3Q [			15	] 6Q
3D [	7		14	] 6D
4D [	8		13	] 5D
4Q [	9		12	] 5Q
GND [	10		11	LE

SN54ABT373...FK PACKAGE (TOP VIEW)



The output-enable (OE) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT373 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT373 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT373 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

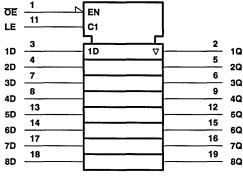
EPIC-IIB is a trademark of Texas Instruments Incorporated.

D3661, JANUARY 1991-REVISED OCTOBER 1992

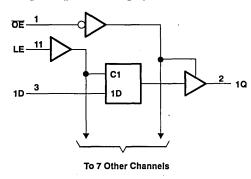
# FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L.	Н	L	L
L	L	X	$Q_0$
н	×	x	z

#### logic symbol†



#### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>
nput voltage range, V <sub>I</sub> (see Note 1)
oltage range applied to any output in the high state or power-off state, $V_0 \ldots -0.5  V$ to 5.5 V
Current into any output in the low state, Io: SN54ABT373
SN74ABT373 128 mA
nput clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package
DW package 0.85 W
N package
Storage temperature range

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3661, JANUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54A	BT373	SN74A	BT373	UNIT
			MIN	MAX	MIN	MAX	I ONLI
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			· 48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST SOURITION	110	Т	A = 25°C	;	SN54A	BT373	SN74A	BT373	
PARAMETER	TEST CONDITION	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},  I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
V <sub>OH</sub>	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		3			3		3		v
VOH	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$		2			2				
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V},  I_{OL} = 48 \text{ mA}$				0.55		0.55			V
VOL.	$V_{CC} = 4.5 \text{ V},  I_{OL} = 64 \text{ mA}$				0.55‡				0.55	
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μA
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μA
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ
loff	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	· μA
I <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
l <sub>O</sub> §	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high		1	250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	V1 = VCC 31 3112	Outputs disabled		0.5	250		250		250	μА
Δlcc <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,				1.5		1.5		1.5	mA
TICC.	Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	IIIA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V			6						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# **SN54ABT373, SN74ABT373 OCTAL TRANSPARENT D-TYPE LATCHES** WITH 3-STATE OUTPUTS D3661, JANUARY 1991-REVISED OCTOBER 1992

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

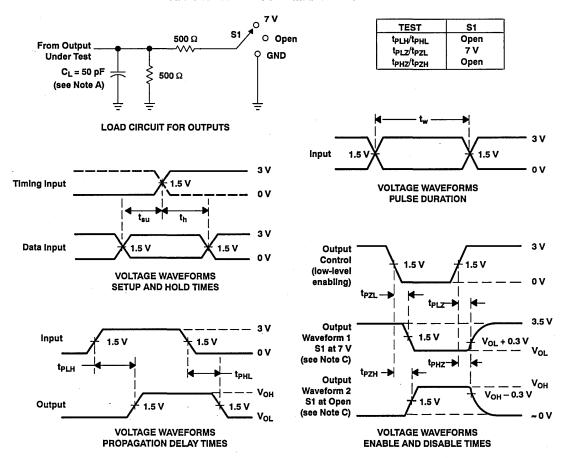
			V <sub>CC</sub> =	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C SN54ABT373		SN74AI	BT373	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high		3.3		3.3		3.3		ns
	Setup time, data before LE↓	High	1.9		2.8		1.9		no
t <sub>su</sub>	Setup time, data before LE‡	Low	1.5		2.8		1.5		ns
th	Hold time, data after LE↓	High or low	1		2.5		1		ns

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T 25°C		SN54ABT373		SN74ABT373		UNIT		
	( 0.)	(3311 \$1)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	D	Q	1.9	3.9	5.4	1.5	6.9	1.9	5.9	ns	
t <sub>PHL</sub>			2.2	4.2	5.7	2	7.2	2.2	6.2	"5	
t <sub>PLH</sub>	LE	Q	2.6	4.6	6.1	2	7.8	2.6	6.6	ns	
t <sub>PHL</sub>	LE	١	•	3.2	5.2	6.7	2.5	7.8	3.2	7.2	lis
t <sub>PZH</sub>	Œ	^	1.2	3.2	4.7	1	6.2	1.2	5.2		
t <sub>PZL</sub>	OE .	Q	2.7	4.7	6.2	1.5	7.2	2.7	6.7	ns	
t <sub>PHZ</sub>	ŌĒ		2.5	4.9	6.4	2.5	8.2	2.5	6.9		
t <sub>PLZ</sub>	OE .	Q	2	4.5	6	2	7	2	6.5	ns	

D3661, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS111A-D3770, FEBRUARY 1991-REVISED OCTOBER 1992

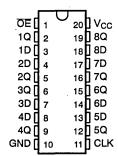
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

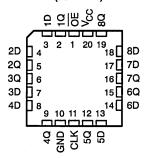
These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ABT374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

SN54ABT374... J PACKAGE SN74ABT374... DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT374...FK PACKAGE
(TOP VIEW)



A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (OE) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT374 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT374 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT374 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

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SCBS111A-D3770, FEBRUARY 1991-REVISED OCTOBER 1992

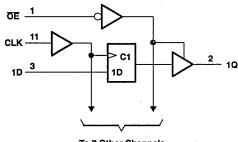
# FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	<b>†</b>	L	L
L	L	Χ	Q <sub>0</sub>
Н	X	X	z

#### logic symbol†

#### ΕN 11 - C1 1D 1Q 1D 5 2Q 2D 7 6 3Q 3D 9 4D 4Q 12 13 5Q 5D 14 15 **6Q** 16 17 7Q 18 19 ЯD

#### logic diagram (positive logic)



To 7 Other Channels

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, v <sub>CC</sub>	–0.5 V to / V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or	power-off state, V <sub>O</sub> 0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT3	374 96 mA
SN74ABT3	374 128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): D	DB package 0.5 W
	W package 0.85 W
N	I package
Storage temperature range	65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT374, SN74ABT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS111A-D3770, FEBRUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54A	BT374	SN74A	BT374	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage		-	0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		- 55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITION		T	A = 25°C		SN54A	BT374	SN74A	UNIT	
PARAMETER	1E31 CONDITIONS			TYP	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
V	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA					2				v
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA			•	0.55‡				0.55	_ v
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μА
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		50		-50	μA
IOFF	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
I <sub>O</sub> §	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	180	mA
	V 55 V 0	Outputs high			250		250		250	μA
Icc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			30		30		30	mA
	11-166 31 3115	Outputs disabled			250		250		250	μА
ΔICC	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	-			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			2.5						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# **SN54ABT374, SN74ABT374** OCTAL EDGÉ-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS111A-D3770, FEBRUARY 1991-REVISED OCTOBER 1992

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

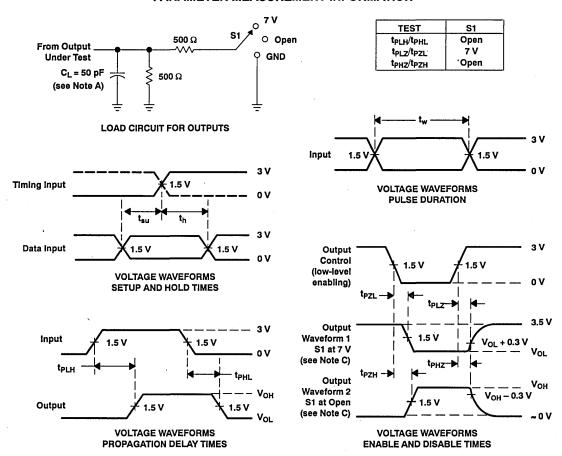
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54A	BT374	SN74AI	BT374	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
	Setup time before CLK†	Data high	1		2.5		1		ns
t <sub>su</sub>	Setup time belore CENT	Data low	1.9 <sup>†</sup>		2.5		1.9 <sup>†</sup>		115
t <sub>h</sub>	Hold time after CLK↑	Data high or low	1.6 <sup>†</sup>		2.5		1.6 <sup>†</sup>		ns

<sup>&</sup>lt;sup>†</sup> This data sheet limit may vary among suppliers.

#### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT374	SN74A	UNIT	
	( 0.)	(001101)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	.
f <sub>max</sub>			150	200		150		150		MHz
t <sub>PLH</sub>	CLK	a	2.2	4.2	5.7	1.8	6.6	2.2	6.2	ns
t <sub>PHL</sub>	OLK		3.1	5.1	6.6	2.6	7.6	3.1	7.1	
t <sub>PZH</sub>	Œ	Q	1.2	3.2	4.7	0.8	5.7	1.2	5.2	ns
t <sub>PZL</sub>	OE	ď	2.7	4.7	6.2	1.5	7.2	2.7	6.7	115
t <sub>PHZ</sub>	ŌĒ	Q	2.5	4.5	6	1.3	7.2	2.5	6.5	ns
t <sub>PLZ</sub>		ď	2	4.5	6	1	7	2	6.5	113

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT377, SN74ABT377 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

D3771, FEBRUARY 1991-REVISED OCTOBER 1992

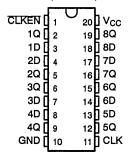
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (–32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

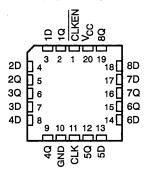
The 'ABT377 is a 8-bit positive-edge-triggered D-type flip-flop with a clock (CLK) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Data (D) input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable (CLKEN) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock (CLK) input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at CLKEN.

SN54ABT377 ... J PACKAGE SN74ABT377 ... DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT377 . . . FK PACKAGE (TOP VIEW)



The SN74ABT377 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT377 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT377 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

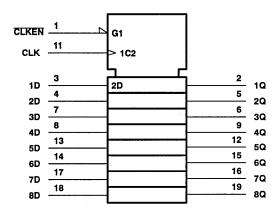
EPIC-IIB is a trademark of Texas Instruments Incorporated.

D3771, FEBRUARY 1991-REVISED OCTOBER 1992

# FUNCTION TABLE (each flip-flop)

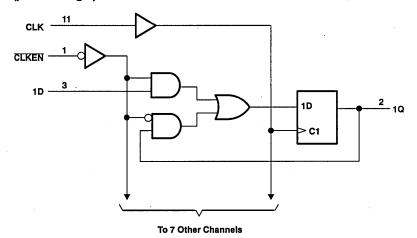
11	NPUTS		OUTPUT
CLKEN	CLK	a	
Н	Х	Х	Q <sub>0</sub>
L	Ť	н	H.
L	1	L	L
×	L	X	Q <sub>0</sub>

# logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



# SN54ABT377, SN74ABT377 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

D3771, FEBRUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> 0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT377
SN74ABT377
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
DW package
N package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54A	BT377	SN74A	BT377	- UNIT
ĺ			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature	· · · · · · · · · · · · · · · · · · ·	-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# SN54ABT377, SN74ABT377 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Т	A = 25°C	),	SN54A	BT377	SN74A	TINU	
PANAMETER	TEST CONDITIONS			TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA	/ <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2	<u> </u>	-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA					3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA					2				, v
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	· •
11	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
loff	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			. 50		50		50	μΑ
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	50	-180	mA
l	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0,	Outputs high		1	250		250		250	μΑ
Icc	V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs low	T	24	30		30	ĺ	30	mA
Δlcc <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		-	3		<b></b>				pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> =		SN54ABT377		SN74ABT377		דואט	
1			MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency		0	150	0	150	0	150	MHz	
t <sub>w</sub>	Pulse duration	CLK high or low	3.3		3.3		3.3		ns	
	Satura time hafara CLIVA	Data high or low	2		2.5		2			
เ <sub>รน</sub>	su Setup time before CLK†	CLKEN high or low	3		3		3		ns	
	Hold time after CLK↑	Data high or low	1.8#		1.8#		1.8#			
t <sub>h</sub>	Hold time after CERT	CLKEN high or low	1.8#		1.8#		1.8#		ns	

<sup>#</sup> This data sheet limit may vary among suppliers.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

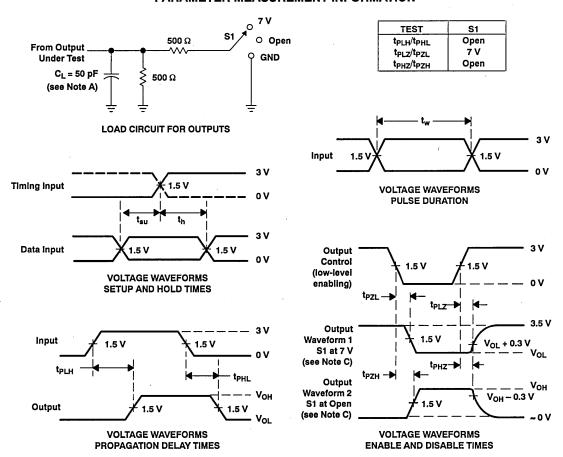
PARAMETER FROM (INPUT)	Y .	то (оитрит)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT377		SN74ABT377		UNIT	
	( ,		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
t <sub>РLН</sub>	CLK	_	2.2	4.5	6	2.2	7	2.2	6.5	
t <sub>PHL</sub>	OLK	Q	3.1	5.3	6.8	2	7.6	3.1	7.3	ns

<sup>&</sup>lt;sup>‡</sup> On products compliant to MiL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>&</sup>lt;sup>5</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_1 \leq 2.5 \text{ ns}$ ,  $t_1 \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

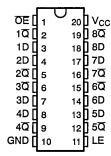
D3772, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (–32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

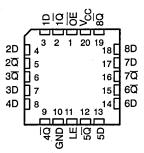
#### description

The 'ABT533 is an 8-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT533...J PACKAGE SN74ABT533...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT533 ... FK PACKAGE (TOP VIEW)



When the latch-enable (LE) input is high, the  $\overline{Q}$  outputs follow the complements of the data (D) inputs. When LE is taken low, the  $\overline{Q}$  outputs are latched at the inverse of the levels set up at the D inputs. The 'ABT533 provides inverted data at its outputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT533 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT533 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT533 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

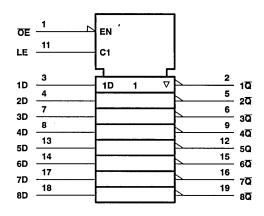


D3772, FEBRUARY 1991-REVISED OCTOBER 1992

# FUNCTION TABLE (each latch)

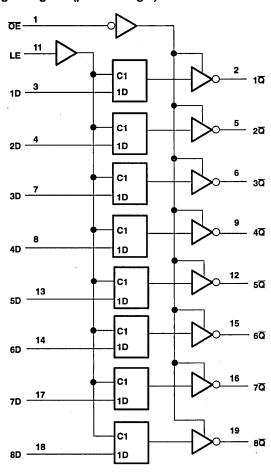
	INPUTS	OUTPUT	
ŌĒ	LE	D	<u> </u>
L	Н	Н	L
L	Н	L	н
L	L	Х	ಠಂ
н	X	Х	Z

### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)





D3772, FEBRUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage range, V <sub>CC</sub> 0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT533
SN74ABT533 128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
<b>DW</b> package
N package 1.3 W

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

			SN54A	BT533	SN74A	BT533	UNIT
			MIN	MAX	MIN	MAX	ONII
V <sub>CC</sub>	V <sub>CC</sub> Supply voltage			5.5	4.5	5.5	٧
V <sub>IH</sub> High-level input voltage			2		2		٧
V <sub>IL</sub>	V <sub>IL</sub> Low-level input voltage			8.0		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	٧
Гон	High-level output current			-24		-32	mA
l <sub>OL</sub>	I <sub>OL</sub> Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	T <sub>A</sub> Operating free-air temperature			125	-40	85	ů

NOTE 2: Unused or floating inputs must be held high or low.

D3772, FEBRUARY 1991-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST SOURITION		7	A = 25°C	;	SN54A	BT533	SN74ABT533		UNIT
PARAMETER	TEST CONDITION	NS .	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$		2			2				· •
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	· •
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μΑ
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ
loff	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>§</sup>	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-140	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high		1	250		250		250	μΑ
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	11 - 100 01 0115	Outputs disabled		0.5	250		250		250	μΑ
	V 55V 000 included 0.4V	Outputs enabled			1.5		1.5		1.5	mA
ΔICC	$V_{CC} = 5.5 \text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND	Outputs disabled			50	-	50		50	μΑ
1	Carlot impose at 100 of Grid	Control inputs			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V									pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V									pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 5 V.

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C MIN MAX					SN74AI	BT533	UNIT
			MIN			MAX	MIN MAX				
t <sub>w</sub>	Pulse duration, LE high or low	,			1				ns		
	Setup time, data before LE↓	High									
t <sub>su</sub>	Setup time, data before LE‡	Low							ns		
th	Hold time, data after LE↓	High or low	1.5#		1.5#		1.5#		ns		

<sup>#</sup> This data sheet limit may vary among suppliers.

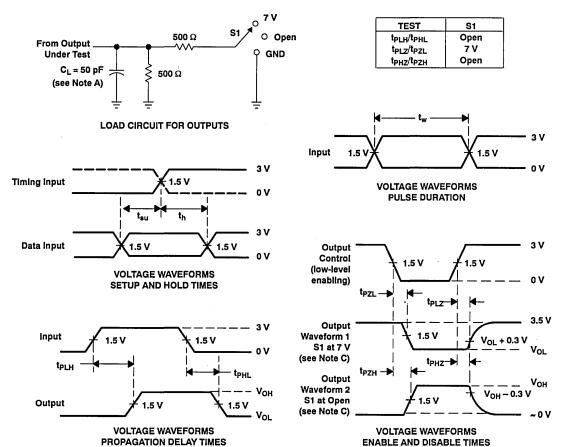
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

D3772, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

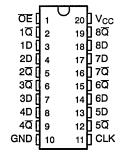
D3773, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OI</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

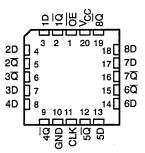
#### description

The 'ABT534 is an 8-bit flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT534 . . . J PACKAGE SN74ABT534 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT534 . . . FK PACKAGE (TOP VIEW)



The eight flip-flops of the 'ABT534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic levels that were set up at the data (D) inputs. The 'ABT534 provides inverted data at its outputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT534 is packaged in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT534 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT534 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

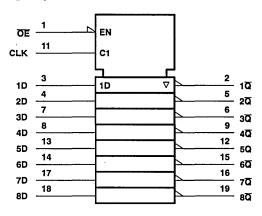


D3773, FEBRUARY 1991-REVISED OCTOBER 1992

# FUNCTION TABLE (each flip-flop)

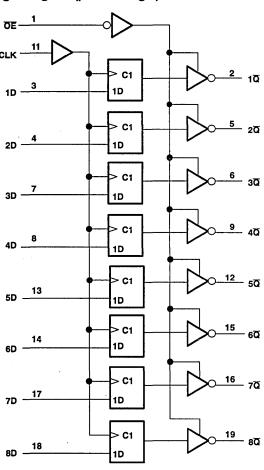
	INPUTS	OUTPUT	
ŌE	CLK	D	<u> </u>
L	1	Н	L
L	1	L	н
L	L	Х	ರ₀
Н	Х	Χ	z

# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)





D3773, FEBRUARY 1991-REVISED OCTOBER 1992

av	solute maximum ratings over operating	g nee-an temperature range (unless otherwise noted).
	Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
	Input voltage range, V <sub>I</sub> (see Note 1)	
	Voltage range applied to any output in the h	igh state or power-off state, V <sub>0</sub> 0.5 V to 5.5 V
	Current into any output in the low state, Io:	SN54ABT534 96 mA
		SN74ABT534 128 mA
	Input clamp current, $l_{ik}$ ( $V_i < 0$ )	–18 mA

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54A	BT534	SN74A	BT534	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	V <sub>CC</sub> Supply voltage				4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2		2		٧
V <sub>IL</sub>	Low-level input voltage					0.8	٧
Vi	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	loL Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

D3773, FEBRUARY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T	A = 25°0	>	SN54A	BT534	SN74ABT534		UNIT
PARAMETER	TEST CONDITION	15	MIN	TYP	MAX	MIN	MAX	MIN	. MAX	וואט
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		3			3		3		v
V <sub>OH</sub>			2			2				•
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
Vo	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			<b>&gt;</b>
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	· ·
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μА
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				50		-50		-50	μΑ
I <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$		·		±100				±100	μA
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
I <sub>O</sub> §	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-140	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high		1	250		250		250	μΑ
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0, \\ V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	V1 = V66 01 G112	Outputs disabled		0.5	250		250		250	μА
Δlcc¶	$V_{CC}$ = 5.5 V, One input at 3.4 V Other inputs at $V_{CC}$ or GND	',			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V									pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V									pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C MIN MAX		SN54ABT534		SN74ABT534		UNIT
					MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	· · · · · · · · · · · · · · · · · · ·		125		125		125	MHz
tw	Pulse duration	CLK high or low	3.5		3.5		3.5		ns
	Setup time, data before CLK†	High	1.6		1.6		1.6		
ī <sub>su</sub>	Setup time, data before CLN7	Low	2.2		2.2		2.2		ns
th	Hold time, data after CLK↑	High or low	1.8#		1.8#		1.8#		ns

<sup>#</sup> This data sheet limit may vary among suppliers.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT534, SN74ABT534 OCTAL EDGE-TRIGGERED D-TYPÉ FLIP-FLOPS WITH 3-STATE OUTPUTS D3773, FEBRUARY 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	то   ,		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT534		SN74ABT534	
	(INPOT)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125	175		125		125		MHz
t <sub>PLH</sub>	CLV	LK Q	2.6	5.1	5.9	2.6		2.6	6.7	
t <sub>PHL</sub>	OLK		3.4	6	6.7	3.4		3.4	7.6	ns
t <sub>PZH</sub>	ŌĒ	Q	1	3.3	4.2	1		1	5	
t <sub>PZL</sub>	OE .	<u>"</u>	2.6	5	5.8	2.6		2.6	6.8	ns
tpHZ	ŌE	Q	2.4	5.3	6.6	2.4		2.4	7.3	
t <sub>PLZ</sub>	OE.	"	2.3	5.1	5.8	2.3		2.3	6.5	ns



#### PARAMETER MEASUREMENT INFORMATION TEST S1 **500** Ω t<sub>PLH</sub>/t<sub>PHL</sub> Open From Output 7 V t<sub>PLZ</sub>/t<sub>PZL</sub> GND **Under Test** t<sub>PHZ</sub>/t<sub>PZH</sub> Open C<sub>L</sub> = 50 pF **500** Ω (see Note A) LOAD CIRCUIT FOR OUTPUTS 3 V Input 1.5 V 3 V 1.5 V **Timing Input** VOLTAGE WAVEFORMS **PULSE DURATION** 3 V **Data Input** 3 V 1.5 V 1.5 V Output 0 V Control 1.5 V (low-level **VOLTAGE WAVEFORMS** enabling) SETUP AND HOLD TIMES 3.5 V Output Waveform 1 Input V<sub>OL</sub> + 0.3 V 1.5 V S1 at 7 V VoL (see Note C) t<sub>PHZ</sub>→ **t**PLH Output VoH Waveform 2 VoH V<sub>OH</sub> -- 0.3 V

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

Output

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns.  $t_r \leq 2.5$  ns.

S1 at Open

VOLTAGE WAVEFORMS

**ENABLE AND DISABLE TIMES** 

~ 0 V

(see Note C)

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

VOL

D. The outputs are measured one at a time with one transition per measurement.

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES

Figure 1. Load Circuit and Voltage Waveforms

### SN54ABT540, SN74ABT540 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

D3774, FEBRUARY 1991-REVISED OCTOBER 1992

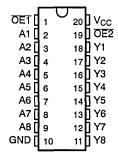
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

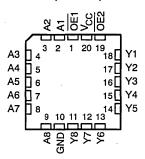
The 'ABT540 octal buffers and line drivers are ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package that facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all corresponding outputs are in the high-impedance state.

SN54ABT540 . . . J PACKAGE SN74ABT540 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT540 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT540 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT540 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT540 is characterized for operation from  $-40^{\circ}$ C to 85°C.

#### **FUNCTION TABLE**

	INPUTS	OUTPUT	
OE1	OE2	A	γ _
L	L	L	Н
L	L	Н	L
Н	Х	X	z
х	н	Х	z

EPIC-IIB is a trademark of Texas Instruments Incorporated.

Texas VI

# SN54ABT540, SN74ABT540 **OCTAL BUFFERS/DRIVERS** WITH 3-STATE OUTPUTS

logic symbol†

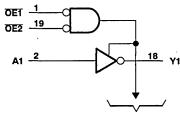
A6

Α7 9

**A8** 

#### ΕN OE2 2 18 **Y1** 3 17 **Y2** 4 16 **Y3 A3** 15 **Y4** A4 6 14 **Y5** 13 **Y6**

## logic diagram (positive logic)



To 7 Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

12 **Y**7

11

18

Supply voltage range, v <sub>CC</sub>		0.5 V to / V
Input voltage range, V <sub>1</sub> (see Note 1)		$\dots$ -0.5 V to 7 V
Voltage range applied to any output in the high state	e or power-off state, VO	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54A	ABT540	96 mA
SN74A	ABT540	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air	): DB package	0.5 W
	DW package	0.85 W
	N package	1.3 W
Storage temperature range		65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54A	BT540	SN74ABT540		LIAUT
			MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	:	2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	V <sub>CC</sub>	0	Vcc	V
l <sub>OH</sub>	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	ပဲ

NOTE 2: Unused or floating inputs must be held high or low.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54ABT540		SN74ABT540		UNIT	
PARAMETER	'5	SI CONDITION	45	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>l</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5			
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 mA		. 2			2				7 °
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$		2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA	= 48 mA			0.55		0.55			
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	, v
1 <sub>1</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or G	ND			±1		±1		±1	μА
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	50	-180	~50	-180	mA
	v ==v		Outputs high		1	250		250		250	μА
Icc	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	$I_{O}=0,$	Outputs low		24	30		30		30	mA
	11 - 400 or and		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data innuta	Outputs enabled			1.5		1.5		1.5	
ΔI <sub>CC</sub> ¶	One input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control inputs	Control inputs			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V				8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

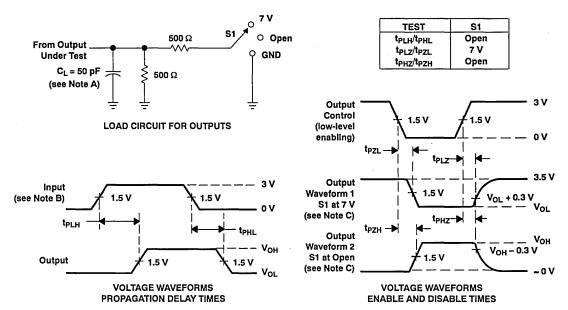
PARAMETER	FROM (INPUT)	TO (OUTPUT)	1 T. = 25°C		SN54A	BT540	SN74ABT540		UNIT		
	(INFO1)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	$\overline{\mathbf{x}}$	
t <sub>PLH</sub>	А		1	2.9	4.1	1		1	4.8		
t <sub>PHL</sub>		, T	1.6	3.1	4.3	1.6		1.6	4.8	ns	
t <sub>PZH</sub>	ŌĒ	V	1.2	3.4	4.9	1.2		1.2	5.9		
t <sub>PZL</sub>	. OE	l Y	. 1.2	3	4.4	1.2		1.2	5.1	ns	
t <sub>PHZ</sub>	117		3.1	5.3	6.5	3.1		3.1	7.3		
t <sub>PLZ</sub>	ŌĒ	Y	Y	2.5	4.4	5.7	2.5		2.5	6.2	ns

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_r \leq 2.5 \text{ ns}$ ,
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCBS093B-D3704, JANUARY 1991-REVISED OCTOBER 1992

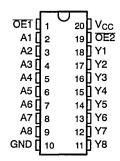
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

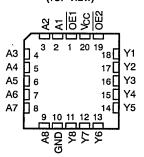
The 'ABT541 octal buffer and line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OET or OE2) input is high, all eight outputs are in the high-impedance state.

SN54ABT541 . . . J PACKAGE SN74ABT541 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT541 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT541 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT541 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

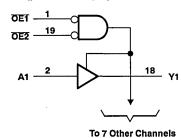
	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н ,
н	X	X	z
X	Н	X	z

EPIC-IIB is a trademark of Texas Instruments Incorporated.

#### logic symbol†

#### **OET** ΕN 19 OE2 18 A1 Y1 3 17 A2 **Y2** 16 **Y3** A3 5 15 A4 **Y4** 6 14 **Y5 A5** 13 **Y6** Α6 8 12 Α7 **Y7** 11 9 **8**A **Y8**

## logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		0.5 V to 7 V
	high state or power-off state, VO	
Current into any output in the low state, Io:	SN54ABT541	96 mA
	SN74ABT541	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		–18 mA
Output clamp current, IOK (VO < 0)		–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (	in still air): DB package	0.5 W
	DW package	0.85 W
	N package	1.3 W
Storage temperature range		65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

		SN54ABT541	SN74ABT5	41
		MIN MAX	MIN M	AX UNIT
Vcc	Supply voltage	4.5 5.	4.5	5.5 V
V <sub>IH</sub>	High-level input voltage	2 🔊	2	V
V <sub>IL</sub>	Low-level input voltage	્ર€ 0.8	3 (	).8 V
VI	Input voltage	0 V <sub>CC</sub>	; 0 V	cc V
Гон	High-level output current	-24	-	32 mA
loL	Low-level output current	े ४।	3	64 mA
Δt/Δν	Input transition rise or fall rate	Ž* .	5	5 ns/V
T <sub>A</sub>	Operating free-air temperature	∸55 125	-40	85 °C

NOTE 2: Unused or floating inputs must be held high or low.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS		7	A = 25°C	;	SN54ABT541		SN74ABT541			
PARAMETER	TEST CONDITION	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5			
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3		v	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		2			2					
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2			
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			0.55 V	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>		15		0.55		
lı	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		, ±1		±1	μΑ	
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50	j	<b>€</b> 50		50	μΑ	
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		~ -50		-50	μΑ	
I <sub>OFF</sub>	$V_{CC} = 0 \text{ V}, \qquad V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100	35			±100	μΑ	
I <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ	
l <sub>O</sub> §	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-140	-180	҈ −50	-180	-50	-180	mA	
	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0,	Outputs high		5	250		250		250	μΑ	
Icc	$V_{\rm CC} = 3.3 \text{ V},  I_{\rm O} = 0,$ $V_{\rm I} = V_{\rm CC} \text{ or GND}$	Outputs low		22	30		30		30	mA	
	1, 166 1 2112	Outputs disabled		1	250		250		250	μA	
	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,	Outputs enabled			1.5		1.5		1.5	mA	
ΔI <sub>CC</sub> ¶	Other inputs at $V_{CC}$ or GND	Outputs disabled			50		50		50	μΑ	
	-	Control inputs			1.5		1.5		1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			5		L				pF	
Co	V <sub>O</sub> = 2.5 V or 0.5 V			5					Ţ	pF	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

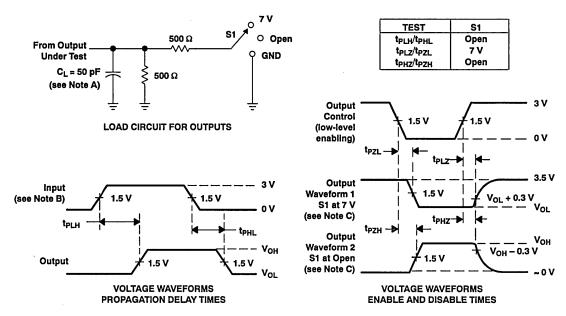
PARAMETER	FROM (INPUT)	TO (OUTPUT)	i i	CC = 5 V A = 25°C		SN54A	BT541	SN74A	BT541	UNIT
	( 0.)	(55.1.51)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	^	V	1	2.6	4.1	1	<b>474.6</b>	1	4.6	ns
t <sub>PHL</sub>	1 ^	ľ	1	2.9	4.2	1,4	₹ 4.7	1	4.6	118
t <sub>PZH</sub>	OE .		1.1	3.1	4.8	1,(1)	5.4	1.1	5.3	ns
t <sub>PZL</sub>		, T	2.1	4.4	5.9	21	6.5	2.1	6.4	115
t <sub>PHZ</sub>	OE Y		2.1	5.1	6.6	్ల≈2.1	7.1	2.1	7.1	ns
t <sub>PLZ</sub>		1.7	4.7	6.2	1.7	6.7	1.7	6.7	113	

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \le 2.5$  ns,  $t_r \le 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT543, SN74ABT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3662, JANUARY 1991-REVISED OCTOBER 1992

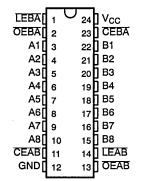
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

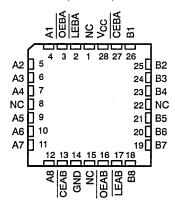
The 'ABT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

SN54ABT543...JT PACKAGE SN74ABT543...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT543...FK PACKAGE (TOP VIEW)



NC - No internal connection

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT543 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT543 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT543 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

# SN54ABT543, SN74ABT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

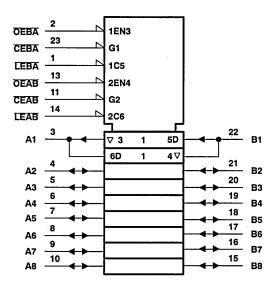
D3662, JANUARY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPL	OUTPUT		
CEAB	LEAB	Α	В	
Н	Х	Х	X	Z
х	X	H,	×	z
L	Н	L	×	B₀‡
L	L	L	L	L
L	L	L	Н	н

<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

# logic symbol§

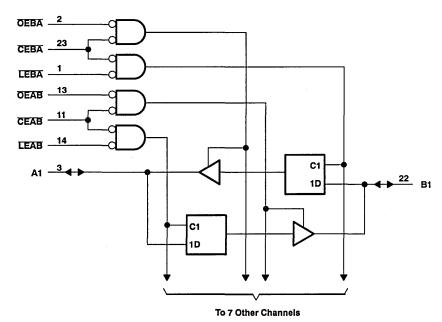


<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

D3662, JANUARY 1991-REVISED OCTOBER 1992

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note	1)	0.5 V to 7 V
Voltage range applied to any output in the high state	or power-off state, V <sub>0</sub>	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54A	BT543	
SN74A	BT543	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	: DB package	0.5 W
	DW package	1 W
	NT package	1.3 W
Storage temperature range		-65°C to 150°C

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# **SN54ABT543, SN74ABT543** OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS D3662, JANUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54A	BT543	SN74ABT543		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	,S"	2		V
V <sub>IL</sub>	Low-level input voltage			€ 0.8		0.8	٧
Vį	Input voltage		g.	<sup>™</sup> V <sub>CC</sub>	0	Vcc	٧
Гон	High-level output current	-	Š	-24		-32	mA
loL	Low-level output current		JO'	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	5		5	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	ô

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			10	Т	A = 25°C	;	SN54A	BT543	SN74A	BT543	
PARAMETER	• "	EST CONDITION	15	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>l</sub> =18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = −3 mA		2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	1 <sub>OH</sub> = -3 mA		3			3		3		l v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				\
	V <sub>CC</sub> = 4.5 V,			2‡					2		
	V <sub>CC</sub> = 4.5 V,					0.55	1	0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡	i	16.		0.55	
,	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		्र्र्थन		±1	
lı lı	$V_I = V_{CC}$ or GND A or B ports		_		±100		<u>4</u> 100		±100	μΑ	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			-	50	,	<b>50</b>		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	ï			-50	Ç	-50		50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	٧			±100	ŞŸ			±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Æ	50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	100	-180	~-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μΑ
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low		24	34#		34#		34#	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.5	250		250		250	μА
"	V <sub>CC</sub> = 5.5 V, One ir	put at 3.4 V,	•			4.5		4.5		4.5	
Δlccll	Other inputs at V <sub>CC</sub> or GND				1.5		1.5	Į	1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs			4				İ		pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		7						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This data sheet limit may vary among suppliers.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT543		SN74ABT543		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	1
t <sub>w</sub>	Pulse duration, LEA	B or LEBA low		3.5		3.5		3.5		ns
	Data before	High	3.5		3.5,	<del>ب</del>	3.5			
	Setup time	<b>LEAB</b> or <b>LEBA</b> ↑	Low	3		<u> </u>	Gi	3		
t <sub>su</sub>	Setup time	Data before	High	3.5		3.5	2	3.5		ns
		CEAB or CEBA†	Low	3		Q 30		3		
	Hald time	Data after LEAB or LE		1†		1†		1†		
th	h Hold time	Data after CEAB or CE	BA↑	1 <sup>†</sup>		1 <sup>†</sup>		1†		ns

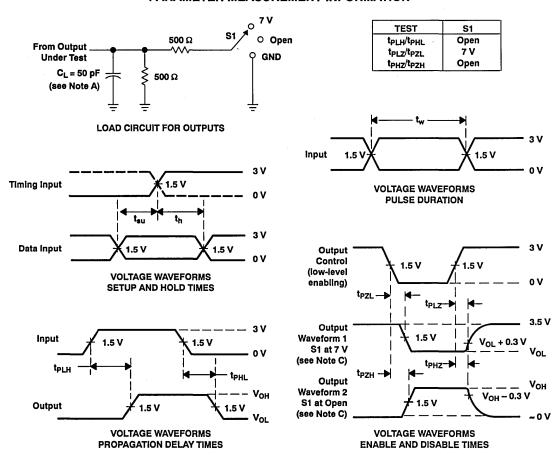
# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT543		SN74ABT543		
	( 5.)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A or B	B or A	1.9	4.4	5.9	1.9		1.9	6.9	ns	
t <sub>PHL</sub>	AUD	BUIA	1.9	4.4	5.9	1.9	4	1.9	6.9	115	
t <sub>PLH</sub>	LEBA or LEAB	A or B	1.6	4.1	5.6	1.6		1.6	6.6	ns	
t <sub>PHL</sub>	LEBA OI LEAD	AUID	2.1	4.6	6.1	2.1	84	2.1	7.1	IIS	
t <sub>PZH</sub>	OEBA or OEAB	A or B	1.4	3.9	5.4	1.4	₹	1.4	6.4	ns	
t <sub>PZL</sub>	OEDA OI OEAB		2.5	5	6.5	2.5		2.5	7.5	115	
t <sub>PHZ</sub>	OEBA or OEAB	A or B	2.5 <sup>†</sup>	5.9	7.4	2.5 <sup>†</sup>		2.5 <sup>†</sup>	8.4	ns	
t <sub>PLZ</sub>	OEBA OI OEAB	AOIB	3	5.5	7	<i>5</i> ₹ 3		3	8	115	
t <sub>PZH</sub>	CERA or CEAR	A or B	1.4	3.9	5.4	1.4		1.4	6.4	ns	
t <sub>PZL</sub>	CEBA or CEAB	A or B	2.5	5	6.5	2.5		2.5	7.5		
t <sub>PHZ</sub>	CEBA or CEAB	A or B	3.2 <sup>†</sup>	5.9	7.4	3.2 <sup>†</sup>		3.2 <sup>†</sup>	8.4		
t <sub>PLZ</sub>	CEDA UI CEAB		3	5.5	7	3		3	8	ns	

<sup>†</sup> This data sheet limit may vary among suppliers.

D3662, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT544, SN74ABT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3775, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

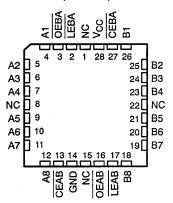
The 'ABT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

SN54ABT544 . . . JT PACKAGE SN74ABT544 . . . DB, DW, OR NT PACKAGE (TOP VIEW)

LEBA [	1	U	24	] v <sub>cc</sub>
OEBA [			23	CEBA
A1 [			22	] B1
A2 [			21	] B2
. A3 [			20	] B3
A4 [			19	] B4
A5 [			18	] B5
A6 [			17	] B6
A7 [			16	B7
A8 [	10		15	] B8
CEAB [	11		14	LEAB
GND [	12		13	OEAB

SN54ABT544...FK PACKAGE (TOP VIEW)



NC-No internal connection

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT544 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in Iess than half the printed-circuit-board area.

The SN54ABT544 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT544 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



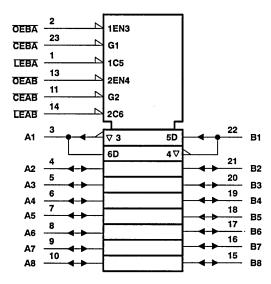
# SN54ABT544, SN74ABT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS D3775, FEBRUARY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPL	JTS		OUTPUT
CEAB	LEAB	OEAB ·	Α	В
Н	X	Х	Х	Z
L	X	Н	Х	z
L	н	L	Х	B <sub>0</sub> ‡
L	L	L	L	н
L	L	L	Н	L

<sup>&</sup>lt;sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

# logic symbol§

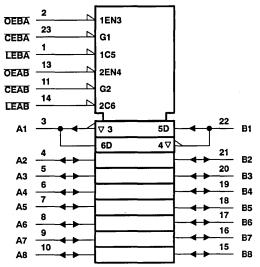


<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

D3775, FEBRUARY 1991-REVISED OCTOBER 1992

### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, VI (except I/O ports) (se	ee Note 1)	
Voltage range applied to any output in the h		
Current into any output in the low state, Io:	SN54ABT544	96 mA
	SN74ABT544	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–18 mA
Output clamp current, IOK (VO < 0)		–50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (ir	n still air): DB package	0.5 W
	DW package	
	NT package	
Storage temperature range		

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



# SN54ABT544, SN74ABT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3775, FEBRUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54A	BT544	SN74A	BT544	11117
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	٧
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		CT COMPLETION		T	A = 25°C		SN54A	BT544	SN74AI	BT544	UNIT
PARAMETER	15	ST CONDITION	5	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V <sub>i</sub>	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
VoH	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		v
∨он	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				·
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$		2 <sup>‡</sup>					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	· ·
1	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА
-	$V_I = V_{CC}$ or GND		A or B ports			±100		±100		±100	μΛ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$				50		50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	<b>\</b>			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	T	Outputs high		1	250		250		250	μΑ
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low		24	34#		34#		34#	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	i	Outputs disabled		0.5	250		250		250	μА
AT II	V <sub>CC</sub> = 5.5 V, One in	put at 3.4 V,	•			4 5		1.5		1.5	m A
Δlcc <sup>ll</sup>	Other inputs at V <sub>CC</sub> or GND					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs				4						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

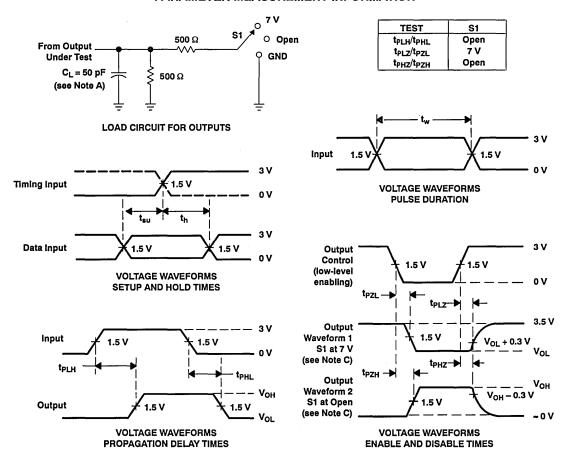
 $<sup>\</sup>slash\hspace{-0.6em}^{\#}$  This data sheet limit may vary among suppliers.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT544, SN74ABT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3775, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT573, SN74ABT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

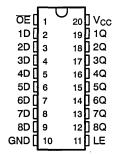
D3663, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

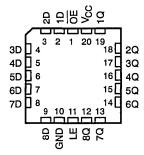
#### description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT573...J PACKAGE SN74ABT573...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT573...FK PACKAGE (TOP VIEW)



The eight latches of the 'ABT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT573 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT573 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT573 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

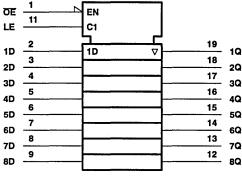
# SN54ABT573, SN74ABT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3663, JANUARY 1991-REVISED OCTOBER 1992

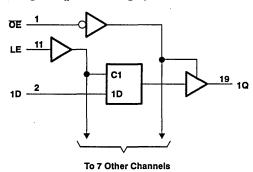
# FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
ŌĒ	LE	D	a
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q <sub>0</sub>
Н	X	X	Z

### logic symbol†



### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		
Voltage range applied to any output in the high	state or power-off state, Vo .	0.5 V to 5.5 V
Current into any output in the low state, Io: Si	N54ABT573	96 mA
SI	N74ABT573	128 mA
Input clamp current, $I_{IK}(V_I < 0)$		–18 mA
Output clamp current, IOK (VO < 0)	·	–50 mA
Maximum power dissipation at TA = 55°C (in st	ill air): DB package	0.5 W
	DW package	0.85 W
	N package	1.3 W
Storage temperature range		-65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# **SN54ABT573, SN74ABT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS**

D3663, JANUARY 1991-REVISED OCTOBER 1992

## recommended operating conditions (see Note 2)

			SN54A	BT573	SN74A	BT573	UNIT
i			MIN	MAX	MIN	MAX	וואט
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
IOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			A = 25°C	;	SN54A	BT573	SN74A	UNIT	
PARAMETER	TEST CONDITION	N5	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},  I_{I} = -18 \text{ mA}$				-1.2	_	-1.2		-1.2	٧
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3		l v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		- 2			2				*
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v
$V_{OL}$	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	l v
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μА
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
lozL	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
l <sub>O</sub> ∮	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	v 55V 1 0	Outputs high		1	250		250		250	μА
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	AL ACC OF CIVED	Outputs disabled		0.5	250		250		250	μA
Δlcc	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V			6		i				pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
 This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# **SN54ABT573, SN74ABT573 OCTAL TRANSPARENT D-TYPE LATCHES** WITH 3-STATE OUTPUTS D3663, JANUARY 1991-REVISED OCTOBER 1992

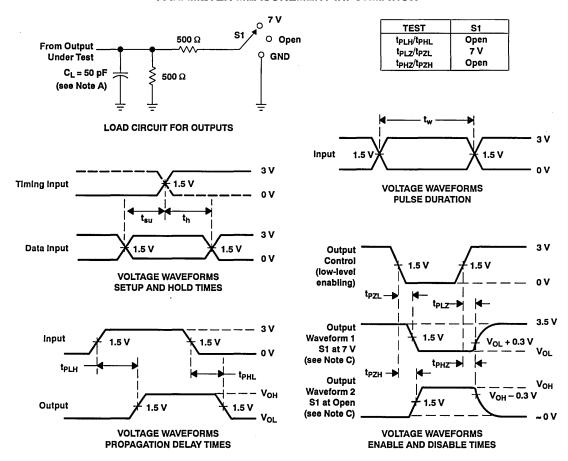
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		,	V <sub>CC</sub> =	: 5 V, 25°C	SN54ABT573		SN74ABT573		UNIT
			MIN MAX		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high		3.3		3.3		3.3		ns
	Columbian data before LEI	High	1.9		2.5		1.9		
t <sub>su</sub>	Setup time, data before LE↓	Low	1.5		2.5		1.5		ns
t <sub>h</sub>	Hold time, data after LE↓		1		2.5		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		то (оитрит)	TO T		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT573		SN74ABT573	
		(001101)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	1.9	3.2	5.4	1.4	6.4	1.9	5.9	ns
t <sub>PHL</sub>		ď	2.2	4.2	5.7	1.6	6.7	2.2	6.2	""
t <sub>PLH</sub>	LE	Q	2.2	4	6.1	2	7.1	2.2	6.6	ns
t <sub>PHL</sub>	LL	"	3.2	5.2	6.7	2.8	7.5	3.2	7.2	] ""
tpzH	ŌĒ	Q	1.2	3.2	4.7	0.8	6.2	1.2	5.2	
t <sub>PZL</sub>	OE	4	2.7	4.7	6.2	2	7.2	2.7	6.7	ns
t <sub>PHZ</sub>	ŌĒ	E Q	2.5	4.9	6.4	2.2	7.7	2.5	6.9	
t <sub>PLZ</sub>	OE		2	4.2	6	1.4	7	2	6.5	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT574, SN74ABT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPLITS

D3705, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB)
   Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art *EPIC-IIB* ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

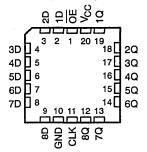
#### description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT574...J PACKAGE SN74ABT574...DB, DW, OR N PACKAGE (TOP VIEW)

ᅊ	1 U	20 1	
1D 🛛	2	19]]	Q
	3	18 🛭 2	Q.
3D [	4	17 🛚 3	3Q
4D [	5	16]] 4	IQ.
5D []	6	15 ]] {	SQ.
6D 🛛	7	14]] 6	SQ.
- 4	8	13] 7	'Q
4	9	12]] 8	3Q
GND [	10	11 🛛 (	CLK

SN54ABT574...FK PACKAGE (TOP VIEW)



The eight flip-flops of the 'ABT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT574 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT574 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT574 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

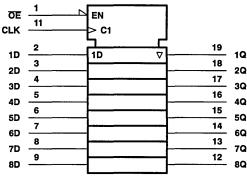
D3705, JANUARY 1991-REVISED OCTOBER 1992

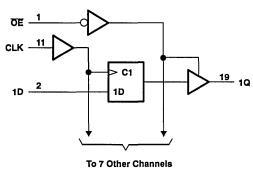
# FUNCTION TABLE (each flip-flop)

(										
	INPUTS		OUTPUT							
ŌĒ	CLK	D	a							
L	Ť	н	Н							
L	<b>†</b>	L	L							
L	L	X	Q <sub>0</sub>							
Н	Х	Х	Z							

## logic symbol†

# logic diagram (positive logic)





## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the h	high state or power-off state, V <sub>0</sub>	o –0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT574	96 mA
	SN74ABT574	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		—18 mA
Output clamp current, $I_{OK}(V_O < 0)$		–50 mA
Maximum power dissipation at $T_A = 55$ °C (i	in still air): DB package	0.5 W
	DW package	0.85 W
	N package	1.3 W
Storage temperature range		65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT574, SN74ABT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3705, JANUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54A	BT574	SN74A	BT574	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	H High-level input voltage		2		2		>
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	٧
V <sub>I</sub>	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current		T	-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature	-	-55	125	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54A	BT574	SN74ABT574			
PARAMETER	TEST CONDITIO	NS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5			
VoH	$V_{CC} = 5 \text{ V},  I_{OH} = -3 \text{ mA}$		3			3		3		<sub>v</sub>	
VOH	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$		2			2				٧	
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2			
Vai	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v	
,V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	V	
t <sub>l</sub>	$V_{CC} = 5.5 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μА	
lozн	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μΑ	
l <sub>OZL</sub>	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ	
IOFF	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА	
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA	
	V 55V 1 0	Outputs high		1	250	·	250		250	μА	
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA	
	11-166 et alta	Outputs disabled		0.5	250		250		250	μА	
Δlcc <sup>¶§</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,				1.5		1.5		1.5	mA	
	Other inputs at V <sub>CC</sub> or GND										
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF	
Co	V <sub>O</sub> = 2.5 V or 0.5 V			. 8						pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# **SN54ABT574, SN74ABT574** OCTAL EDGÉ-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS D3705, JANUARY 1991—REVISED OCTOBER 1992

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT574		SN74ABT574		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			150		150		150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
	Setup time, data before CLK†	High	1		1.5		1		ns
t <sub>su</sub>		Low	1.5		2		1.5		
th	Hold time, data after CLK†	High or low	1.5 <sup>†</sup>		2		1.5 <sup>†</sup>		ns

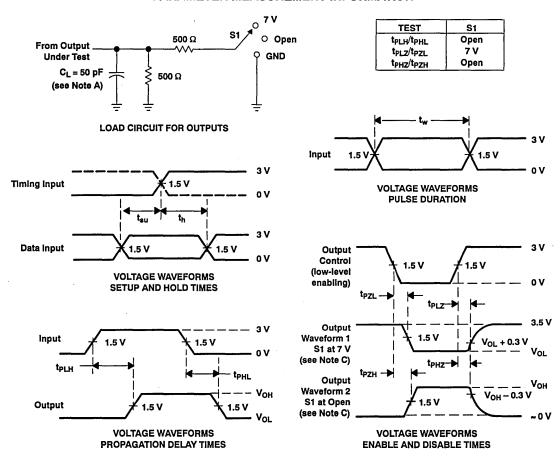
<sup>&</sup>lt;sup>†</sup> This data sheet limit may vary among suppliers.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	RAMETER FROM (INPUT)	то (ОИТРИТ)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT574	SN74A	UNIT		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>			150	200		150		150		MHz	
t <sub>PLH</sub>	CLK	CLK	Q	2.2	3.9	6.2	2.2	7	2.2	6.8	ns
t <sub>PHL</sub>	OLK	"	3	4.8	6.6	3	7.4	3	7.1	113	
t <sub>PZH</sub>	OE .	Q	1	3.3	4.3	1	6	1	5.1		
t <sub>PZL</sub>	OE	<b>"</b>	2.5	4.7	5.9	2.5	6.8	2.5	6.7	ns	
t <sub>PHZ</sub>	Œ	705	2.4	4.9	6.2	2.4	7.3	2.4	7		
t <sub>PLZ</sub>		q	2	4	5.8	2	6.9	2	6.5	ns	

D3705, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns.}$   $t_r \leq 2.5 \text{ ns.}$
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS113A-D3776, FEBRUARY 1991-REVISED OCTOBER 1992

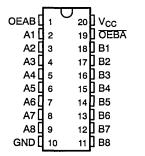
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

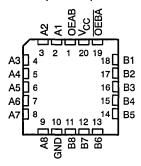
The 'ABT620 bus transceiver is designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'ABT620 provides inverted data at its outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

SN54ABT620...J PACKAGE SN74ABT620...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT620 . . . FK PACKAGE (TOP VIEW)



The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and OEBA. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. In this way, each output reinforces its input in this configuration.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT620 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT620 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT620 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

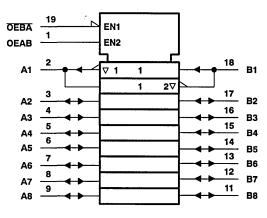
Texas **V** Instruments

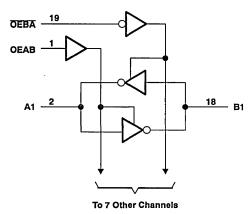
#### **FUNCTION TABLE**

INP	UTS	OPERATION
OEBA	OEAB	OPERATION
L	L	B data to A bus
L	н	B data to A bus, 不 data to B bus
н	L	Isolation
н	Н	A data to B bus

# logic symbol†

### logic diagram (positive logic)





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	. $-0.5V$ to $7V$
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	. $-0.5 V to 7 V$
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT620	96 mA
SN74ABT620	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	0.85 W
N package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

			SN54ABT620		SN74A	UNIT		
			MIN	MAX	MIN	MAX	ONII	
V <sub>CC</sub>	Supply voltage		4.5	5,5	4.5	5.5	V	
V <sub>IH</sub>	High-level input voltage			4	2		V	
VIL	Low-level input voltage			<i>\$</i> 0.8		8.0	V	
Vı	Input voltage		Q.4	∛ V <sub>CC</sub>	0	Vcc	V	
loн	High-level output current		Q.	-24		-32	mA	
loL	Low-level output current		Ş	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.Y	5		5	ns/V	
TA	Operating free-air temperature		_55	125	-40	85	°Ç	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT620		SN74ABT620		UNIT	
PARAMETER				MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	I	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>i</sub> = -18 mA				-1.2		-1.2		-1.2	V	
V <sub>ОН</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5			2.5		2.5		V	
	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3			
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2					
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					. 2			
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 48 \text{ mA}$					0.55		0.55			V	
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA			0.55‡				0.55	L_ <b>`</b>		
1	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	1 μA	
	$V_I = V_{CC}$ or GND		A or B ports			±100		±100		±100	μΛ	
l <sub>ozh</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$				50		<i>(ii)</i> 50		50	μΑ	
l <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$					-50		₹ –50		-50	μΑ	
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V}, \qquad V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100	Ţ,Ĉ			±100	μA		
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Š	50		50	μА	
lo¶	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 \text{ V}$		-50	-100	-180	్ల¥50	-180	-50	-180	mA	
lcc	V <sub>CC</sub> = 5.5 V,	A or B ports	Outputs high		5	250		250		250	μА	
	l <sub>O</sub> = 0,		Outputs low		24	30		30		30	mA	
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.5	250		250		250	μΑ	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V,	Data inputs	Outputs enabled			1.5		1.5		1.5	mA	
	One input at 3.4 V, Other inputs at		Outputs disabled			0.05		0.05		0.05		
	V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		7						рF	

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS113A-D3776, FEBRUARY 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	1	<sub>CC</sub> = 5 V, <sub>A</sub> = 25°C	SN54ABT620		SN74ABT620		UNIT
<u> </u>			MIN	TYP MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	4.1	1		1	4.8	ns
t <sub>PHL</sub>			1	4.3	1	4.	1	4.8	
t <sub>PZH</sub>	OEBA	А	1.3	4.6	1.3	19	1.3	5.5	ns
t <sub>PZL</sub>			1	6.1	1	<i>,</i>	1	7.1	
t <sub>PHZ</sub>	OEBA	Α	2	6.3	2,4	5,	2	7	ns
t <sub>PLZ</sub>	OEBA		1.4	5.4	1,4)		1.4	5.8	
t <sub>PZH</sub>	OEAB	В	1.6	6.2	Д),6		1.6	6.8	ns
t <sub>PZL</sub>	CEAD		2	5.9	Ç₹ 2		2	6.4	
t <sub>PHZ</sub>	OEAB	В	1.2	5.6	1.2		1.2	6.5	ns
t <sub>PLZ</sub>	OEAD		1.1	4.7	1.1		1.1	5.6	

#### PARAMETER MEASUREMENT INFORMATION TEST S1 500 $\Omega$ O Open Open t<sub>PLH</sub>/t<sub>PHL</sub> From Output tplz/tpzL 7 V **Under Test** GND t<sub>PHZ</sub>/t<sub>PZH</sub> Open C<sub>L</sub> = 50 pF **500** Ω (see Note A) 3 V Output Control 1.5 V LOAD CIRCUIT FOR OUTPUTS (low-level enabling) 3.5 V Output Input Waveform 1 V<sub>OL</sub> + 0.3 V (see Note B) 1.5 V S1 at 7 V VOL (see Note C) t<sub>PHZ</sub>-▶ **t**PLH tpzH t<sub>PHL</sub> Output $v_{oh}$ Waveform 2 - V<sub>OH</sub> V<sub>OH</sub> - 0.3 V S1 at Open Output 1.5 V (see Note C) ~ 0 V **VOLTAGE WAVEFORMS** VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES**

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{<}$  10 MHz,  $Z_{0}$  = 50  $\Omega$ ,  $t_{r}$   $_{<}$  2.5 ns,  $t_{r}$   $_{<}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS114A-D3777, FEBRUARY 1991-REVISED OCTOBER 1992

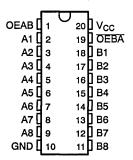
- Space-Saving Package Option: Shrink Small-Outline Package (DB)
   Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

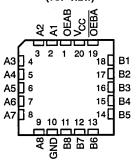
The 'ABT623 bus transceiver is designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'ABT623 provides true data at its outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

SN54ABT623...J PACKAGE SN74ABT623...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT623...FK PACKAGE (TOP VIEW)



The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and OEBA. Each output reinforces its input in this configuration. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT623 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT623 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT623 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

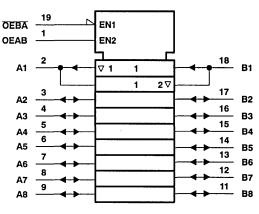
SCBS114A-D3777, FEBRUARY 1991-REVISED OCTOBER 1992

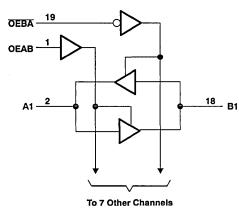
#### **FUNCTION TABLE**

INP	UTS	OPERATION
OEBA	OEAB	OPERATION
L	L	B data to A bus
L	н	B data to A bus, A data to B bus
н	L	Isolation
н	Н	A data to B bus

### logic symbol<sup>†</sup>

### logic diagram (positive logic)





#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		. −0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note	1)	0.5 V to 7 V
Voltage range applied to any output in the high state	or power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54A	ιBT623	96 mA
SN74A	ABT623	128 mA
Input clamp current, $I_{IK}(V_I < 0)$		–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air)	): DB package	0.5 W
	DW package	0.85 W
	N package	1.3 W
Storage temperature range		-65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### recommended operating conditions (see Note 2)

			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5,5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2	Q	2		V
VIL	Low-level input voltage		<i>₹</i> 7 0.8		0.8	V	
Vı	Input voltage		Ó.	₹ V <sub>CC</sub>	0	Vcc	V
Іон	High-level output current		(ن).	-24		-32	mA
loL	Low-level output current		1.8	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	ζ.,	5		5	ns/V
TA	Operating free-air temperature		≪ –55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CT COMPLETION	16	Т	<sub>A</sub> = 25°C	;	SN54A	BT623	SN74ABT623		UNIT
PARAMETER	15	ST CONDITION	15	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>j</sub> = –18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	2.5			2.5		2.5				
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$		2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,			0.55		0.55			v		
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,				±1		#		±1	μА	
'1	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΛ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		<i>∰</i> 50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	- 2	<sup>2</sup> –50		-50	μΑ
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100	Ţ,			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Ż	50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	<i>ু</i> ≆50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		5	250	*	250		250	μΑ
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		22	30		30		30	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		1	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,		Outputs enabled			1.5		1.5		1.5	
Δl <sub>CC</sub> #	One input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND Control inputs					1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	•		4						pF	
Cio	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		A or B ports		7						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

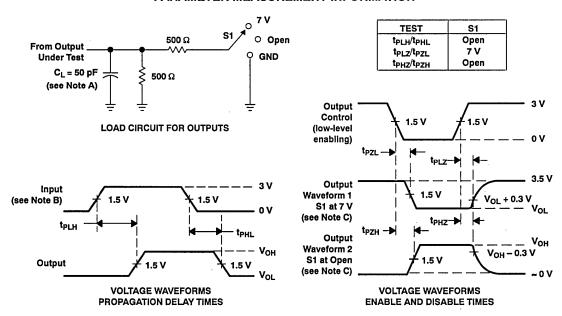
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	i .	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT623		SN74ABT623	
	( 0.7		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	2.6	4.1	1	4.6	1	4.6	ns
t <sub>PHL</sub>	AUID	BUIA	1	2.6	4.2	1	4.6	1	4.6	115
t <sub>PZH</sub>	OEBA	Α	1.7	3.4	6.5	1.7	<b>.</b> \$7₹5	1.7	7.5	ns
t <sub>PZL</sub>	OEBA	^	1.7	3.8	6.5	1.7	7.5ري/	1.7	7.5	113
t <sub>PHZ</sub>	OEBA	Α	1.7	4.2	6.5	1.7,4		1.7	7.5	ns
t <sub>PLZ</sub>	OEBA	^	1.7	4.7	6.5	1,70	7.5	1.7	7.5	115
t <sub>PZH</sub>	OEAB	В	1.7	4.8	6.5	4)7	7.5	1.7	7.5	ne
tpzL	OEAB	В	1.7	4	6.5	Q-1.7	7.5	1.7	7.5	ns
t <sub>PHZ</sub>	OEAB	_	1.7	3.9	6.5	1.7	7.5	1.7	7.5	ns
t <sub>PLZ</sub>	UEAB	В	1.7	3.2	6.5	1.7	7.5	1.7	7.5	

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



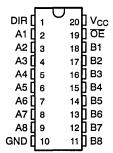
SCBS104A-D3778, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>Δ</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

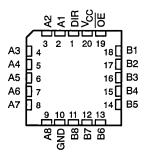
#### description

The 'ABT640 bus transceiver is designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

SN54ABT640 . . . J PACKAGE SN74ABT640 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT640...FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT640 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT640 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT640 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### **FUNCTION TABLE**

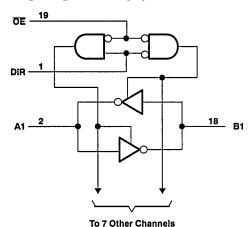
INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L.	L	B data to A bus
L	н	A data to B bus
Н	Х	Isolation

EPIC-IIB is a trademark of Texas Instruments Incorporated.

#### logic symbol<sup>†</sup>

#### ŌΕ G3 3 EN1 [BA] 3 EN2 [AB] 1 2♡ 17 **B2** 16 15 **B4** 14 **A5 B**5 13 **B6** A6 12 8 **B7 A7 A8 B8**

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (s	see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the h	high state or power-off state, $V_{O}$	$\dots$ -0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT640	96 mA
	SN74ABT640	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)		–18 mA
Output clamp current, IOK (VO < 0)		– 50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (i	in still air): DB package	0.5 W
	DW package	0.85 W
	N package	1.3 W
Storage temperature range		65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54A	BT640	SN74A	BT640	UNIT
			MIN	MAX	MIN	MAX	UNII
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2	49	2		V
V <sub>IL</sub>	Low-level input voltage		<i>/</i> 4/ 0.8		0.8	V	
Vı	Input voltage		g<	₹ V <sub>CC</sub>	0	Vcc	V
Іон	High-level output current		<u>(j.</u>	-24		-32	mA
loL	Low-level output current		Ş	48	l	64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	ŞĞ,	5		5	ns/V
TA	Operating free-air temperature		_55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			A = 25°C	;	SN54A	BT640	SN74ABT640		
PARAMETER	'5	SI CONDITION	3	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = 18 mA			-1.2		-1.2	j	-1.2	V	
	V <sub>CC</sub> = 4.5 V,	2.5			2.5		2.5				
V	V <sub>CC</sub> = 5 V,	3			3		3		v		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	4.5 V, I <sub>OH</sub> = -24 mA					2				· ·
	V <sub>CC</sub> = 4.5 V,	<sub>C</sub> = 4.5 V, I <sub>OH</sub> = -32 mA							2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>OL</sub> = 48 mA			0.55		0.55			V	
VOL	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	· •
1.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		<b>#1</b> .		±1	
lı lı	$V_i = V_{CC}$ or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	V <sub>O</sub> = 2.7 V			50		<i>‰</i> 50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 \	/			±100	Ş			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Q	50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	<i>≪</i> ≚50	-180	50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		5	250	*	250		250	μА
lcc	I <sub>O</sub> = 0,	A or B ports	Outputs low		24	30		30		30	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data in auto	Outputs enabled			1.5		1.5		1.5	
Δl <sub>CC</sub> #	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  Data inputs  Control inputs		Outputs disabled			0.05		0.05		0.05	mA
						1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			4						pF	
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		A or B ports		7						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT640	SN74A	UNIT	
	(1111-01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	}
t <sub>PLH</sub>	A or B	B or A	1	2.7	4.2	1	, 5	1	4.9	ns
t <sub>PHL</sub>	AOIB	BOIA	1.5	2.7	4.3	1.5	<u>بي</u> 5	1.5	4.9	
t <sub>PZH</sub>	OE	A or B	1.5	3.7	4.9	1.5	<b>√</b> 5.9	1.5	5.8	no
t <sub>PZL</sub>	OE	AOIB	1.3	· 5	5.9	ং (১	7.4	1.3	7.3	ns
t <sub>PHZ</sub>	ŌĒ	A or B	2.5	4.1	6.5	2.5	6.9	2.5	6.8	ns
t <sub>PLZ</sub>	<u> </u>	7016	2	3.3	5.3	2	5.6	2	5.5	

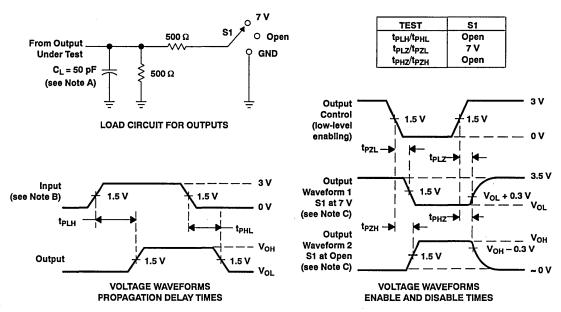
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>mbox{\$}$  The parameters  $\mbox{I}_{\mbox{\scriptsize OZH}}$  and  $\mbox{I}_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \le 2.5$  ns,  $t_r \le 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54ABT646, SN74ABT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS068B-D3659, JULY 1991-REVISED OCTOBER 1992

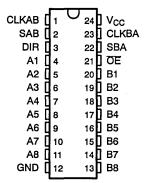
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

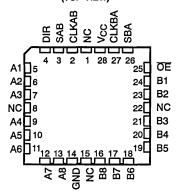
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

SN54ABT646...JT PACKAGE SN74ABT646...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT646...FK PACKAGE (TOP VIEW)



NC - No internal connection

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT646 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT646 is characterized for operation from  $-40^{\circ}$ C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



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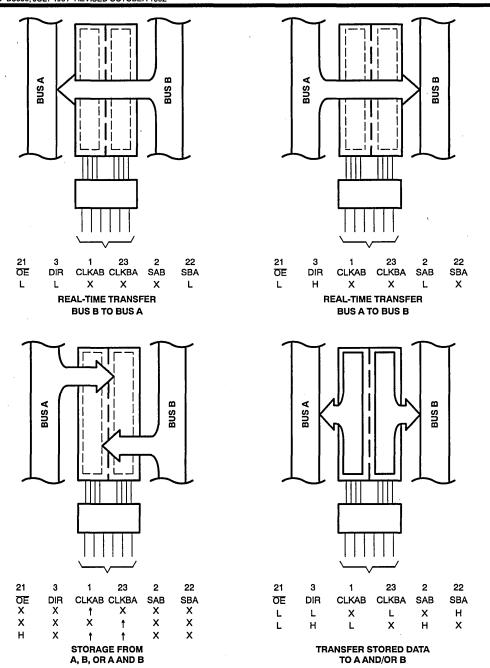


Figure 1. Bus-Management Functions

Pin numbers shown are for DB, DW, JT, and NT packages.



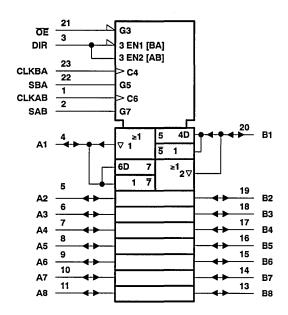
### **SN54ABT646, SN74ABT646 OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS068B-D3659, JULY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLE**

		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION		
ŌE	OE DIR CLKAB CLKBA		SAB SBA		A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION			
Х	×	t	X	Х	X	Input	Unspecified <sup>†</sup>	Store A, B unspecified <sup>†</sup>		
X	Х	X	<b>†</b>	Х	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>		
Н	Х	1	1	Х	Х	input	Input	Store A and B data		
Н	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage		
L	L	Х	Х	Х	, L	Output	Input	Real-time B data to A bus		
L	L	X	L	X	н	Output	Input	Stored B data to A bus		
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus		
L	Н	L	Х	н	Х	Input	Output	Stored A data to B bus		

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

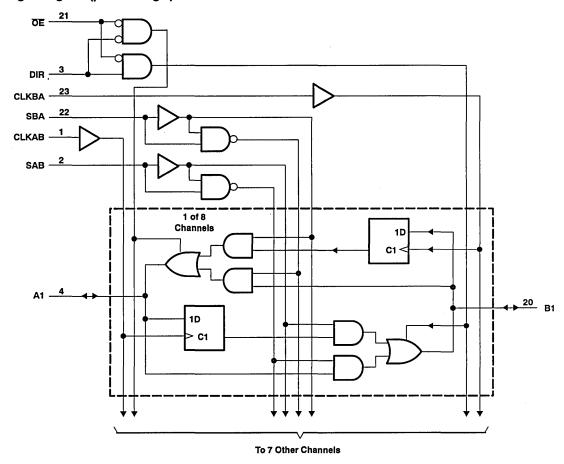
#### logic symbol‡



<sup>&</sup>lt;sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.



#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

# SN54ABT646, SN74ABT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS068B-D3659, JULY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise	∍ noted)†
Supply voltage range, V <sub>CC</sub> –	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_0 \dots -0.1$	5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT646	96 mA
SN74ABT646	
Input clamp current, $I_{ K }(V_1 < 0)$	18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	1 W
NT package	1.3 W
Storage temperature range	'C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

		SN54A	BT646	SN74A	BT646	TINU
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	,57	2		V
V <sub>IL</sub>	Low-level input voltage		⊘¥ 0.8		0.8	V
V <sub>I</sub>	Input voltage	Q.	· V <sub>CC</sub>	0	Vcc	V
Іон	High-level output current	3	-24		-32	mA
loL	Low-level output current	8	48		64	mA
Δt/Δv	Input transition rise or fall rate	8	5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### SN54ABT646, SN74ABT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA445755		TEST CONDITIONS		T	<sub>A</sub> = 25°C	;	SN54A	BT646	SN74A	BT646	
PARAMETER	"	SI CONDITIONS	5	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$		2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			٧
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡	<u> </u>	<u> </u>		0.55	V
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		ζ, ±1		±1	
lį	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	6	50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				50	N	-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	,			±100	<u> </u>			±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	य	50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V		Outputs high			250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	I <sub>O</sub> = 0,	Outputs low			30		30		30	mA
	V1 = V00 01 GIVD		Outputs disabled			250		250		250	μΑ
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>CC</sub>	One input at 3.4 or GND	V,			1.5		1.5		1.5	mA
Ci	V <sub>1</sub> = 2.5 V or 0.5 V		Control inputs		7						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		12						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> =		SN54A	BT646	SN74A	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	]
f <sub>clock</sub>	Clock frequency		0	125	0	<b>125</b>	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low		4		4.	15.55	4		ns
	Sotup time A or B before CLIVADA or CLIVAA	High	3.5		3.5	7/2	3.5		
t <sub>su</sub>	Setup time, A or B before CLKAB† or CLKBA†	Low	3		₹/3°		3		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑	•	0		0		0		ns

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

### SN54ABT646, SN74ABT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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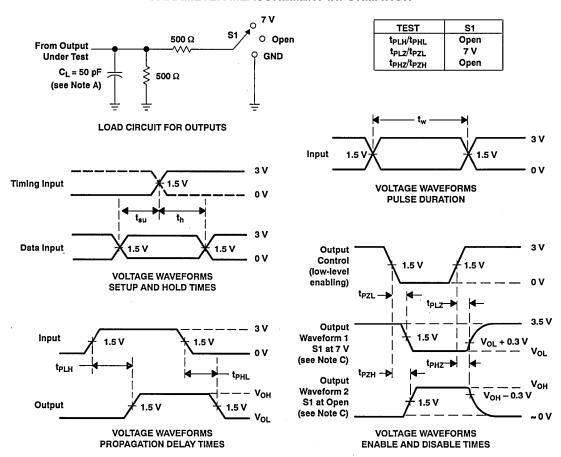
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT646	SN74ABT646		UNIT
	( 0.)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125					125		MHz
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2.2	4	6.8			2.2	7.8	ns
t <sub>PHL</sub>	CERBA OI CERAB	AUID	1.7	4	7.4			1.7	8.4	115
t <sub>PLH</sub>	A or B	B or A	1.5	3	5.9		25	1.5	6.9	ns
t <sub>PHL</sub>	7 7016	BUIA	1.5	3.3	5.9		,5	1.5	6.9	115
t <sub>PLH</sub>	SAB or SBA†	B or A	1.5	4	6.1		Ç.	1.5	7.1	ns
t <sub>PHL</sub>	SAB OF SBA	B OF A	1.5	3.6	6.9		*	1.5	7.9	113
t <sub>PZH</sub>	OE	A or B	1	4.3	5.3	25		1	6.3	ns
t <sub>PZL</sub>	]	AOIB	2.1	5.8	7.4			2.1	8.8	113
t <sub>PHZ</sub>	- OE	A or B	1.5	3.5	7.3	Q.		1.5	8.3	ns
t <sub>PLZ</sub>	]	AUID	1.5	3	7			1.5	7.5	115
t <sub>PZH</sub>	DIR	A or B	1.2	4.5	5.7			1.2	6.7	ns
t <sub>PZL</sub>		AUID	2.5	6.5	9			2.5	9.5	113
t <sub>PHZ</sub>	DIR	A or B	1.5	3.8	6.7			1.5	7.7	ns
t <sub>PLZ</sub>	] ""	AUID	1.5	3.8	7.2			1.5	8.2	115

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

#### SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

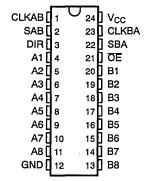
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

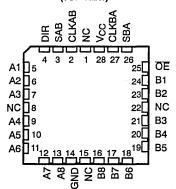
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646A.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

SN54ABT646A...JT PACKAGE SN74ABT646A...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT646A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646A is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT646A is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT646A is characterized for operation from  $-40^{\circ}$ C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



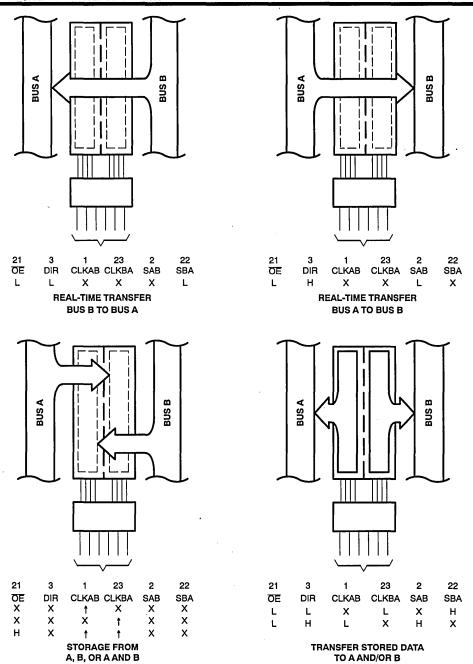


Figure 1. Bus-Management Functions

Pin numbers shown are for DB, DW, JT, and NT packages.



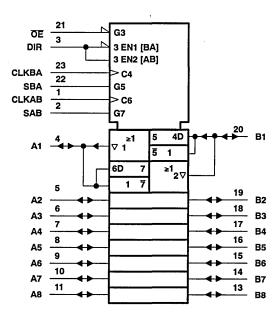
### **SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLE**

		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
X	X	1	Х	Х	Х	Input	Unspecified <sup>†</sup>	Store A, B unspecified†
X	X	X	†	Х	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>
Н	Х	Ť	†	Х	Х	Input	Input	Store A and B data
Н	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L _	L	X	L_	X	н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L _	н	L	X	Н	X	Input	Output	Stored A data to B bus

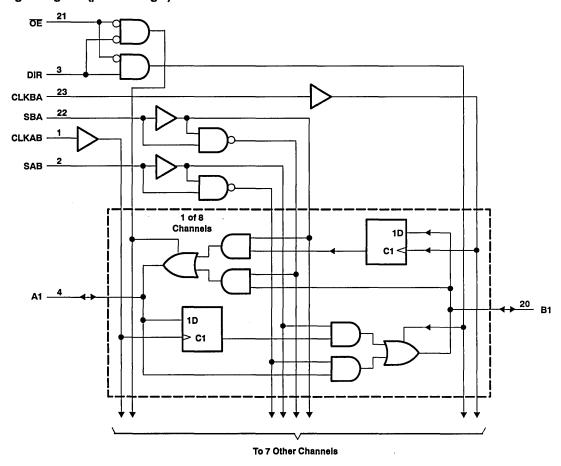
<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

#### logic symbol<sup>‡</sup>



<sup>&</sup>lt;sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

### **SN54ABT646A**, **SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless other	wise noted)†
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT646A	96 mA
SN74ABT646A	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		SN54AE	3T646A	SN74AB	UNIT	
ľ		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	٧
Vı	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

#### **SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS

SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		OT CONDITIO	NC.	Т	A = 25°C		SN54AE	T646A	SN74AE	3T646A	
PARAMETER	115	ST CONDITIC	INS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V <sub>1</sub>	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m	4	2			2				v
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m}_{A}$	Α	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	<b>V</b>
I.	V <sub>CC</sub> = 5.5 V,	I = V <sub>CC</sub> or GND				±1		±1		±1	μА
lį	$V_I = V_{CC}$ or GND					±100		±100		±100	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
l <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V},$	$V_0 = 0.5 V$				-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.9$	5 V			±100				±100	μА
ICEX	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μA
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V		Outputs high			250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			30		30		30	mA
	11-166 91 9115	I = ACC OL GIAD				250		250		250	μΑ
ΔI <sub>CC</sub> #		$_{\rm C}$ = 5.5 V, One input at 3. ner inputs at V $_{\rm CC}$ or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	·	Control inputs		7						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5	V	A or B ports		12						pF

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		T646A	SN74ABT646A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	125	0	125	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	4		4		4		ns
t <sub>su</sub>	Setup time, A or B before CLKAB† or CLKBA†	3		3.5		3		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑	0		1.5		0		ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

### **SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

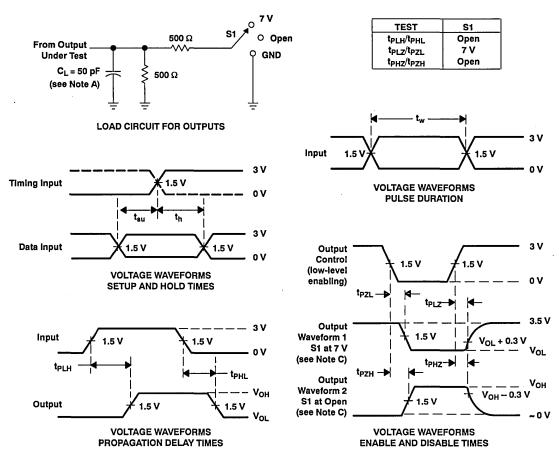
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	T646A	SN74AB	T646A	UNIT
	(	(5517 51)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125			125		125		MHz
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	2.2	5.6	ns
t <sub>PHL</sub>	CLRBA OI CLRAB	AUID	1.7	4	5.1	1.2	6.7	1.7	5.6	113
t <sub>PLH</sub>	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t <sub>PHL</sub>	7 ^0''	D 01 A	1.5	3.3	4.6	1.5	5.6	1.5	5.4	115
t <sub>PLH</sub>	SAB or SBA†	B or A	1.5	4	5.1	1.5	7.8	1.5	6.5	ns
t <sub>PHL</sub>	T SAB OF SBA	5017	1.5	3.6	4.9	1.5	6.2	1.5	5.9	118
t <sub>PZH</sub>	OE OE	A a = B	1.5	4.3	5.3	1.5	7	1.5	6.3	
t <sub>PZL</sub>	7 6 1	A or B	3	5.8	7.4	3	10.5	3	8.8	ns
t <sub>PHZ</sub>	OE OE	A == D	1.5	3.5	4.5	1	7.3	1.5	5	ns
t <sub>PLZ</sub>	7 5 1	A or B	1.5	3	4	1.5	5.7	1.5	4.5	ns
t <sub>PZH</sub>	DIR	A D	1.5	4.5	5.7	1.5	7.3	1.5	6.7	
t <sub>PZL</sub>		A or B	2.5	6.5	9	2.5	11	2.5	9.5	ns
t <sub>PHZ</sub>	DIR	A or B	1.5	3.8	5	1	9	1.5	5.7	no.
t <sub>PLZ</sub>		A or B	1.5	3.8	4.7	1.2	6.7	1.5	6	ns

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992





NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50~\Omega$ ,  $t_f \leq 2.5~ns$ ,  $t_f \leq 2.5~ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

# SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

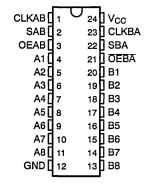
SCBS083B-D3709, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

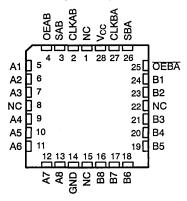
#### description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT651.

SN54ABT651 ... JT PACKAGE SN74ABT651 ... DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT651 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all the other data sources to the two sets of bus lines are at high impedance, each set will remain at its last state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT651 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

#### SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS083B-D3709, JANUARY 1991-REVISED OCTOBER 1992

#### description (continued)

The SN54ABT651 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT651 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### **FUNCTION TABLE**

		INPU	TS			DAT	A I/O	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	Н	<b>†</b>	<b>†</b>	X	X	Input	Input	Store A and B data
×	н	<b>†</b>	H or L	×	×	Input	Unspecified <sup>†</sup>	Store A, hold B
н	н	†	t	X‡	×	Input	Output	Store A in both registers
L	X	H or L	<b>†</b>	X	Х	Unspecified <sup>†</sup>	Input	Hold A, store B
L	L	†	t	×	X‡	Output	input	Store B in both registers
L	L	X	X	x	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	Н	Output	Output	Stored B data to A bus
Н	н	X	X	, L	×	Input	Output	Real-time A data to B bus
н	Н	H or L	X	Н	Х	Input	Output	Stored A data to B bus
н	L ·	H or L	H or L	н	н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

<sup>\*</sup> When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.

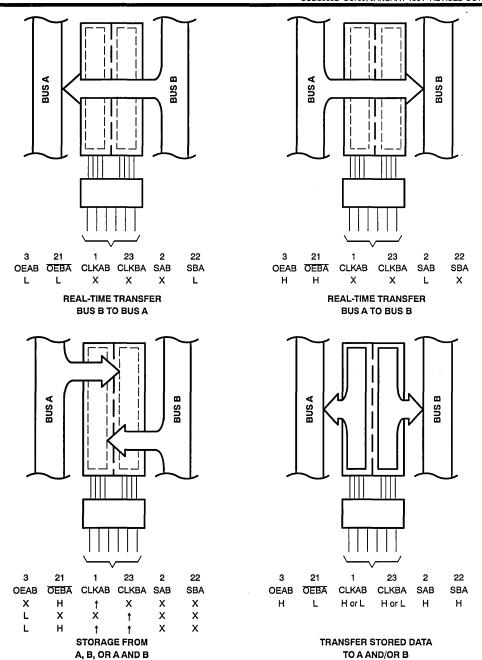


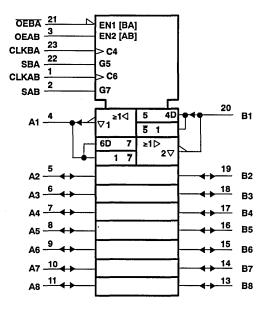
Figure 1. Bus-Management Functions

Pin numbers shown are for DB, DW, JT, and NT packages.



# SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS083B-D3709, JANUARY 1991-REVISED OCTOBER 1992

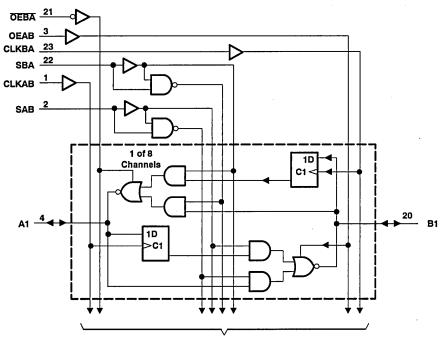
#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

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#### logic diagram (positive logic)



To 7 Other Channels

Pin numbers shown are for DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>	t
Supply voltage range, V <sub>CC</sub> 0.5 V to 7	٧
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub> −0.5 V to 5.5	
Current into any output in the low state, I <sub>O</sub> : SN54ABT651	ıΑ
SN74ABT651 128 m	ıΑ
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	
DW package 1 \	W
NT package	
Storage temperature range65°C to 150°	,C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



### SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 2)

	<del></del>	SN54ABT65	SN74A	SN74ABT651	
		MIN MA	MIN	MAX	UNIT
Vcc	Supply voltage	4.5 5	4.5	5.5	٧
VIH	High-level input voltage	2	2		٧
VIL	Low-level input voltage	& 0.	3	0.8	٧
Vı	Input voltage	o V <sub>C</sub>	0	Vcc	V
l <sub>он</sub>	High-level output current		1	-32	mA
loL	Low-level output current	ූ ් 4	3	64	mA
Δt/Δν	Input transition rise or fall rate	á"	5	5	ns/V
T <sub>A</sub>	Operating free-air temperature	-55 12	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEST CONDITIONS			T	A = 25°C	;	SN54ABT651		SN74ABT651		
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA	·			-1.2		-1.2		-1.2	V
·	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	3			3		3				
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	2			2				V		
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$	2‡					2			
.,	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,			0.55‡		J.		0.55	\ \		
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		ζ;, ±1		±1	•
lj	V <sub>I</sub> = V <sub>CC</sub> or GND	A or B ports			±100	4	±100		±100	μΑ	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	Ó	50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	23	-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 \	V	_	***************************************	±100	δ,			±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	र	50		50	μА
101	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V	I <sub>O</sub> = 0,	Outputs high			250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$		Outputs low			30		30		30	mA
	AI - ACC OL CIAD		Outputs disabled			250		250		250	μΑ
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		6						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V A or B ports				7.5		1				pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>S$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS083B-D3709, JANUARY 1991-REVISED OCTOBER 1992

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		BT651	SN74ABT651		UNIT
		MIN	MAX	MIN MAX		MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	125	0,	C)125	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	4		.42	(Ø)	4		ns
t <sub>su</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	3		<i>হ</i> িষ্ক	,	3		ns
th	Hold time, A or B after CLKAB† or CLKBA†	0		₹0		0		ns

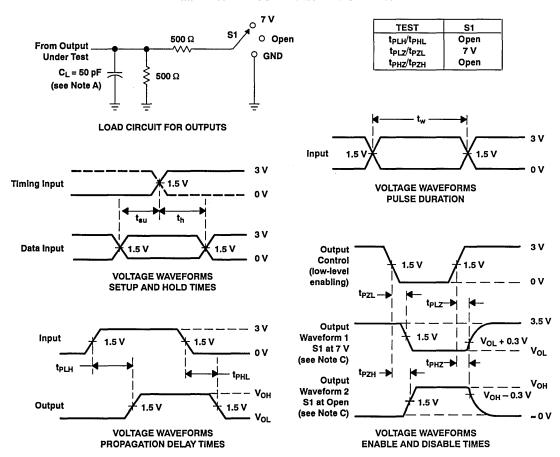
# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT651		SN74ABT651		UNIT	
	( 5.)	(001: 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>		<del></del>	125			125		125		MHz	
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	5.9	2.2	5.6	ns	
t <sub>PHL</sub>	CLRBA OF CLRAB	AUID	1.7	4	5.1	1.7	5.9	1.7	5.6		
t <sub>PLH</sub>	A or B	B or A	1.5	4	5.1	1.5	6:4	1.5	6.2		
t <sub>PHL</sub>	1 7015	BUIA	1.5	3.3	4.6	1.5	\$.6	1.5	5.4	ns	
t <sub>PLH</sub>	SAB or SBA†	A or B	1.5	4	5.1	1.5	<i>≸</i> 6.8	1.5	6.5	ns	
t <sub>PHL</sub>	SAB OF SBA		1.5	3.6	4.9	1.5	6.2	1.5	5.9		
t <sub>PZH</sub>	OEBA	А	1.3	3.6	4.6	1,33	5.9	1.3	5.8	ns	
t <sub>PZL</sub>	] CEBA		2.5	5.7	6.8	<b>,2.</b> 5	8.9	2.5	8.5		
t <sub>PHZ</sub>	OEBA	^	1.5	3.2	4.5	,∜°1.5	6.2	1.5	5		
t <sub>PLZ</sub>		<b>^</b>	1.5	3	3.8	ື 1.5	4.3	1.5	4.1	ns	
t <sub>PZH</sub>	OEAB	В	1.8	4.3	6.1	1.8	6.7	1.8	6.5		
t <sub>PZL</sub>	] OEAB	В	2.9	5.5	6.5	2.9	7.6	2.9	7.4	ns	
t <sub>PHZ</sub>	OEAB	-	1.5	3.3	4.5	1.5	6.5	1.5	5.5		
t <sub>PLZ</sub>	CEAB	В	1.5	3.4	4.4	1.5	5.2	1.5	5.1	ns	

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS083B-D3709, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_r \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

# SN54ABT652, SN74ABT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

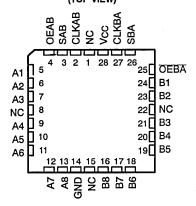
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT652.

SN54ABT652 . . . JT PACKAGE SN74ABT652 . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT652 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

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#### SN54ABT652, SN74ABT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

#### description (continued)

The SN74ABT652 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT652 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT652 is characterized for operation from  $-40^{\circ}$ C to 85°C.

#### **FUNCTION TABLE**

INPUTS				DATA	A I/O†	OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	L	L	X	Х	Input	Input	Isolation
L	Н	<b>†</b>	<b>†</b>	X	х	Input	Input	Store A and B data
Х	Н	†	Ĺ.	Х	х	Input	Unspecified <sup>‡</sup>	Store A, hold B
Н	н	†	Ť	X‡	х	Input	Output	Store A in both registers
L	Х	L	†	X	х	Unspecified <sup>‡</sup>	Input	Hold A, store B
L	L	1	t	Х	X‡	Output	Input	Store B in both registers
L	L	X	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	L	Х	н	Output	Input	Stored B data to A bus
н	н	X	X	L	х	Input	Output	Real-time A data to B bus
Н	Н	L	Х	н	х	Input	Output	Stored A data to B bus
н	L	L	Ĺ	н	н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

<sup>&</sup>lt;sup>‡</sup> Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

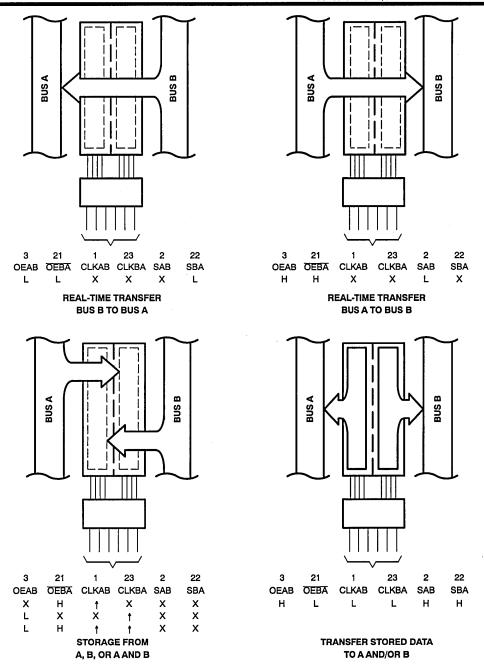


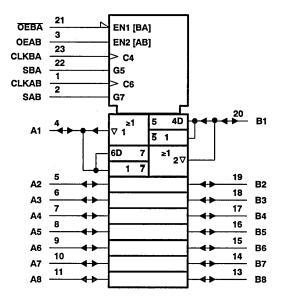
Figure 1. Bus-Management Functions

Pin numbers shown are for DB, DW, JT, and NT packages.



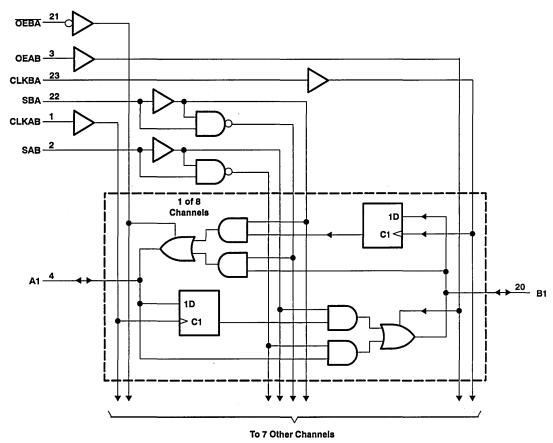
### SN54ABT652, SN74ABT652 **OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

#### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### SN54ABT652, SN74ABT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>
Current into any output in the low state, Io: SN54ABT652
SN74ABT652
Input clamp current, I <sub>IK</sub> (V <sub>1</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package
DW package
NT package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

		SN54A	BT652	SN74A	BT652	LIMIT
		MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2	, N	2		٧
V <sub>IL</sub>	Low-level input voltage		<b>₹ 0.8</b>		0.8	٧
Vı	Input voltage	0.		0	Vcc	٧
Іон	High-level output current	3	-24		-32	mA
loL	Low-level output current	8	48		64	mA
Δt/Δν	Input transition rise or fall rate	<u> </u>	5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### SN54ABT652, SN74ABT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	_			τ	A = 25°C	;	SN54A	BT652	SN74A	BT652	
PARAMETER	"	EST CONDITION	15	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V <sub>i</sub>	l <sub>l</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA		2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>				0.55	
1.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		ু(≩1		±1	
l <sub>į</sub>	$V_I = V_{CC}$ or GND		A or B ports			±100		<b>∌</b> 100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$				50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	<u>.</u> Ĉ	-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	v			±100	ರ			±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Ş	50		50	μА
lo¶	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V		-50	-100	-180	≪−50	-180	-50	180	mA
	V 5 5 V	1 0	Outputs high			250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			30		30		30	mA
	17 - 100 01 0115		Outputs disabled			250		250		250	μΑ
Δl <sub>CC</sub> #	$V_{CC} = 5.5 \text{ V},$ Other inputs at $V_{CC}$	One input at 3.4 or GND	4 V,	•		1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		7						pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,	A or B ports		12						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> =		SN54A	BT652	SN74A	BT652	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	ĺ
f <sub>clock</sub>	Clock frequency	0	125	0,	√ <u>12</u> 5	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	4	-	.49	.W.	4		ns
t <sub>su</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	3.5		⟨3,5∖	<del>~</del>	3.5		ns
t <sub>h</sub>	Hold time, A or B after CLKAB↑ or CLKBA↑	0		<b>`</b> 0		0		ns

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## **SN54ABT652, SN74ABT652 OCTAL BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

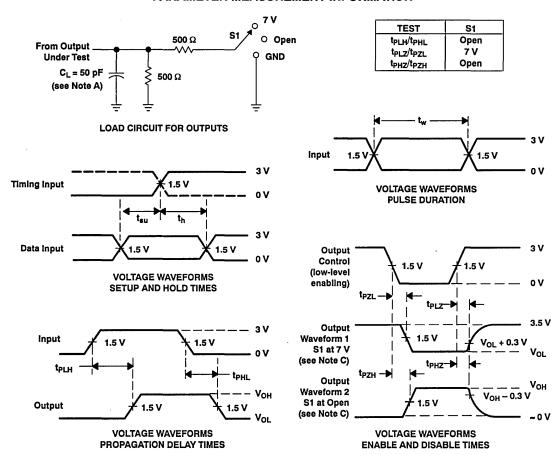
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54A	3T652	SN74A	BT652	UNIT
	( 0.)	(33.13.)	MIN	TYP	MIN	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125	200		125		125		MHz
t <sub>PLH</sub>	CLK	B or A	2.2	5.3	6.8	2.2	8.2	2.2	7.8	
t <sub>PHL</sub>	OLK	B 01 A	1.7	5.9	7.4	1.7	8.8	1.7	8.4	ns
tpLH	A or B	B or A	1.5	4.4	5.7	1.5	.7	1.5	6.7	ns
tpHL	AUID	B 01 A	1.5	4.4	5.7	1.5	47	1.5	6.7	ns
t <sub>PLH</sub>	SAB or SBA†	B or A	1.5	4.6	5.9	1.5	6,7.4	1.5	6.9	
t <sub>PHL</sub>	SAB OF SBA	BUA	1.5	5.4	6.7	1.5 🗘	8	1.5	7.7	ns
t <sub>PZH</sub>	OEBA		1.3	3.3	4.6	1,8	6	1.3	5.8	
t <sub>PZL</sub>	UEBA	^	2.5	4.5	6.8	<i>2</i> ,5	8.9	2.5	8.5	ns
t <sub>PHZ</sub>	OEBA		1.5	6.2	7.7	<sub>Q</sub> 9.5	8.3	1.5	8.2	
t <sub>PLZ</sub>	OEBA	A	1.5	5	6.3	₹ 1.5	7.1	1.5	6.8	ns
t <sub>PZH</sub>	OEAB	В	1.8	3.8	6.1	1.8	6.9	1.8	6.5	
t <sub>PZL</sub>	OEAB		2.9	4.9	6.5	2.9	7.6	2.9	7.4	ns
t <sub>PHZ</sub>	OEAB	В	1.5	4.5	5.7	1.5	7.1	1.5	6.9	
t <sub>PLZ</sub>	OEAB		1.5	4.1	5.3	1.5	6.6	1.5	6.2	ns

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS070B-D3660, JULY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

#### SN54ABT652A, SN74ABT652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

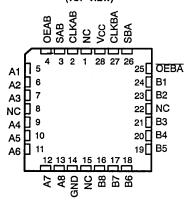
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT652A.

SN54ABT652A . . . JT PACKAGE SN74ABT652A . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT652A...FK PACKAGE (TOP VIEW)



NC - No internal connection

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

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#### SN54ABT652A, SN74ABT652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

#### description (continued)

The SN74ABT652A is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT652A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT652A is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

		INPU	rs			DATA	\ I/O <sup>†</sup>	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	L ·	L	Х	Х	Input	Input	Isolation
L	Н	<b>†</b>	1	X	Х	Input	Input	Store A and B data
x	Н	<b>†</b>	L	X	X	Input	Unspecified <sup>‡</sup>	Store A, hold B
Н	Н	<b>†</b>	1	X‡	X	Input	Output	Store A in both registers
L	X	L	1	X	X	Unspecified <sup>‡</sup>	Input	Hold A, store B
L	L	<b>†</b>	<b>↑</b>	X	X‡	Output	Input	Store B in both registers
L	L	X	Х	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	Н	Output	Input	Stored B data to A bus
н	Н	X	X	L	X	Input	Output	Real-time A data to B bus
н	Н	L	X	Н	X	Input	Output	Stored A data to B bus
н	L	L	L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

<sup>\*</sup> Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

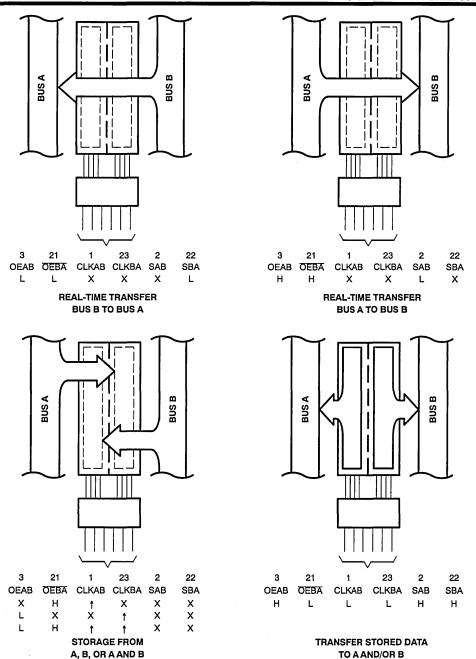


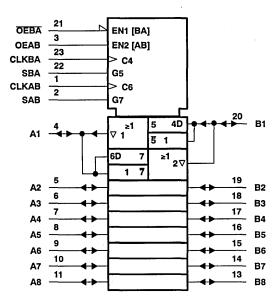
Figure 1. Bus-Management Functions

Pin numbers shown are for DB, DW, JT, and NT packages.



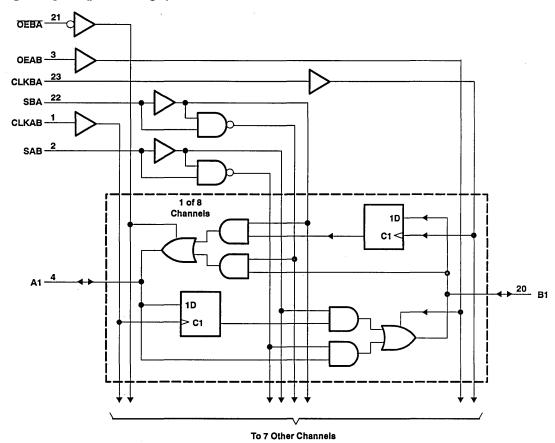
# SN54ABT652A, SN74ABT652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### SN54ABT652A, SN74ABT652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT652A
SN74ABT652A
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
DW package 1 W
NT package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

		SN54A	BT652A	SN74AB	T652A	UNIT
ĺ		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	. 2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
Vi	Input voltage	0	Vcc	0	Vcc	V
loн	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	ပ့

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## SN54ABT652A, SN74ABT652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				7	<sub>A</sub> = 25°C	;	SN54AE	T652A	SN74AE	T652A	
PARAMETER	"	EST CONDITIC	ons	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3	•	3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/		2			2				V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 m/	A	2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
$V_{OL}$	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	V
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
11	VI = VCC or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μA
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mΑ
			Outputs high			250		250		250	μА
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{L} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			30		30		30	mΑ
	AI - A26 01 GIAD		Outputs disabled			250		250		250	μA
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>C</sub>	One input at CC or GND	1 3.4 V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 \	/	Control inputs		7						рF
Cio	$V_0 = 2.5 \text{ V or } 0.5$	V	A or B ports		12						рF

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> :		SN54AB	T652A	SN74AB	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	125	0	125	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	4		4		4		ns
t <sub>su</sub>	Setup time, A or B before CLKAB† or CLKBA†	3		3		3		ns
t <sub>h</sub>	Hold time, A or B after CLKAB† or CLKBA†	0		0		0		ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT652A, SN74ABT652A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

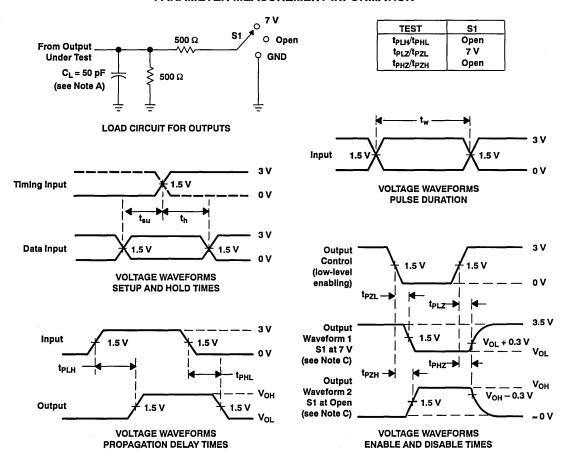
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	CC = 5 V A = 25°C		SN54AB	T652A	SN74AB	T652A	UNIT
	(,	(00 0)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125	200		125		125		MHz
t <sub>PLH</sub>	CLK	B or A	2.2	4	5.1	2.2	5.9	2.2	5.6	ns
t <sub>PHL</sub>			1.7	4	5.1	1.7	5.9	1.7	5.6	115
t <sub>PLH</sub>	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t <sub>PHL</sub>	7 ^0'5	l Bory	1.5	3.3	4.6	1.5	5.6	1.5	5.4	ns
t <sub>PLH</sub>	SAB or SBA†	B or A	1.5	4	5.1	1.5	6.8	1.5	6.5	ns
t <sub>PHL</sub>	SAB UI SBA	BULA	1.5	3.6	4.9	1,5	6.2	1.5	5.9	115
t <sub>PZH</sub>	OEBA	A	2	3.6	4.6	2	5.9	2	5.8	
t <sub>PZL</sub>	UEBA	A	3	5.7	6.8	3	8.9	3	8.5	ns
t <sub>PHZ</sub>	OEBA	^	1.5	3.2	4.5	1.5	6.2	1.5	5	
t <sub>PLZ</sub>		A	1.5	3	3.8	1.5	4.3	1.5	4.1	ns
t <sub>PZH</sub>	OEAB	В	2	4.3	6.1	2	6.7	2	6.5	
t <sub>PZL</sub>		°	3	5.5	6.5	3	7.6	3	7.4	ns
t <sub>PHZ</sub>	OEAB	В	1.5	3.3	4.5	1.5	6.5	1.5	5.5	ns
tplz	1		1.5	3.4	4.4	1.5	5.2	1.5	5.1	113

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS072B-D3875, SEPTEMBER 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

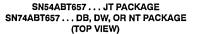
#### SN54ABT657, SN74ABT657 OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

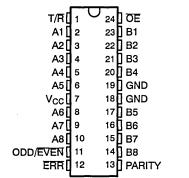
D3694, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

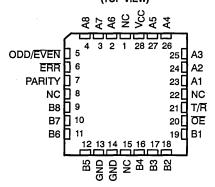
#### description

The 'ABT657 contains eight noninverting buffers with parity generator/checker circuits and control signals. The transmit/receive (T/R) input determines the direction of data flow. When T/R is high, data flows from the A port to the B port (transmit mode); when T/R is low, data flows from the B port to the A port (receive mode). When the output-enable (OE) input is high, both the A and B ports are in the high-impedance state.





SN54ABT657...FK PACKAGE (TOP VIEW)



NC - No internal connection

Odd or even parity is selected by a logic high or low level on the ODD/EVEN input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/EVEN input. For example, if ODD/EVEN is low (even parity selected) and there are five high bits on the A bus, then PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the error (ERR) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/EVEN is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, then ERR is low, indicating a parity error.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT657 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



#### SN54ABT657, SN74ABT657 OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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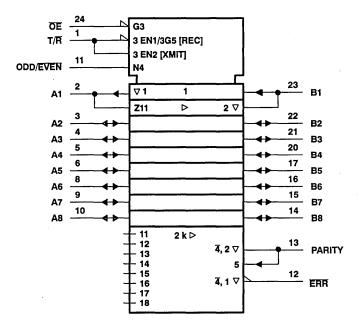
#### description (continued)

The SN54ABT657 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT657 is characterized for operation from -40°C to 85°C.

**FUNCTION TABLE** 

NUMBER OF A OR B		INPUT	S	INPUT/OUTPUT		OUTPUTS
INPUTS THAT ARE HIGH	ŌĒ	T/R	T/R ODD/EVEN PARITY		ERR	OUTPUT MODE
	L	Н	Н	Н	Z	Transmit
	L	Н	L	L	Z	Transmit
0.0.4.0.0	[ L	L	н	н	н	Receive
0, 2, 4, 6, 8	L	L	Н	L	L	Receive
	[ L	L	L	н	L	Receive
	L	L	L	L	н	Receive
	Ĺ	Н	Н	L	Z	Transmit
	L	Н	L	н	z	Transmit
40.55	L	L	н	н	L	Receive
1, 3, 5, 7	L	L	Н	L	н	Receive
	L	L	L	н	Н	Receive
	L	L	L	L	L	Receive
Don't care	H	Х	Х	Z	Z	Z

#### logic symbol†

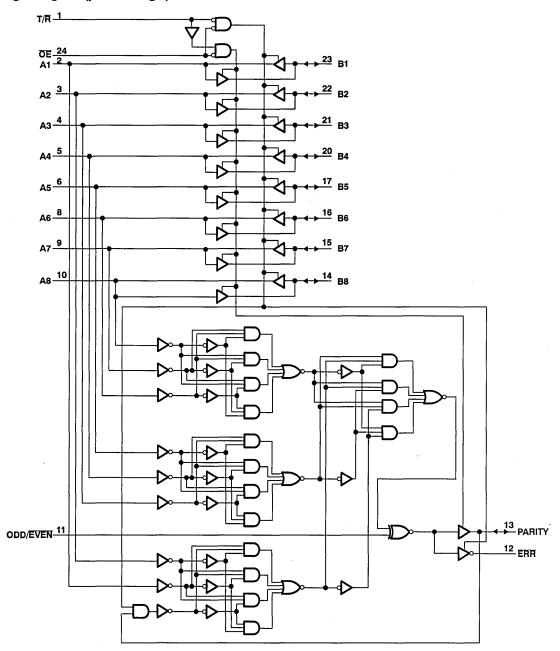


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.



# PRODUCT PREVIEW

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### SN54ABT657, SN74ABT657 OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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absolute maximum ratings over operating	g free-air temperature range	(unless otherwise noted) <sup>†</sup>
Cumply vallence range 1/		0514-71/

Supply voltage range, v <sub>CC</sub>	–0.5 V to / V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power	
Current into any output in the low state, Io: SN54ABT657 .	96 mA
	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB pace	kage 0.5 W
DW pa	ckage 1 W
NT pac	kage 1.3 W
Storage temperature range	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

	•	SN54A	SN54ABT657		SN74ABT657		
l		MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V	
V <sub>IH</sub>	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	٧	
V <sub>I</sub>	Input voltage	0	Vcc	0	Vcc	٧	
Іон	High-level output current		-24		-32	mA	
loL	Low-level output current		48		64	mA	
Δt/Δν	Input transition rise or fall rate		5		5	ns/V	
TA	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### SN54ABT657, SN74ABT657 OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		7	A = 25°C	;	SN54A	BT657	SN74ABT657		UNIT		
PARAMETER		ST CONDITION	15	MIN	TYP	MAX	. MIN	MAX	MIN	MAX	UNII		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧		
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5		•	2.5		2.5				
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA	3			3		3		v			
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA	2			2				٧			
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA		2§					2		1		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v		
VOL	$V_{OL}$ $V_{CC} = 4.5 \text{ V},  I_{OL} = 64 \text{ m}$					0.55§				0.55	v		
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА		
՝ կ	$V_I = V_{CC}$ or GND		A or B ports			±100		±100		±100			
lozh <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	<sub>C</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μΑ		
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ		
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100				±100	μΑ		
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ		
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA		
	V 55V	1 0	Outputs high			250		250		250	μΑ		
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{L} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			30		30		30	mA		
	11-1000101011		Outputs disabled			250		250		250	μA		
	V <sub>CC</sub> = 5.5 V, One	Data la sute	Outputs enabled			1		1.5		1			
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA		
	V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5	:		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs		Control inputs								pF		
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports								pF		

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

### **SN54ABT657**, **SN74ABT657** OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS D3694, JANUARY 1991-REVISED OCTOBER 1992

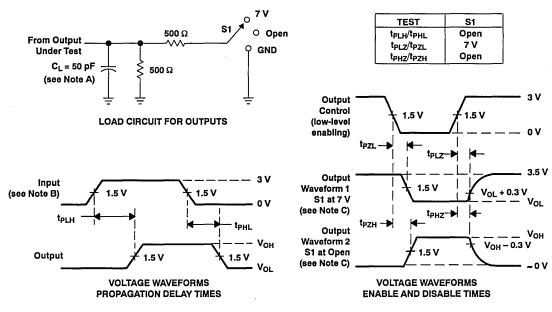
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 pF$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	ſ	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT657		SN74ABT657		
	( 01)	(00.1.01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>РLН</sub>	A or B	B or A	1.1	3.3	5	1.1		_ 1.1	5.5	ns	
t <sub>PHL</sub>		BOTA	1.2	3	4.3	1.2		1.2	4.8	l lis	
t <sub>PLH</sub>	<b>A</b> -2	PARITY	2.6	6.5	8.7	2.6		2.6	10.1	ns	
t <sub>PHL</sub>		- ANITI	3.2	7	9.1	3.2		3.2	10.6	ns	
t <sub>PLH</sub>	ODD/EVEN	PARITY, ERR	1.7	5	6.6	1.7		1.7	7.3	ns	
t <sub>PHL</sub>	ODD/EVEN		1.9	5	6.6	1.9		1.9	7.3		
t <sub>PLH</sub>	В	ERR	5.3	9.2	11.7	5.3		5.3	13.8		
t <sub>PHL</sub>	]	Enn	5.2	9.6	12.1	5.2		5.2	14.5	ns	
t <sub>PLH</sub>	PARITY	ERR	2.8	6	7.6	2.8		2.8	9.4		
t <sub>PHL</sub>	] FARIT	Enn	3.5	6.4	8	3.5		3.5	9.4	ns	
t <sub>PZH</sub>	OE	A P PARITY OF EDD	1.3	3.8	5.6	1.3		1.3	6.6	ns	
t <sub>PZL</sub>	UE	A, B, PARITY, or ERR	1.9	4.4	7	1.9		1.9	8.2	i ns	
t <sub>PHZ</sub>	OE OE	A, B, PARITY, or ERR	3.1	5.1	7	3.1		3.1	7.6	ne	
t <sub>PLZ</sub>	7	A, D, FARILT, OF ERR	3.4	5.4	7.6	3.4		3.4	8.1	ns	

#### SN54ABT657, SN74ABT657 OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

D3694, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3779, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

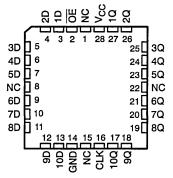
These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

SN54ABT821 . . . JT PACKAGE SN74ABT821 . . . DB, DW, OR NT PACKAGE (TOP VIEW)

OE[	1	U <sub>24</sub>	] Vcc
1D[	2	23	] 1Q
2D[	3	22	2Q
3D[	4	21	] 3Q
4D[	5	20	] 4Q
5D[	6	19	] 5Q
6D[	7	18	] 6Q
7D[	8	17	] 7Q
8D[	9	16	] 8Q
9D[	10	15	] 9Q
10D[	11	14	] 10Q
GND[	12	13	] CLK

SN54ABT821 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT821 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT821 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT821 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

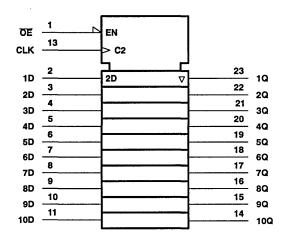


D3779, FEBRUARY 1991-REVISED OCTOBER 1992

## FUNCTION TABLE (each flip-flop)

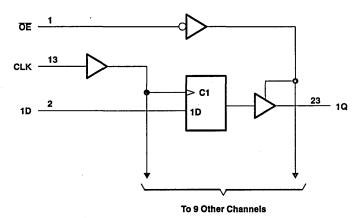
	INPUTS		OUTPUT
QE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Χ	Q <sub>o</sub>
Н	X	Х	z

#### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.



D3779, FEBRUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise	∍ noted)†
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_0 \dots -0$ .	5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT821	96 mA
SN74ABT821	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	
DW package	1 W
NT package	1.3 W
Storage temperature range –65°	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		SN54A	BT821	SN74A	BT821	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	٧
Vi	Input voltage	0	Vcc	0	Vcc	٧
Юн	High-level output current		-24		-32	mA
l <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

D3779, FEBRUARY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T	A = 25°C	;	SN54A	BT821	SN74A					
PARAMETER	l lest conditio	NS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT			
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V			
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5					
V <sub>OH</sub>	$V_{CC} = 5 \text{ V},  I_{OH} = -3 \text{ mA}$		3			3		3		v			
*OH	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$					2				· •			
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		]			
V	V <sub>CC</sub> = 4.5 V, l <sub>OL</sub> = 48 mA				0.55		0.55			_ v			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	٧			
Ι	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ			
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА			
l <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ			
I <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ			
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μÀ			
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-140	-180	-50	-180	-50	-180	mA			
	V 55V 1 0	Outputs high		1	250		250		250	μА			
Icc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA			
	V1 = VCC 01 G115	Outputs disabled		0.5	250		250		250	μΑ			
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 Other inputs at V <sub>CC</sub> or GND	V,			1.5		1.5		1.5	mA			
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			4						pF			
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7						pF			

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> =		SN54A	BT821	SN74AI	UNIT	
	'		MIN	MAX	MIN	MAX	MIN	MAX	1
f <sub>clock</sub> Clock frequency			0	125	0	125	0	125	MHz
	Pulse duration, CLK high or low	High	2.9		2.9		2.9		
tw		Low	3.8		3.8		3.8		ns
t <sub>su</sub>	Setup time, data before CLK†		2.1		2.1		2.1		ns
th	Hold time, data after CLK↑		1.3		1.3		1.3		ns

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

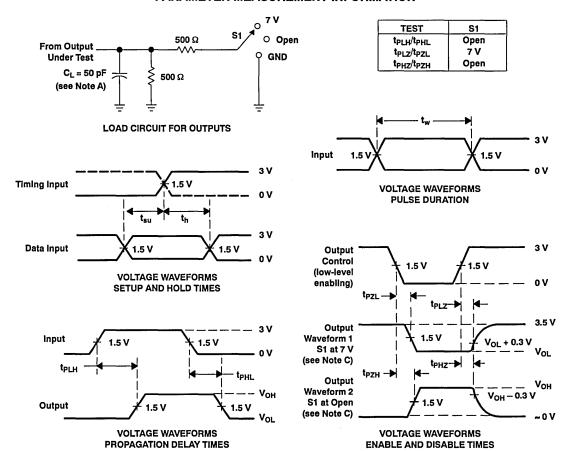
# SN54ABT821, SN74ABT821 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS D3779, FEBRUARY 1991—REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM (INPUT)	TO (OUTPUT)	1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			BT821	SN74ABT821		UNIT
	(INTO I)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125			125		125		MHz
t <sub>PLH</sub>	CIV		2.1	4.1	5.6	2.1		2.1	6.2	ns
t <sub>PHL</sub>	CLK	, Q	2.8	4.6	6.2	2.8		2.8	6.7	115
t <sub>PZH</sub>	ŌĒ		1	3	4.5	1		1	5.3	
t <sub>PZL</sub>	OE .	Q	2.2	4.1	5.6	2.2		2.2	6.3	ns
t <sub>PHZ</sub>	ŌĒ		2.7	4.7	6.2	2.7		2.7	6.7	
t <sub>PLZ</sub>	OE	Q	2.8	4.6	6.1	2.8		2.8	6.5	ns

D3779, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega_1$  t<sub>1</sub>  $\leq$  2.5 ns, t<sub>1</sub>  $\leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3695, JANUARY 1991-REVISED OCTOBER 1992

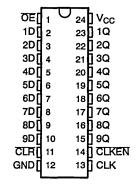
- Space-Saving Package Option:
   Shrink Small-Outline Package (DB)
   Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

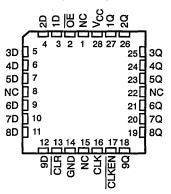
These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable (CLKEN) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'ABT823 has noninverting data (D) inputs. Taking the clear (CLR) input low causes the nine Q outputs to go low independently of the clock.

SN54ABT823...JT PACKAGE SN74ABT823...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT823...FK PACKAGE (TOP VIEW)



NC - No internal connection

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT823 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



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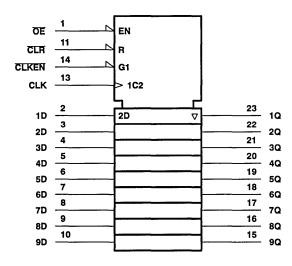
#### description (continued)

The SN54ABT823 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT823 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

FUNCTION TABLE (each flip-flop)

	INPUTS				
ŌĒ	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	Н	L	<b>†</b>	Н	н
L	Н	L	†	L	L
L	Н	Н	X	X	Qo
Н	Х	Х	Х	X	z

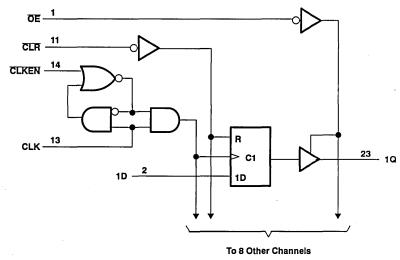
#### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

D3695, JANUARY 1991-REVISED OCTOBER 1992

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	−0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT823	96 mA
SN74ABT823	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, IOK (VO < 0)	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air): DB package	
DW package	
NT package	
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

D3695, JANUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

		SN	54AI	BT823	SN74A		
		м	IN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		.5	5.5	4.5	5.5	٧
VIH	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		8.0	V
Vi	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate			5		5	ns/V
TA	Operating free-air temperature		55	125	-40	85	ပ္

NOTE 2: Unused or floating inputs must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54ABT823		SN74ABT823		UNIT	
	TEST CONDITIONS			MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},$	l <sub>l</sub> = -18 mA				-1.2		-1.2		-1.2	٧
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = −3 mA			2.5		_	2.5		2.5		٧
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		_	3		3		
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				
	V <sub>CC</sub> = 4.5 V,	5 V, I <sub>OH</sub> = -32 mA				_			2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA					0.55		0.55			V
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1		±1	μА
I <sub>OZH</sub>	$V_{CC} = 5.5 \text{ V},$	, V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	$V_{CC} = 0 \text{ V}$ , $V_I \text{ or } V_O \le 4.5 \text{ V}$				±100				±100	μА	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
l <sub>O</sub> §	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V		-50	-140	-180	50	-180	50	-180	mA
	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or Gi		Outputs high		1	250		250		250	μА
Icc			Outputs low		24	30		30		30	mA
	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -		Outputs disabled		0.5	250		250		250	μА
Δlcc <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, Other inputs at	One input at 3.4 V t V <sub>CC</sub> or GND				1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V										pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V										pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

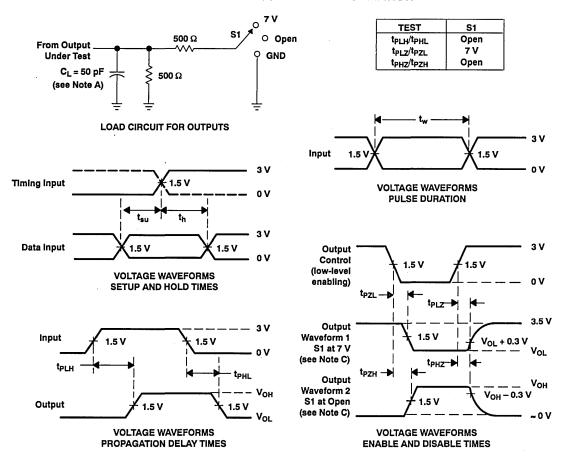
<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

D3695, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54ABT827, SN74ABT827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

D3696, JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

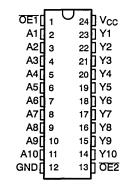
#### description

These 10-bit buffers and bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

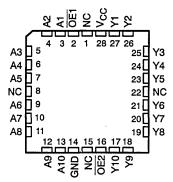
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all ten outputs are in the high-impedance state. The 'ABT827 provides true data at its outputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT827 . . . JT PACKAGE SN74ABT827 . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT827 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT827 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT827 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

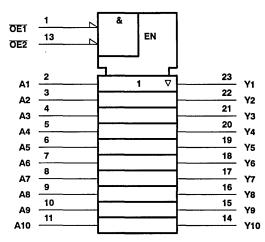
PRODUCT PREVIEW

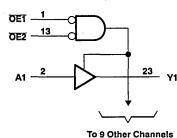
### **FUNCTION TABLE**

	INPUTS	OUTPUT	
OE1	OE2	Α	Υ
L	L	L	L
L	L	Н	Н
Н	X	X	Z
Х	н	х	z

# logic symbol†

# logic diagram (positive logic)





Pin numbers shown are for DB, DW, JT, and NT packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	. −0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT827	96 mA
SN74ABT827	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>\$\</sup>forall \text{Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\*\*These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# recommended operating conditions (see Note 2)

		SN54ABT827		SN74A	BT827	TINU
		MIN	MAX	MIN	MAX	וואט
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	V
Vı	Input voltage	0	Vcc	0	Vcc	V
I <sub>ОН</sub>	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	ů

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			A = 25°C	;	SN54A	BT827	SN74ABT827		UNIT
PARAMETER	lesi condition	No	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	ONII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	$V_{CC} = 5 \text{ V},  I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$		2			2				•
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			<
VOL	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>				0.55	•
lı	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$			±1		±1		±1	μA	
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$			50		50		50	μΑ	
lozL	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$			-50		-50		-50	μΑ	
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V}, \qquad V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
lo <sup>§</sup>	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-140	-180	-50	-180	-50	-180	mA
	V 55V	Outputs high		1	250		250		250	μΑ
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	11 - 166 or all	Outputs disabled		0.5	250		250		250	μA
	V FEV One inner at 2.4V	Outputs enabled			1.5		1.5		1.5	mA
Δlcc <sup>¶</sup>	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND	Outputs disabled			50		50		50	μΑ
	Care inpute at 766 of City	Control inputs			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			4	•				_	pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

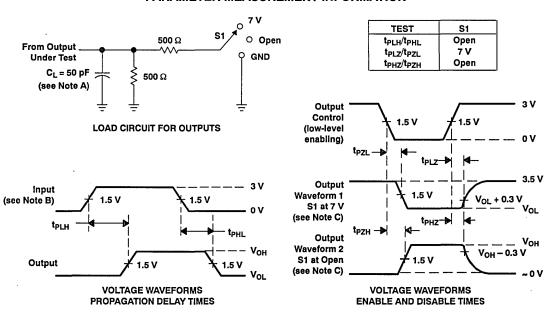
<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT827		SN74ABT827		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	Α			1.1	3	4.4	1.1		1.1	4.8	
t <sub>PHL</sub>		1	1.1	2.9	4.1	1.1		1.1	4.7	ns	
t <sub>PZH</sub>	ŌĒ	Y	1.6	3.7	5.1	1.6		1.6	5.9	ns	
t <sub>PZL</sub>	OE.		2.6	4.6	5.9	2.6		2.6	6.9		
t <sub>PHZ</sub>	ŌĒ		2	4.8	6.3	2		2	6.8		
t <sub>PLZ</sub>	OE .	T	2.5	5.1	6.6	2.5		2.5	6.9	ns	

# PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_r \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

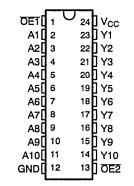
# description

These 10-bit buffers and bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

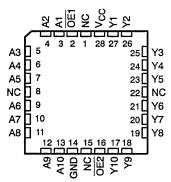
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all ten outputs are in the high-impedance state. The 'ABT828 provides inverting data at its outputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT828...JT PACKAGE SN74ABT828...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT828 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT828 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT828 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT828 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

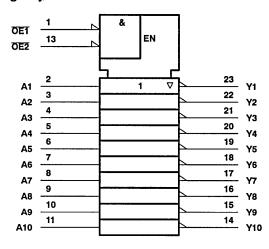
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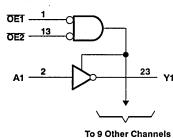
# **FUNCTION TABLE**

	INPUTS	OUTPUT	
OET	OE2	Α	Y
L	L	L	Н
L	L	Н	L
н	X	X	z
Х	н	Х	z

# logic symbol†

# logic diagram (positive logic)





Pin numbers shown are for DB, DW, JT, and NT packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the high state o	r power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54AB1	Г828	96 mA
SN74AB7	T828	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air):	DB package	0.5 W
	DW package	1 W
	NT package	1.3 W
Storage temperature range		-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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# recommended operating conditions (see Note 2)

		SN54ABT828		SN74A	UNIT	
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2		2		٧
$V_{IL}$	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24		-32	mA
l <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			A = 25°C	;	SN54A	BT828	SN74ABT828		UNIT
PANAMETER	TEST CONDITION	NO.	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = −3 mA		2.5			2.5		2.5		
V	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V},  I_{OH} = -24 \text{ mA}$	,	2			2				V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	V
lı	$V_{CC} = 5.5 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μА
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μΑ
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				50		-50		-50	μΑ
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
l <sub>O</sub> §	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-140	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high		1	250		250		250	μΑ
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	1 1 - 100 or and	Outputs disabled		0.5	250		250		250	μΑ
		Outputs enabled			1.5		1.5		1.5	mA
Δί <sub>CC</sub> ¶	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND	Outputs disabled			50		50		50	μА
	Care inputs at 400 of dist	Control inputs			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		4						pF	
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>9</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

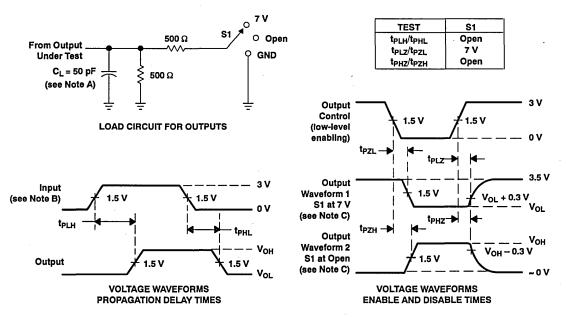
This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT828		SN74ABT828	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	Y	1.1	3	4.4	1.1		1.1	4.8	ns
t <sub>PHL</sub>			1.1	2.9	4.1	1.1		1.1	4.7	
t <sub>PZH</sub>	ŌĒ		1.6	3.7	5.1	1.6		1.6	5.9	20
t <sub>PZL</sub>	05	Ť	2.6	4.6	5.9	2.6		2.6	6.9	ns
t <sub>PHZ</sub>	OE	DE V	2	4.8	6.3	2		2	6.8	ns
t <sub>PLZ</sub>	05	T	2.5	5.1	6.6	2.5		2.5	6.9	

# PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

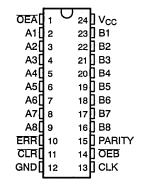
D3781, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Parity Error Flag With Parity Generator/Checker
- Register for Storage of the Parity Error Flag
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mll DIPs

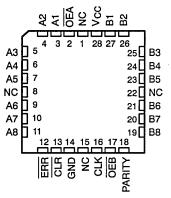
# description

The 'ABT833 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (ERR) output indicates whether or not an error in the B data has occurred. The output-enable (OEA and OEB) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT833 provides true data at its outputs.

SN54ABT833 . . . JT PACKAGE SN74ABT833 . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT833...FK PACKAGE (TOP VIEW)



NC - No internal connection

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the ERR flag. The parity-error output is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear (CLR) input. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT833 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT833 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT833 is characterized for operation from -40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



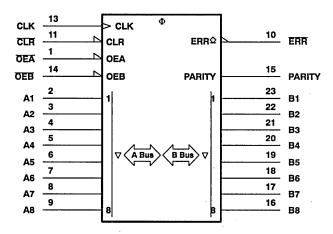
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FU				

			INPUTS				OUTP	UT AND I/O		
OEB	ŌĒĀ	CLR	CLK	Al Σ OF H's	Bi <sup>†</sup> Σ OF H's	А	В	PARITY	ERR‡	FUNCTION
L	Н	х	x	Odd Even	NA	NA	Α.	L H	NA	A data to B bus and generate parity
н	L	н	t	NA	Odd Even	В	NA	NA	H L	B data to A bus and check parity
Х	Х	L.	Х	Х	Х	Х	NA	NA	Н	Check error flag register
н	Н	H L H H	No† No† † †	X X Odd Even	×	z	z	z	NC H H L	Isolation <sup>§</sup>
L	L	х	х	Odd Even	NA	NA	Α	H	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

# logic symbol¶



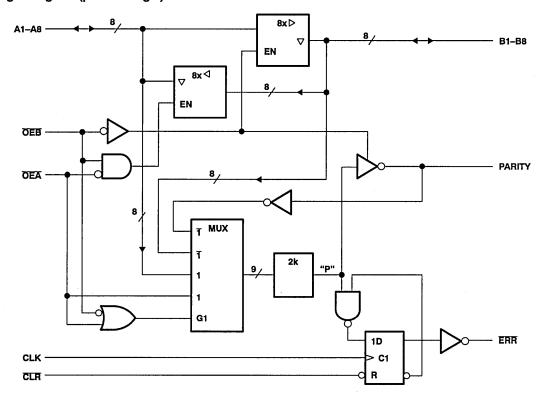
This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

<sup>†</sup> Summation of high-level inputs includes PARITY along with Bi inputs.

<sup>&</sup>lt;sup>‡</sup> Output states shown assume the ERR output was previously high.

<sup>§</sup> In this mode, the ERR output (when clocked) shows inverted parity of the A bus.

# logic diagram (positive logic)



### **ERROR FLAG FUNCTION TABLE**

INP	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
CLR	CLK	POINT "P"	ERR <sub>n-1</sub> †	Enn	
Н	1	Н	Н	Н	
н	1	×	L	Ľ	Sample
Н	1	L	x	L	
L	Х	Х	Х	Н	Clear

<sup>†</sup> The state of the ERR output before any changes at CLR, CLK, or point "P".

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# ERR H DEB H L H CEVEN COLK Tephil Teph

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

• • • • • • • • • • • • • • • • • • • •	•
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$\dots$ -0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT833	96 mA
SN74ABT833	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



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# recommended operating conditions (see Note 2)

			SN54AI	SN54ABT833		SN74ABT833	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		٧
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vi	Input voltage		0	Vcc	0	Vcc	V
VoH	High-level output voltage	ERR		5.5		5.5	V
loн	High-level output current			-24		-32	mA
loL	Low-level output current	Except ERR		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T	A = 25°(	2	SN54ABT833		SN74ABT833		UNIT
PARAMETER	"	EST CONDITION	13	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	וואט
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>i</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V <sub>OH</sub>	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$	All outputs	3			3		3		l <sub>v</sub>
VOH	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA	except ERR	2			2				ľ
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA		2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA				0.55		0.55			v
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	ľ
loн	$V_{CC} = 4.5 \text{ V},$	V <sub>OH</sub> = 5.5 V	ERR								μА
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА
ч	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΛ
Ę	V <sub>CC</sub> = 0 V,	V <sub>I</sub> ≃ GND	A or B ports			-50		-50		-50	μA
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	•	50		50	μA
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μA
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$ V	,			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μA
lcc	l <sub>O</sub> = 0,	A or B ports	Outputs low		24	30		30		30	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μΑ
A1#	$V_{CC} = 5.5 \text{ V},$	One input at 3.4	V,			50		50		50	4
Δl <sub>CC</sub> #	Other inputs at V <sub>CC</sub> or GND				50		50		50	μΑ	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs								pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 \	/	A or B ports								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

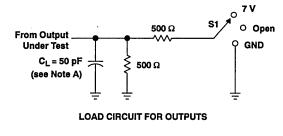
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C				SN74ABT833		UNIT
1			MIN	MIN MAX		MAX	MIN	MAX	
		CLK high							ns
tw	t <sub>w</sub> Pulse duration	CLK low	3		3		3		
		CLR low	3		3		3		
	Cotus time before CLIVA	A port							
t <sub>su</sub> Set	Setup time before CLK†	CLR							ns
t <sub>h</sub>	Hold time after CLK†	A port							ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	SN54ABT833	SN74ABT833	UNIT
t <sub>PLH</sub>						
t <sub>PHL</sub>	A or B	B or A				ns
t <sub>PZH</sub>	ŌĒ	A or B				ns
t <sub>PZL</sub>	OE.	AOIB				115
t <sub>PHZ</sub>	ŌE	A or B				ns
t <sub>PLZ</sub>	02	AGIB				113
t <sub>PLH</sub>	A or OE	PARITY				ns
t <sub>PHL</sub>	AGIGE	I Allii				113
t <sub>PLH</sub>	CLR	ERR	4.4		5.2	ns
t <sub>PHL</sub>	CLK	]	5.7		6.2	113

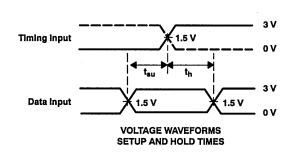


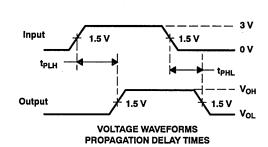
# PARAMETER MEASUREMENT INFORMATION

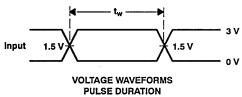


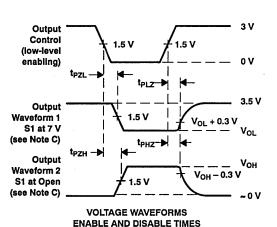
TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	7 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	Open

ERR	S1
t <sub>PHL</sub> (see Note E)	Open
t <sub>PLH</sub> (see Note F)	7 V









NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t<sub>PHL</sub> is measured at 1.5 V.
- F. tpLH is measured at VoL + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT841, SN74ABT841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3783, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

# description

The 'ABT841 10-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

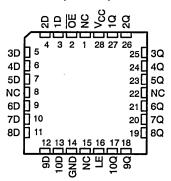
The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT841 ... JT PACKAGE SN74ABT841 ... DB, DW, OR NT PACKAGE (TOP VIEW)

		_	
OE[	<sub>1</sub> U	24	] V <sub>CC</sub>
1D[	2	23	1Q
2D[	3	22	2Q
3D[	4	21	3Q
4D[	5	20	4Q
5D[	6	19	5Q
6D[	7	18	6Q
7D[]	8	17	7Q
8D[]	9	16	8Q
9D[]	10	15	9Q
10D[]	11	14	10Q
GND[]	12	13	LE

SN54ABT841 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT841 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT841 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT841 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

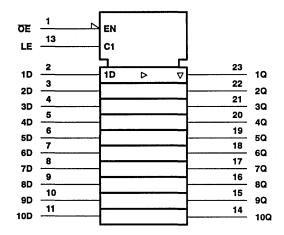


# SN54ABT841, SN74ABT841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS D3783, FEBRUARY 1991-REVISED OCTOBER 1992

					_	_
FU	NC	TIC	N	TA	В	_E

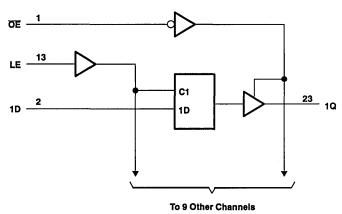
	INPUTS		OUTPUT
OE	LE	D	a
L	Н	Н	Н
L	Н	L	L
L	L	×	Q <sub>0</sub>
Н	Х	Х	z

# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.



# SN54ABT841, SN74ABT841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3783, FEBRUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwi	se noted)†
Supply voltage range, V <sub>CC</sub>	−0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT841	96 mA
SN74ABT841	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	
DW package	
NT package	1.3 W
Storage temperature range –6	5°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# recommended operating conditions (see Note 2)

		SN54#	BT841	SN74A		
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	V
Vi	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
TA	Operating free-air temperature	55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# SN54ABT841, SN74ABT841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3783, FEBRUARY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT COMPLETO	NC	1	A = 25°C	;	SN54A	BT841	SN74A	BT841	LIMIT
PARAMETER	TEST CONDITION	NS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
W	$V_{CC} = 5 \text{ V},  I_{OH} = -3 \text{ mA}$		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		2			2				•
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			٧
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	V
l <sub>j</sub>	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
lozh	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μΑ
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
I <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
I <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V},  V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
lo <sup>§</sup>	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-140	180	-50	-180	-50	-180	mA
	V 55V L 0	Outputs high		1	250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	VI = VCC 01 GIVE	Outputs disabled		0.5	250		250		250	μΑ
	V E E V One input et 2.4 V	Outputs enabled			1.5		1.5		1.5	mA
ΔICC	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND	Outputs disabled			50		50		50	μΑ
	Carlot impace at VCC of GIAB	Control inputs			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V									pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V									рF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> =		SN54AI	BT841	SN74AE	3T841	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high or low		3.8		3.8		3.8		ns
	Setup time, data before LE↓	High	2.5		2.5		2.5		
t <sub>su</sub>	Setup tillie, data belore LE‡	Low	1.5		1.5		1.5		ns
	Hold time, data after LE↓	High	1.5		1.5		1.5		
t <sub>h</sub>	riola lille, data alter LE‡	Low	1		1		1		ns



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

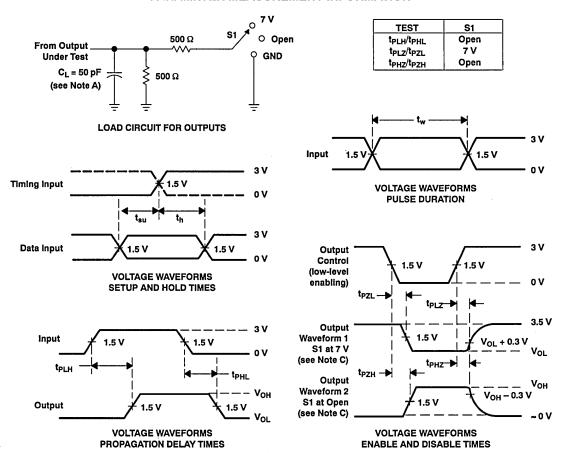
This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT841, SN74ABT841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS D3783, FEBRUARY 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V		SN54A	BT841	SN74A	UNIT	
	( 0.7)	(001/01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	2.1	4.1	5.5	2.1	6.2	2.1	6.2	ns
t <sub>PHL</sub>	]	l u	2	4	5.4	2	6.1	2	6.1	115
t <sub>PLH</sub>	15	LE Q 2.1 4.1 5.8 2.8 4.6 6.2	2.1	6.2	2.1	6.2	ns			
t <sub>PHL</sub>			2.8	4.6	6.2	2.8	6.7	2.8	6.7	115
t <sub>PZH</sub>	OE .	Q	1	3	4.5	1	5.3	1	5.3	ns
t <sub>PZL</sub>		ď	2.2	4.1	5.6	2.2	6.3	2.2	6.3	115
t <sub>PHZ</sub>	ŌĒ	Q	2.7	4.7	6.2	2.7	7.1	2.7	7.1	
t <sub>PLZ</sub>	) UE	ų ,	2.8	4.6	6.1	2.8	6.5	2.8	6.5	ns

# PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5 ns$ ,  $t_f \leq 2.5 ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT843, SN74ABT843 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3784, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

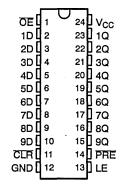
# description

The 'ABT843 9-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

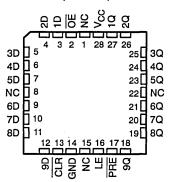
The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT843...JT PACKAGE SN74ABT843...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT843...FK PACKAGE (TOP VIEW)



NC - No internal connection

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



# SN54ABT843, SN74ABT843 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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# description (continued)

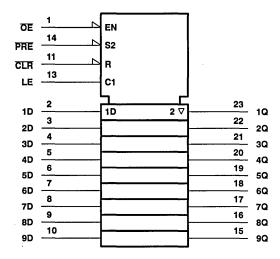
The SN74ABT843 is packaged in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT843 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT843 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

### **FUNCTION TABLE**

		INPUTS			OUTPUT
PRE	CLR	ŌĒ	LE	D	Q
L	Х	L	X	X	Н
Н	L	L	X	X	L
н	Н	L	н	L	L
н	Н	L	Н	Н	н
н	н	L	L	×	Q <sub>0</sub>
×	X	н	X	×	Z

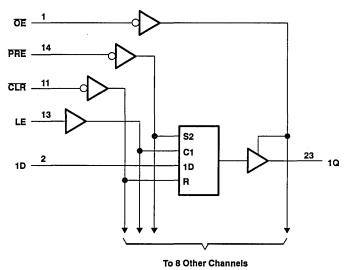
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.



# logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		–0.5 V to 7 V
Input voltage range, VI (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the h	igh state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT843	
,	SN74ABT843	128 mA
Input clamp current, IIK (VI < 0)		–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		–50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in	n still air): DB package	
	DW package	
	NT package	
Storage temperature range		65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Texas VI

# SN54ABT843, SN74ABT843 9-BIT BUS INTERFACE D-TYPE LATCHES **WITH 3-STATE OUTPUTS**

D3784, FEBRUARY 1991-REVISED OCTOBER 1992

# recommended operating conditions (see Note 2)

		SN54	ABT843	SN74AI	BT843	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		8.0		0.8	٧
VI	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEOT CONDITION		T	A = 25°C	;	SN54A	SN54ABT843  MIN MAX  -1.2 2.5 3 2 0.55  ±1 50 -50 -50 -180		BT843	
PARAMETER	TEST CONDITION	NS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>i</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		2			2				v
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA		2‡					2		
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡			1	0.55	٧
11	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μА
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
lozL	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V		-		-50		-50		-50	μΑ
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-140	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high		1	250		250		250	μΑ
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		24	30		30		30	mA
	VI = VCC OF GIVE	Outputs disabled		0.5	250		250		250	μА
Δlcc¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			4						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $<sup>\</sup>P$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

# SN54ABT843, SN74ABT843 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS D3784, FEBRUARY 1991—REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> =		SN54A	BT843	SN74ABT843		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
		CLR low	5.5		5.5		5.5		
t <sub>w</sub>	Pulse duration	PRE low	4.5		4.5		4.5		ns
		LE high	3.3		3.3		3.4		
	Setunding data before LEI	High	2.5	-	2.5		2.5		
t <sub>su</sub>	Setup time, data before LE↓	Low	3		3	5.5 4.5 3.4		ns	
t <sub>h</sub>	Hold time, data after LE↓		0.5		0.5		0.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

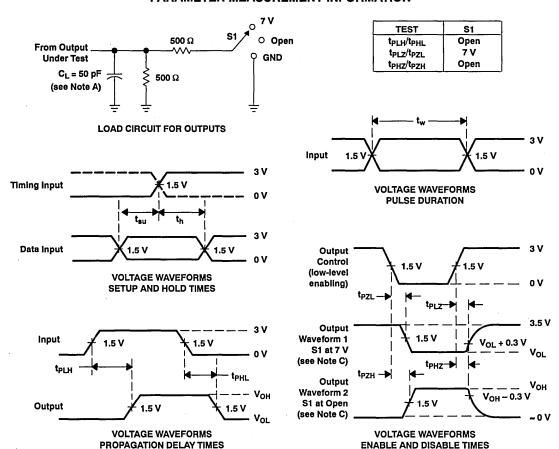
PARAMETER	FROM (INPUT)	TO	TO V <sub>CC</sub> = 5 V, SN54ABT843 SN74 (OUTPUT)		I SN54ABT843 I SN74ABT		BT843	UNIT		
	( 01)	(001101)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	}
t <sub>РLН</sub>	D	a	1.6	3.6	5.2	1.6		1.6	6	ns
t <sub>PHL</sub>		<b>4</b>	2.2	5	6.3	2.2		2.2	7.2	113
t <sub>PLH</sub>	LE		2	4.1	5.6	2		2	6.5	
t <sub>PHL</sub>	LE	Q	2.8	4.8	6.3	2.8		2.8	6.9	ns
t <sub>PLH</sub>	PRE	Q	2.2	4.7	6.2	2.2		2.2	7.4	
t <sub>PHL</sub>	rne	<b>u</b>	3	5.2	6.5	3		3	7.2	ns
t <sub>PLH</sub>	CLR	Q	2.5	5	6.3	2.5		2.5	7.1	
t <sub>PHL</sub>	CLN	<b>"</b>	3.1	5.5	6.8	3.1		3.1	8	ns
t <sub>PZH</sub>	ŌĒ	^	1	2.7	4.2	1		1	5.2	
t <sub>PZL</sub>	OE.	Q	2	4.2	5.5	2		2	6.5	ns
t <sub>PHZ</sub>	ŌĒ	0	2.9	4.9	6.2	2.9		2.9	6.8	
t <sub>PLZ</sub>	OE .	Q	2.2	5	6.3	2.2		2.2	5.7	ns



# SN54ABT843, SN74ABT843 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3784, FEBRUARY 1991-REVISED OCTOBER 1992

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

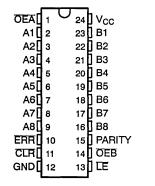
D3786, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>Δ</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Parity Error Flag With Parity Generator/Checker
- Latch for Storage of the Parity Error Flag
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

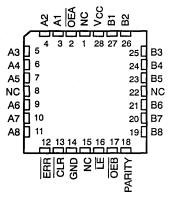
### description

The 'ABT853 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (ERR) output indicates whether or not an error in the B data has occurred. The output-enable (OEA and OEB) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT853 provides true data at its outputs.

SN54ABT853...JT PACKAGE SN74ABT853...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT853...FK PACKAGE (TOP VIEW)



NC - No internal connection

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the ERR flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable (LE) and clear (CLR) control inputs. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT853 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT853 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT853 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



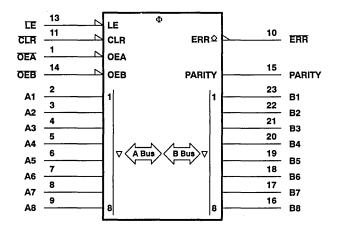
D3786, FEBRUARY 1991-REVISED OCTOBER 1992

NCT	ION	TA	

			INPUTS	1			OUTPL	TS AND I/O	8	
OEB	ÖEA	CLR	LE	Al Σ OF H	BI <sup>†</sup> Σ OF H	Α	В	PARITY	ERR‡	FUNCTION
L	н	х	х	Odd Even	NA	NA	Α	L H	NA	A data to B bus and generate parity
н	L	x	L	NA	Odd Even	В	NA	NA	H L	B data to A bus and check parity
Н	L	Н	Н	NA	X	X	NA	NA	NC	Store error flag
Х	Х	L	Н	X	Х	X	NA	NA	Н	Clear error flag register
н	н	H L	H	X X	×	7	z	z	NC H	Isolation <sup>§</sup>
•	.,	×	L L	L Odd H Even			_	<u>-</u>	H	(parity check)
L	L	х	х	Odd Even	NA	NA	Α	Ĥ	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

# logic symbol<sup>¶</sup>



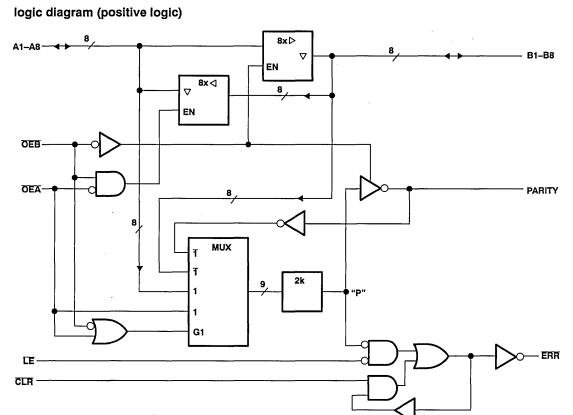
<sup>&</sup>lt;sup>¶</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB; DW, JT, and NT packages.



<sup>†</sup> Summation of high-level inputs includes PARITY along with Bi inputs.

<sup>&</sup>lt;sup>‡</sup> Output states shown assume the ERR output was previously high.

<sup>§</sup> In this mode, the ERR output (when clocked) shows inverted parity of the A bus.

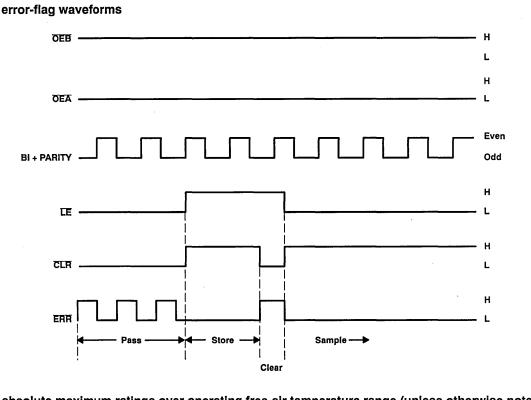


# **ERROR FLAG FUNCTION TABLE**

INPL	JTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	LE	POINT "P"	ERR <sub>n-1</sub> †	Enn	
L	L	L H	L X L		Pass
Н	L	L X H	X L H	L L H	Sample
L	Н	X	Х	Н	Clear
н	н	×	L H	L H	Store

<sup>†</sup> The state of the ERR output before any changes at CLR, LE, or point "P".

D3786, FEBRUARY 1991-REVISED OCTOBER 1992



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $v_{CC}$
nput voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, $V_0 \ldots -0.5  V$ to 5.5 $V$
Current into any output in the low state, Io: SN54ABT853
SN74ABT853
nput clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Dutput clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package
DW package
NT package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



# recommended operating conditions (see Note 2)

			SN54A	BT853	SN74A	LINUT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	,	4.5	5.5	4.5	5.5	
VIH	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
V <sub>OH</sub>	High-level output voltage	ERR		5.5		5.5	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current	Except ERR		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	_	EST CONDITION	10	T	A = 25°(		SN54ABT853		SN74ABT853		UNIT
PARAMETER	''	EST CONDITION	15	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
V <sub>ОН</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$	All outputs	3			3		3		v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> =24 mA	except ERR	2			2				
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> =32 mA		2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
Іон	$V_{CC} = 4.5 \text{ V},$	V <sub>OH</sub> = 5.5 V	ERR								μA
1.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА
l <sub>l</sub>	$V_I = V_{CC}$ or GND		A or B ports			±100		±100		±100	μ.
I <sub>IL</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> = GND	A or B ports			-50		-50		-50	μA
l <sub>OZH</sub> §	$V_{CC} = 5.5 \text{ V},$	V <sub>0</sub> = 2.7 V				50		50		50	μA
l <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$ V	,			±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μA
lo <sup>1</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mΑ
	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μA
lcc	I <sub>O</sub> = 0,	A or B ports	Outputs low		24	30		30		30	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	,	Outputs disabled		0.5	250		250		250	μΑ
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,					50		50		50	μА
	Other inputs at V <sub>CC</sub> or GND							-			<u> </u>
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs								pF
Cio	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	/	A or B ports	L							pF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

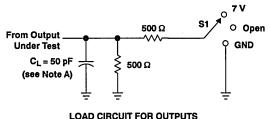
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

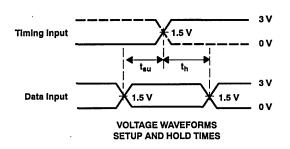
### PARAMETER MEASUREMENT INFORMATION

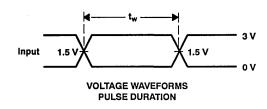


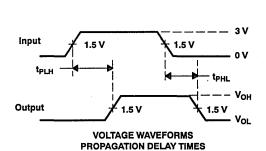
S1
Open
7 V
Open

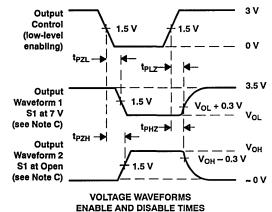
ERR	S1
t <sub>PHL</sub> (see Note E)	Open
t <sub>PLH</sub> (see Note F)	7 V











NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_t \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t<sub>PHL</sub> is measured at 1.5 V.
- F. tpLH is measured at VoL + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms



# SN54ABT861, SN74ABT861 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3788, FEBRUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

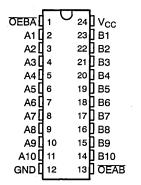
# description

The 'ABT861 is a 10-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

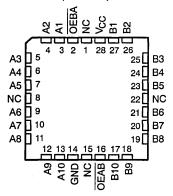
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT861 . . . JT PACKAGE SN74ABT861 . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT861 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT861 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT861 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT861 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

### **FUNCTION TABLE**

INP	UTS	OPERATION
OEAB	OEBA	OPERATION
L	Н	A data to B bus
Н	L	B data to A bus
Н	Н	Isolation
L	L	Latch A and B (A = B)

EPIC-IIB is a trademark of Texas Instruments Incorporated.



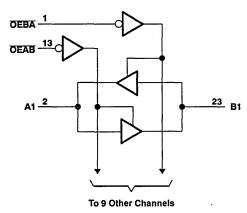
# SN54ABT861, SN74ABT861 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3788, FEBRUARY 1991-REVISED OCTOBER 1992

# logic symbol†

### EN1 **OEAB** EN2 23 В1 2∇ 22 **B2** A2 21 АЗ **B3** 20 A4 **B4** 19 Α5 **B**5 18 **B**6 A6 17 8 **B7 A7** 16 **B8 8A** 15 **A9 B9** 11 14 **B10**

# logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, v <sub>CC</sub>	–0.5 V to / V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or pow	ver-off state, V <sub>O</sub> 0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT861	96 mA
SN74ABT861	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB p	ackage 0.5 W
DW	backage1 W
NT p	ackage 1.3 W
Storage temperature range	–65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT861, SN74ABT861 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3788, FEBRUARY 1991-REVISED OCTOBER 1992

# recommended operating conditions (see Note 2)

			SN54A	BT861	SN74A	UNIT	
	•		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		٧
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vi	Input voltage		0	Vcc	0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ပဲ

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Voh  Vol  I <sub>1</sub> Iozh <sup>§</sup> IozL <sup>§</sup> Ioff  Icex  Iof	TEST CONDITIONS			1	A = 25°C	;	SN54ABT861		SN74ABT861		
PAHAMETER	.	SI CONDITION	15	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		l v
∨он	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> =24 mA		2			2				1 °
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA		2‡					2		1
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	1 _ v
I.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА
4	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ.
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	$V_{CC} = 0 V$ ,	$V_1$ or $V_0 \le 4.5$	V			±100				±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μА
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low		24	30		30		30	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μА
	V <sub>CC</sub> = 5.5 V,	Data inputs	Outputs enabled			1.5		1.5		1.5	
ΔI <sub>CC</sub> #	One input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
Δl <sub>CC</sub> #	V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5	1
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		7						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

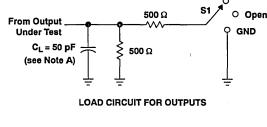
 $<sup>\</sup>mbox{\$}$  The parameters  $\mbox{I}_{\mbox{OZH}}$  and  $\mbox{I}_{\mbox{OZL}}$  include the input leakage current.

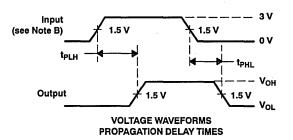
<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

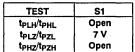
<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

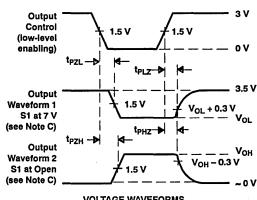
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT861		SN74ABT861		UNIT
	(		MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
t <sub>PLH</sub>	A or B	B or A	1.1	3.4	4.9	1.1		1.1	5.2	ns
t <sub>PHL</sub>			1	3.2	4.4	1		1	4.9	
t <sub>PZH</sub>	OEAB or OEBA	B or A	1.2	3.5	5	1.2	-	1.2	5.9	ns
tpZL	OEAB OF CEBA		2.4	4.6	6	2.4		2.4	6.9	
t <sub>PHZ</sub>	OEAB or OEBA	B or A	3.1	5.3	6.5	3.1		3.1	7.5	ns
t <sub>PLZ</sub>			3.7	5.3	6.6	3.7		3.7	7.1	

# PARAMETER MEASUREMENT INFORMATION









**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES** 

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_r \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

#### SN54ABT862, SN74ABT862 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB "BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

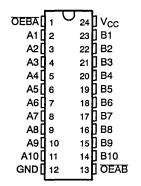
#### description

The 'ABT862 is a 10-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

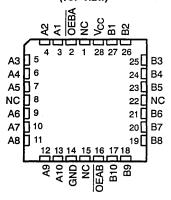
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT862...JT PACKAGE SN74ABT862...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT862 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT862 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT862 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT862 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

#### **FUNCTION TABLE**

INP	UTS	OPERATION
OEAB	OEBA	OPERATION
L	Н	A data to B bus
Н	L	B data to A bus
Н	н	Isolation
L	L	Latch A and B $(A = \overline{B})$

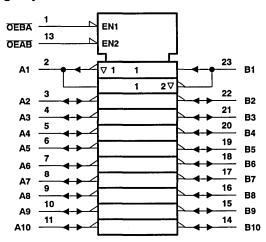
EPIC-IIB is a trademark of Texas Instruments Incorporated.



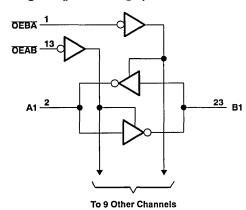
#### SN54ABT862, SN74ABT862 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1992

#### logic symbol†



#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

٠	upply voltage range, V <sub>CC</sub> –0.5 V to 7 V
١	put voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
١	oltage range applied to any output in the high state or power-off state, $V_0$ $-0.5$ V to 5.5 V
(	urrent into any output in the low state, Io: SN54ABT862
	SN74ABT862
1	put clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
(	utput clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
١	aximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
	DW package 1 W
	NT package
9	torage temperature range

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### recommended operating conditions (see Note 2)

			SN54A	BT862	SN74A	TINU	
1			MIN	MAX	MIN	MAX	וואט
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT862		SN74ABT862		UNIT
PARAMETER	15	1EST CONDITIONS			TYP	MAX	MIN	MAX	MIN	MAX	UNII
Vik	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA	=-18 mA			-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				v
	V <sub>CC</sub> = 4.5 V,	$l_{OH} = -32 \text{ mA}$		2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55	1	0.55			· V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	v
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	^
t <sub>i.</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND					±100		±100		±100	μΑ
l <sub>OZH</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$				50		50		50	μА	
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 0.5 V$				-50		-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 5.5 V	Outputs high			50		50		50	μA
lo <sup>¶</sup>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μА
lcc	l <sub>O</sub> = 0,	A or B ports	Outputs low		24	30		30		30	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data insute	Outputs enabled			1.5		1.5		1.5	
Δl <sub>CC</sub> #	One input at 3.4 V, Data Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control inputs			1.5		1.5	,	1.5		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs			4						pF	
Cio	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		A or B ports		7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

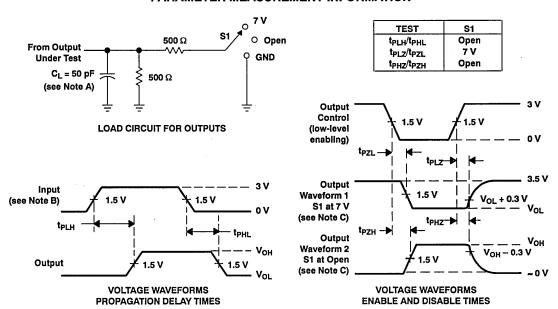
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54ABT863, SN74ABT863 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3789, FEBRUARY 1991-REVISED OCTOBER 1992

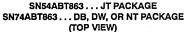
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

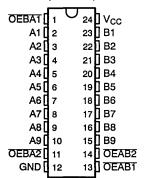
#### description

The 'ABT863 is a 9-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

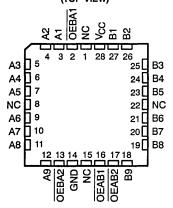
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.





SN54ABT863 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT863 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT863 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT863 is characterized for operation from  $-40^{\circ}$ C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



#### **FUNCTION TABLE**

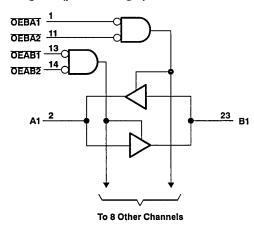
	INP	OPERATION		
OEAB1	OEAB2	<b>OEBA1</b>	OEBA2	OPERATION
L	L	L	L	Latch A and B
L	L	Н	X	A to B
L	L	X	Н	A 10 B
Н	Х	Ĺ	Ĺ	B to A
Х	Н	L	L	BIOA
Н	Х	Н	Х	
н	X	X	Н	Isolation
×	Н	X	Н	isolation
х	Н	Н	Х	

#### logic symbol†

PRODUCT PREVIEW

#### **OEBA1** EN1 11 **OEBA2** 13 **OEAB1** EN2 **OEAB2** A1 **⊽** 1 В1 1 1 2 ▽ 22 A2 **B2** 21 АЗ **B3** 20 A4 В4 19 **B**5 Α5 18 **B**6 A6 8 17 Α7 **B7** 9 16 **A8 B**8 10 15 A9 **B9**

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub> −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT863
SN74ABT863
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
DW package
NT package 1.3 W
Storage temperature range –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54A	BT863	SN74A	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	V
I <sub>OH</sub>	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T <sub>A</sub>	Operating free-air temperature	-	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



#### SN54ABT863, SN74ABT863 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3789, FEBRUARY 1991-REVISED OCTOBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT863		SN74ABT863		UNIT
PARAMETER				MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>j</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2			2				ľ
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$		2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55	i	0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	· •
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
l <sub>i</sub>	$V_I = V_{CC}$ or GND A or B ports				±100		±100		±100	μΑ	
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_I \text{ or } V_O \le 4.5$	V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	1	Outputs high		1	250		250		250	μА
lcc	$I_{O} = 0$ ,	A or B ports	Outputs low		24	30		30		30	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,		Outputs enabled			1.5		1.5		1.5	
Δl <sub>CC</sub> #	One input at 3.4 V, Data inputs Other inputs at	Outputs disabled			0.05		0.05		0.05	mA	
	V <sub>CC</sub> or GND	Control inputs	l inputs			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	' <sub>I</sub> = 2.5 V or 0.5 V Control inputs		_	4		İ				pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		7						рF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT863		SN74ABT863		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
t <sub>PLH</sub>	A or B	B or A	1.3	3.3	4.9	1.3		1.3	5.3	ns
t <sub>PHL</sub>	1 7015		1.2	3.2	4.4	1.2		1.2	5.2	
t <sub>PZH</sub>	OEAB or OEBA	B or A	1.3	3.7	5	1.3		1.3	6.5	ns
t <sub>PZL</sub>	OEAB OI OEBA		2.2	4.6	6	2.2		2.2	7.3	1 "5
t <sub>PHZ</sub>	OEAB or OEBA	B or A	3	5	6.5	3		3	7.1	
t <sub>PLZ</sub>	OEAD OF OEDA		2.5	4.8	6.6	2.5		2.5	6.8	ns



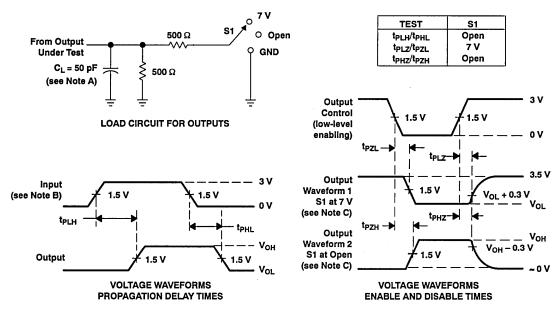
<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>mbox{\$}$  The parameters  $\mbox{I}_{\mbox{\scriptsize OZH}}$  and  $\mbox{I}_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3664, NOVEMBER 1990-REVISED OCTOBER 1992

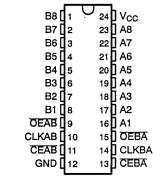
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, B = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

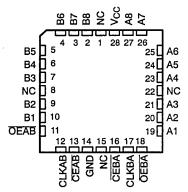
The 'ABT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT2952...JT PACKAGE SN74ABT2952...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT2952 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT2952 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2952 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



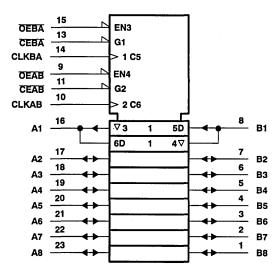
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#### FUNCTION TABLE<sup>†</sup>

	INPUTS					
CEAB	CLKAB	OEAB	Α	В		
Н	Х	L	Х	B <sub>0</sub> ‡		
Х	L	L	X	B <sub>0</sub> ‡		
L	<b>†</b>	L	L	L		
L	<b>†</b>	L	Н	Н		
Х	X	Н	Χ	z		

<sup>&</sup>lt;sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.

#### logic symbol§

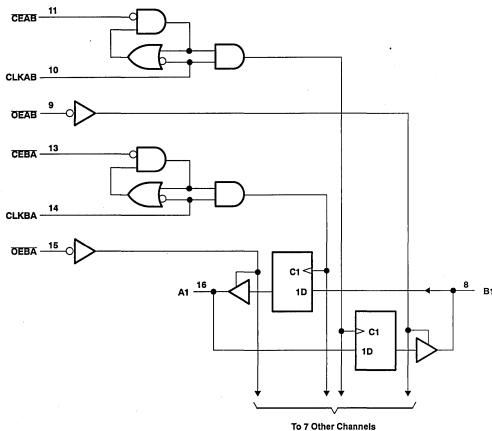


<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

Level of B before the indicated steady-state input conditions were established.

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#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT2952	96 mA
SN74ABT2952	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



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#### recommended operating conditions (see Note 2)

			SN54AE	3T2952	SN74AE	T2952	UNIT
		•	MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	٧
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	40	85	ç

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	75	CT CONDITIO	NC .	T	A = 25°(	-	SN54AE	T2952	SN74AB	T2952	
PARAMETER	"5	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		l v l
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	4	2			. 2				
	V <sub>CC</sub> = 4.5 V,	l <sub>OH</sub> = - 32 m/	4	2‡					2		i i
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 48 mA				0.55		0.55			v
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
l <sub>i</sub>	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
"	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_I$ or $V_O \le 4.5$	5 V			±100				±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	180	mA
<u> </u>	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μΑ
lcc	l <sub>O</sub> = 0,	A or B ports	Outputs low		24	35		35		35	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μА
A1 #	V <sub>CC</sub> = 5.5 V, One in	nput at 3.4 V,				4.5		4.5		4.5	4
∆lcc#	Other inputs at V <sub>C0</sub>	or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3.5						pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	/	A or B ports		7.5						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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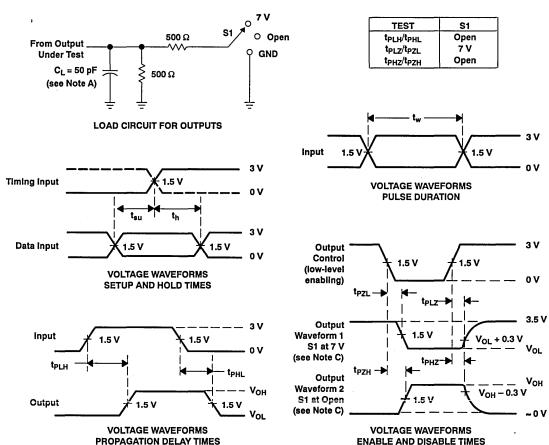
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT2952		SN74ABT2952		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			0	150	0	150	0	150	MHz
	Pulse duration		CLK high	3		3		3		
t <sub>w</sub>	Fulse duration	CLK low	3.5		3.5		3.5		ns	
		A D	High	4		4		4		
	Catura tima hafaya CLICA	A or B	Low	3		3		3		
t <sub>su</sub>	Setup time before CLK†	CE	High	3.5		3.5		3.5		ns
		I CE	Low	2.5		2.5		2.5		
	Lield time offer Oliva	A or B	•	0		0		0		
t <sub>h</sub>	Hold time after CLK↑	CE		0		0		0		ns



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NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \le 2.5$  ns,  $t_f \le 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D4511, AUGUST 1992-REVISED OCTOBER 1992

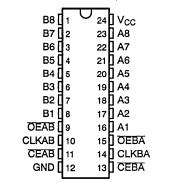
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

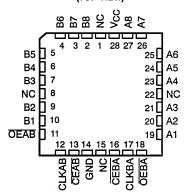
The 'ABT2952A consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT2952A...JT PACKAGE SN74ABT2952A...DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT2952A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT2952A is packaged in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2952A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2952A is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

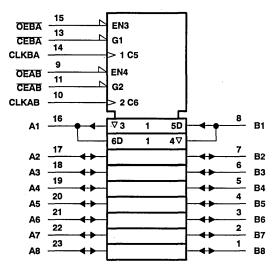
# SN54ABT2952A, SN74ABT2952A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS D4511, AUGUST 1992-REVISED OCTOBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPU	TS		OUTPUT				
CEAB								
Н	Х	L	×	B <sub>0</sub> ‡				
X	L	L	×	В <sub>0</sub> ‡ В <sub>0</sub> ‡				
L	<b>†</b>	L.	L	L				
L	1	L	н	н				
×	Х	Н	X	z				

<sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.

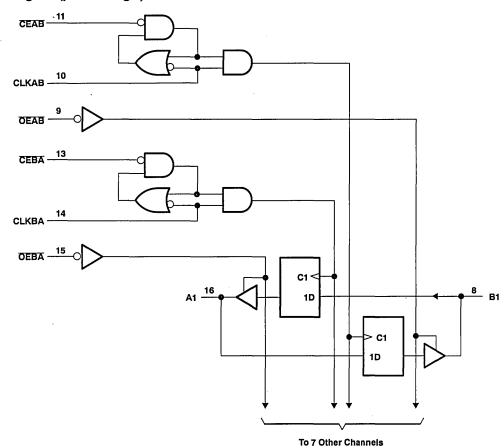
#### logic symbol§



<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

<sup>‡</sup> Level of B before the indicated steady-state input conditions were established.

#### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub> 0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT2952A
SN74ABT2952A
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
DW package
NT package 1.3 W
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



D4511, AUGUST 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T2952A	SN74AB	T2952A	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2	8	2		٧
V <sub>IL</sub>	Low-level input voltage			<i>‰</i> 0.8		0.8	٧
Vı	Input voltage		0,4	<sup>₹</sup> V <sub>CC</sub>	0	Vcc	٧
Іон	High-level output current		<u>,0</u>	-24		-32	mA
loL	Low-level output current		, S	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	185	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		OT COMPLETO	· · · · · · · · · · · · · · · · · · ·	Т	A = 25°0	>	SN54AB1	2952A	SN74AB	T2952A	UNIT
PARAMETER	'E	ST CONDITIO	NS.	MIN	TYP	MAX	MIN	MAX	MIN	MAX	וואט
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	4	2			2				
l	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	4	2‡					2		1
.,	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA		******		0.55 <sup>‡</sup>		43		0.55	
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		₹41		±1	
h .	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		<u>∜</u> 4100		±100	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	,4			50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	Ų.	50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	S V			±100	S) St			±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	ŖŸ	50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	~50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	1	Outputs high		1	250		250		250	μΑ
lcc	I <sub>O</sub> = 0,	A or B ports	Outputs low		24	35		35		35	mA
İ	$V_i = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μA
A1 #	V <sub>CC</sub> = 5.5 V, One ir	put at 3.4 V,				4.5		4.5		4.5	
Δl <sub>CC</sub> #	Other inputs at V <sub>CC</sub>	or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3.5						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		7.5						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

2-230

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

### SN54ABT2952A, SN74ABT2952A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS D4511, AUGUST 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

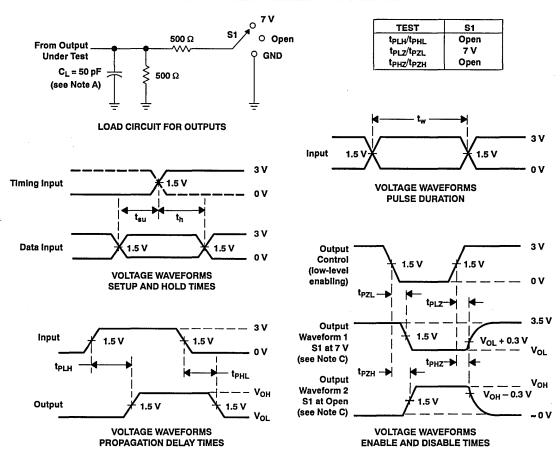
					V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		2952A	SN74ABT2952A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			0	150	۸0	150	0	150	MHz
t <sub>w</sub>	Pulse duration		CLK high or low	3.3		3.30	. Z-	3.3		ns
	Cabus time before CLVA	A or B	High or low	2.5		29.5	9	2.5		
t <sub>su</sub>	Setup time before CLK†	CE	High or low	3		85.3%		3		ns
	Lield time offer CLIVA	A or B		1.5		1.5		1.5		
t <sub>h</sub>	Hold time after CLK↑	CE		2		2		2		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT2952A		SN74ABT2952A		UNIT
	( 0.)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	2	3.3	5.2	26	6.3	2	5.9	ns
t <sub>PHL</sub>	T CLIVAB OF CLIVBA		2.5	4	6.1	2,5	6.8	2.5	6.3	113
t <sub>PZH</sub>	OEBA or OEAB	A or B	1.5	3.2	4.7	(1:50)	5.7	1.5	5.6	
t <sub>PZL</sub>	T CEBA OF CEAB	A or B	2	3.7	5.7	4 €.	6.7	2	6.6	ns
t <sub>PHZ</sub>	OEBA or OEAB	A or B	1.5	3.5	5.1	1.5	6.5	1.5	6.4	
t <sub>PLZ</sub>	T DEBA OF DEAB		1.5	3.4	5.9	1.5	6.7	1.5	6.2	ns

D4511, AUGUST 1992-REVISED OCTOBER 1992





NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3790, FEBRUARY 1991-REVISED OCTOBER 1992

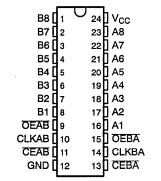
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Inverting Outputs
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

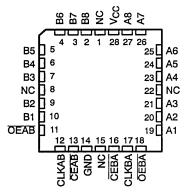
The 'ABT2953 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT2953 . . . JT PACKAGE SN74ABT2953 . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT2953...FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN74ABT2953 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2953 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT2953 is characterized for operation from -40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



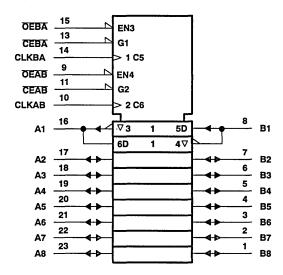
D3790, FEBRUARY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPU	TS		OUTPUT
CEAB	CLKAB	В		
Н	X	L	Х	B₀‡
Х	L	L	×	B <sub>o</sub> ‡
L	<b>†</b>	L	L	н
L	<b>†</b>	L.	Н	L
X	X	Н	Χ	l z

<sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.

#### logic symbol§

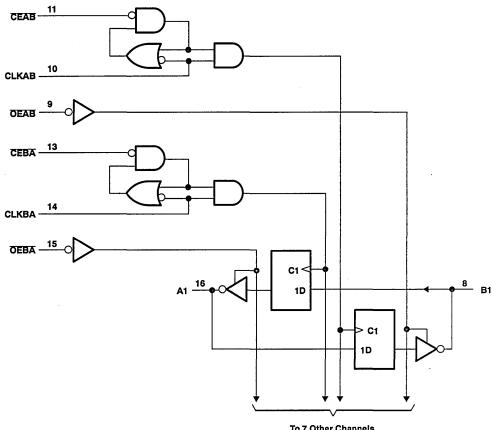


<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

<sup>‡</sup> Level of B before the indicated steady-state input conditions were established.

D3790, FEBRUARY 1991-REVISED OCTOBER 1992

#### logic diagram (positive logic)



To 7 Other Channels

Pin numbers shown are for DB, DW, JT, and NT packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> 0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>
Current into any output in the low state, Io: SN54ABT2953
SN74ABT2953
Input clamp current, $I_{ K }(V_{ } < 0)$
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
DW package 1 W
NT package 1.3 W
Storage temperature range –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



D3790, FEBRUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AE	3T2953	SN74AE	3T2953	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vi	Input voltage	· · · · · · · · · · · · · · · · · · ·	0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	70	ST CONDITIO		T	A = 25°0	;	SN54ABT2953		SN74ABT2953		UNIT
PARAMETER	'5	SI CONDITIO	13	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 3 mA		2.5			2.5		2.5		v
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	\	2			2				
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 64 \text{ mA}$					0.55 <sup>‡</sup>				0.55	
	$V_{CC} = 5.5 V$ , $V_{I} = V_{CC}$ or GND		Control inputs			±1		±1		±1	μА
ıı			A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$					50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_{\rm I}$ or $V_{\rm O} \le 4.5$	5 V			±100				±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
1	$V_{CC} = 5.5 \text{ V},$		Outputs high		1	250		250		250	μА
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		24	35		35		35	mA
	$V_I = V_{CC}$ or GND	V <sub>I</sub> = V <sub>CC</sub> or GND Outp			0.5	250		250		250	μΑ
A1#	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,				1.5		1.5		1.5	mA	
Δlcc#	Other inputs at V <sub>CC</sub> or GND					1.5		1.5		1.5	"'^
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	<i>'</i>	A or B ports		7						pF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>S$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

### SN54ABT2953, SN74ABT2953 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS D3790, FEBRUARY 1991-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

_				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54AE	4ABT2953 SN		SN74ABT2953		
				MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency				150	0	150	0	150	MHz	
t <sub>w</sub>	Pulse duration CLK		CLK high	3		3		3			
	CLK low			3.5		3.5		3.5		ns	
		A or B	High	4		4		4		ns	
			Low	3		3		3			
t <sub>su</sub>	Setup time before CLK†	CE	High	3.5	_	3.5		3.5			
		ICE	Low	2.5		2.5		2.5			
	Hold time after CLK†	A or B	A or B		-	0		0			
th		time after CLK†		0		0		0		ns	

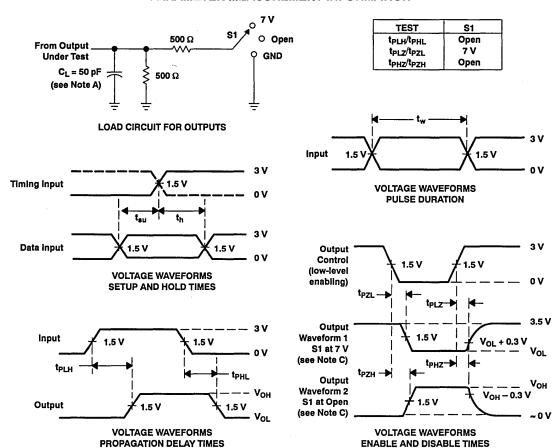
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	l l		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT2953		SN74ABT2953	
	( 0.)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	T		150			150		150		MHz
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2.6	5.1	6.6	2.6		2.6	7.6	ns
t <sub>PHL</sub>	7 CLNDA OI CLNAB		3.2	5.7	7.2	3.2		3.2	8.2	
t <sub>PZH</sub>	OEBA or OEAB	A or B	1	3.3	4.8	1		1	5.8	200
t <sub>PZL</sub>	OEDA OI OEAD	A or B	2.2	4.7	6.2	2.2		2.2	7.5	ns
t <sub>PHZ</sub>	OEBA or OEAB	r OEAB A or B	3.6	6.1	7.6	3.6		3.6	8.1	
t <sub>PLZ</sub>	OEBA OF OEAB		3.1	6.6	7.1	3.1		3.1	7.6	ns



D3790, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\leq}$  10 MHz,  $Z_0 = 50~\Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



General Information	1
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ABT Widebus+™	4.
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ABT 25-Ω Incident-Wave Switching Drivers	6
Futurebus+/BTL Transceivers	7
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#### ABT Widebus™

#### **Features**

- Enhanced AC performance over ABT octals
- JEDEC standard 48-/56-pin SSOP package
- New EIAJ standard Shrink Widebus™ TSSOP package
- Flow-through package pinout organizes all inputs on one side and all outputs on the other side
- Distributed V<sub>CC</sub> and GND pinouts
- Universal bus transceiver (UBT™) architectures
- Hot-card insertion and power-up 3-state circuitry
- TI has established an alternate source

#### Benefits

- Improved propagation delay versus number of outputs switching. Superior pin-to-pin output skew; 15–20% faster speed
- 16, 18, or 20 bits of logic in the same space as that of a typical octal
- 30% board space improvement over SSOP Widebus™ package; meets 1.1-mm height requirements for memory card and other thin applications
- Facilitates easy board layout; pin compatible with popular AC/ACT Widebus™ functions
- Minimized mutual coupling and 2:1 I/O-to-GND rates result in < 0.8-V simultaneous switching noise typically
- Advanced integration, as one UBT<sup>™</sup> can replace nearly all common bus interface logic
- Device protection for end-equipment-specific applications such as telecom
- Standardization that comes from a common product approach

The following table lists ABT Widebus™ devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the General Purpose Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT16265	56	12-Bit to 24-Bit Multiplexed Transceiver
'ABT16471	56	16-Bit Registered Transceiver
'ABT16472	56	18-Bit Registered Transceiver
'ABT16473	56	18-Bit Registered Transceiver
'ABT16474	56	18-Bit Registered Transceiver
'ABT16475	56	18-Bit Registered Transceiver
'ABT16533	48	16-Bit D-Type Latch
'ABT16534	48	16-Bit D-Type Flip-Flop
'ABT16544	56	16-Bit Registered Transceiver
'ABT16620	48	16-Bit Transceiver
'ABT16834	56	16-Bit Registered Transceiver
'ABT16854	56	16-Bit Registered Transceiver
'ABT16861	56	20-Bit Transceiver
'ABT16864	56	18-Bit Transceiver
'ABT16953	56	16-Bit Registered Transceiver

Widebus, Shrink Widebus, and UBT are trademarks of Texas Instruments Incorporated.

#### SN54ABT16240, SN74ABT16240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS095A-D3956, DECEMBER 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical OE (active-low output-enable) inputs.

SN54ABT16240 . . . WD PACKAGE SN74ABT16240 . . . DL PACKAGE (TOP VIEW)

	_			
10E[	1	U	48	] 20E
1Y1	2		47	] 1A1
1Y2[	3			] 1A2
GND[	4		45	] GND
1Y3[	5		44	] 1A3
1Y4[	6		43	] 1A4
V <sub>CC</sub> [	7		42	] v <sub>cc</sub>
2Y1[	8			2A1
2Y2[	9		40	2A2
GND[	10		39	] GND
2Y3[	11		38	] 2A3
2Y4[	12		37	] 2A4
3Y1[	13		36	] 3A1
3Y2[	14		35	] 3A2
GND[	15		34	] GND
3Y3[	16		33	] 3A3
3Y4[	17			] 3A4
V <sub>CC</sub> [	18		31	] v <sub>cc</sub>
4Y1[	19		30	] 4A1
4Y2[	20		29	] 4A2
GND[	21		28	] GND
4Y3[	22			] 4A3
4Y4[	23			] 4A4
40E[	24		25	30E
	ı			ı

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16240 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16240 is characterized for operation from –40°C to 85°C.

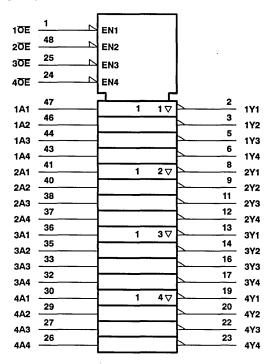
## FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	н
Н	X	Z

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

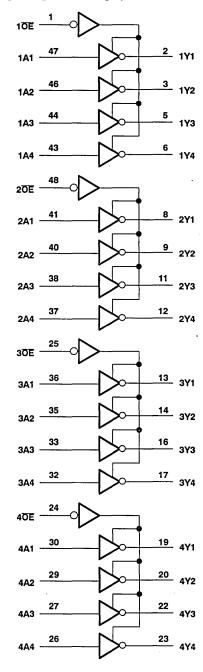


#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### SN54ABT16240, SN74ABT16240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS095A-D3956, DECEMBER 1991-REVISED OCTOBER 1992

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $^\dagger$

–0.5 V to 7 V
0.5 V to 7 V
0.5 V to 5.5 V
96 mA
128 mA
–18 mA
–50 mA
0.85 W
65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54AB	T16240	SN74AB	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	40	85	ů

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### SN54ABT16240, SN74ABT16240 **16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS**

SCBS095A-D3956, DECEMBER 1991-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T <sub>A</sub> = 25°C			T16240	SN74ABT16240		UNIT
PARAMETER	'E	SI CONDIIIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		1 <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				٧
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA			2‡					2		
V-	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA			-	0.55	-	0.55			v
$V_{OL}$	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
1	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or 0			±1		±1		±1	μА	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50		50		50	μА	
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	V <sub>O</sub> = 0.5 V			-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high		·	50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	.,,		Outputs high			2		2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_0 = 0$ ,	Outputs low			32	<del></del>	32	·	32	mA
	1 1 - 100 01 0110		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data la suta	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		1		0.05	mA
	V <sub>CC</sub> or GND	Control input	Control inputs			1.5		1.5		1.5	}
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				7						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 \	/			7						pF

#### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	•		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16240		SN74ABT16240		
	(	(66.1.61.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tpLH	А	^		1	2.7	3.8	1	4.8	1	4.7	
t <sub>PHL</sub>			1.1	3.1	4.3	1.1	4.9	1.1	4.8	ns	
t <sub>PZH</sub>	ŌĒ	Y	1.3	3.3	4.3	1.3	5.4	1.3	5.3	ns	
t <sub>PZL</sub>	OE		1.4	3.4	6.2	1.4	7.2	1.4	7.1		
t <sub>PHZ</sub>	OE Y	1.6	3.6	4.8	1.6	7.2	1.6	6.1			
t <sub>PLZ</sub>		OE Y	1.4	3	5.1	1.4	5.7	1.4	5.6	ns	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

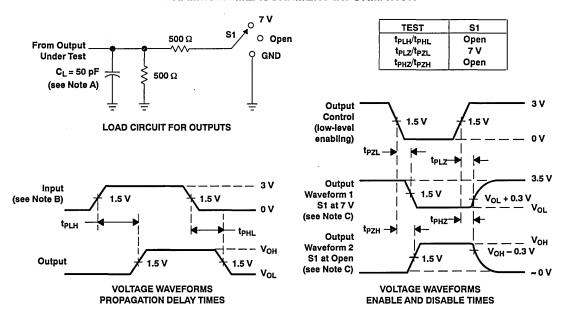
 $<sup>\ ^\</sup>S$  The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS095A-D3956, DECEMBER 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS096A-D3792, FEBRUARY 1991-REVISED OCTOBER 1992

<ul> <li>Members of the Texas Instruments         Widebus ™ Family</li> <li>State-of-the-Art EPIC-IIB ™ BiCMOS Design</li> </ul>	SN54ABT16241 WD PACKAGE SN74ABT16241 DL PACKAGE (TOP VIEW)
Significantly Reduces Power Dissipation	10E[ 1 48] 20E
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce) &lt; 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C</li> </ul>	1Y1 2 47 1A1 1Y2 3 46 1A2
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> <li>Minimizes High-Speed Switching Noise</li> </ul>	GND 4 45 GND 1Y3 5 44 1A3
<ul> <li>Flow-Through Architecture Optimizes PCB Layout</li> </ul>	1Y4[] 6 43]] 1A4 V <sub>CC</sub> [] 7 42]] V <sub>CC</sub>
<ul> <li>High-Drive Outputs (–32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)</li> </ul>	2Y1 8 41 2A1 2Y2 9 40 2A2
Packaged in Plastic 300-mil Shrink	GND 10 39 Q GND
Small-Outline Packages (DL) and 380-mil	2Y3 [] 11
Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings	3Y1 🛛 13 36 🖟 3A1 3Y2 🖟 14 35 🖟 3A2
description	GND 15 34 GND 3Y3 16 33 3A3
The 'ABT16241 is a 16-bit buffer and line driver	3Y3U 16 33U 3A3 3Y4U 17 32U 3A4
designed specifically to improve both the	V <sub>CC</sub> 18 31 V <sub>CC</sub>
performance and density of 3-state memory	4Y1 19 30 4A1
address drivers, clock drivers, and bus-oriented	4Y2[] 20 29[] 4A2
receivers and transmitters. The device can be	GND 21 28 GND
used as four 4-bit buffers, two 8-bit buffers, or one	4Y3 22 27 4A3
16-bit buffer. This device provides true outputs and complementary output-enable (OE and OE) inputs.	4Y4[] 23

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.  $\overline{OE}$  should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16241 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16241 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16241 is characterized for operation from -40°C to 85°C.

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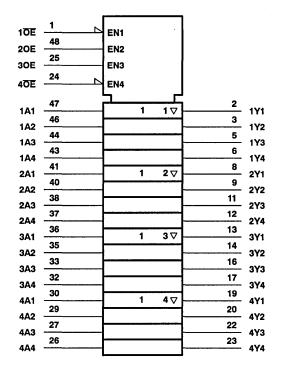
SCBS096A-D3792, FEBRUARY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLES**

INPL	INPUTS						
10E, 40E	1A, 4A	1Y, 4Y					
L	H	Н					
L	L	L					
Н	Х	z					

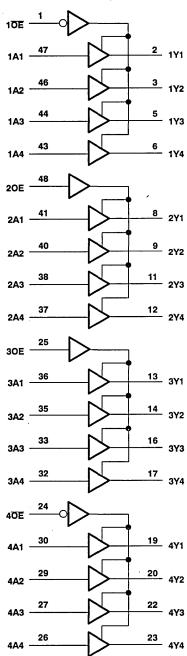
INPL	OUTPUTS	
20E, 30E	2A, 3A	2Y, 3Y
н	Н	H
Н	`L	ļ L
L	X	z

### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



SCBS096A-D3792, FEBRUARY 1991-REVISED OCTOBER 1992

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16241	96 mA
SN74ABT16241	128 mA
Input clamp current, $I_{iK}$ ( $V_1 < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

		-	SN54AB	T16241	SN74AB	UNIT	
l			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA `
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SCBS096A-D3792, FEBRUARY 1991-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			Т	A = 25°0	;	SN54AB	T16241	SN74ABT16241		UNIT
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m.	A	2			2				· •
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 m.	A	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	ľ
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	<sub>C</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1		±1	μА
lozн§	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μΑ	
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μA
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V		Outputs high			2		2		2	
lcc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	I <sub>O</sub> = 0,	Outputs low			32		32		32	mA
	11-1000 01 0115		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Doto inputo	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at		Outputs disabled			0.05		1		0.05	mA
	V <sub>CC</sub> or GND Control inputs		S			1.5		1.5		1.5	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				7						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V	,			7						pF

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			T16241	SN74AB	UNIT	
	(	(001/01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	^		1	2.7	3.4	1	3.8	1	3.7	ns
t <sub>PHL</sub>	1 ^	r	1	2.7	3.9	1	4.6	1	4.5	115
tpzH	OE or OE	~	1.2	3.3	4.2	1.2	5.1	1.2	5	ns
t <sub>PZL</sub>	OE OF OE	, ,	1.3	3.4	5.9	1.3	7	1.3	6.9	115
t <sub>PHZ</sub>	OE or OE		1.5	4.1	5	1.5	7	1.5	6.2	ns
t <sub>PLZ</sub>			1.7	3.6	5.1	1.7	5.7	1.7	5.6	115

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

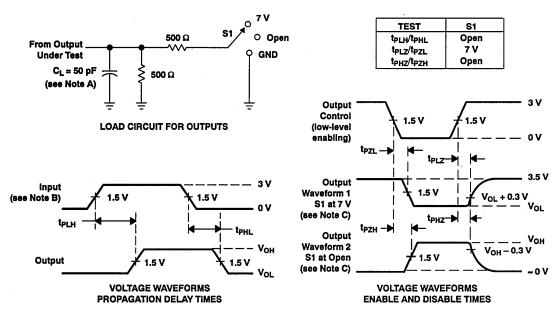
<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $<sup>^{\#}</sup>$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS096A-D3792, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_r \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16244 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical OE (active-low output-enable) inputs.

SN54ABT16244... WD PACKAGE SN74ABT16244... DGG OR DL PACKAGE (TOP VIEW)

	$\overline{}$	
10E[	₁	48 20E
1Y1[	2	47 🛮 1A1
1Y2[	3	46 <b>]</b> ] 1A2
GND[	4	45 ]] GND
1Y3[	5	44 🛛 1A3
1Y4[	6	43 🛭 1A4
Vcc[	7	42]] V <sub>CC</sub>
2Y1 [	8	41 🛮 2A1
2Y2[	9	40 2A2
GND[	10	39 GND
2Y3[	11	38 🛛 2A3
2Y4[]	12	37 🛮 2A4
3Y1 []	13	36 🛭 3A1
3Y2[	14	35 🛛 3A2
GND[	15	34 GND
3Y3[	16	33 🛮 3A3
3Y4[	17	32 🛭 3A4
V <sub>CC</sub> [	18	31 V <sub>CC</sub>
4Y1 🛚	19	30 🛭 4A1
4Y2[]	20	29 🛮 4A2
GND	21	28 GND
4Y3[	22	27 🛮 4A3
4Y4[]	23	26 🛮 4A4
40E[	24	25 3OE

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16244 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16244 is characterized for operation from -40°C to 85°C.

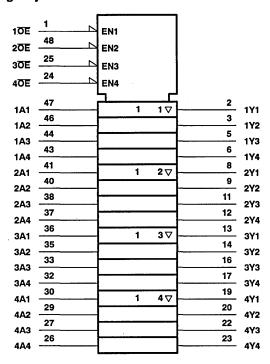
## FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	Н
Н	x	Z

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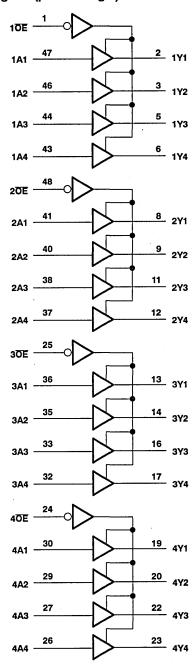
Texas VI

#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub> −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16244
SN74ABT16244
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package
DL package
Storage temperature range —65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

			SN54AB	T16244	SN74AB	T16244	UNIT
ļ			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage	2		2		٧	
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	, 0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	R TEST CONDITIONS			T,	<sub>A</sub> = 25°C	;	SN54AB	T16244	SN74AB	T16244	UNIT
PARAMETER				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>i</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
1 .,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = - 24 m/	A	2			2				<b>V</b>
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m/	Α	2‡					2		
· ·	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	V
l <sub>i</sub>	$V_{CC} = 5.5 \text{ V}$ , $V_{I} = V_{CC} \text{ or } C$		SND			±1		±1		±1	μА
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V					50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
1 <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	50	180	-50	-180	mA
	V 55V		Outputs high			2		2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			32		32		32	mA
	11-1000 01 0113		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data inputa	Outputs enabled			1		1.5		1	· ·
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		.1		0.05	mA
	V <sub>CC</sub> or GND Control inputs		s			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	V <sub>I</sub> = 2.5 V or 0.5 V			7.5						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V	,			7						рF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16244		SN74ABT16244		UNIT	
	(	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	Y	1	2.3	3.2	1	3.6	1	3.5	ns
t <sub>PHL</sub>			1	2.3	3.7	1	4.2	1	4.1	
t <sub>PZH</sub>	OE	Y	1	2.6	3.8	1	4.9	1	4.6	ne
t <sub>PZL</sub>	OE		1	2.9	5.5	1	6.5	1	6.2	ns
t <sub>PHZ</sub>	ŌE	Y	1.7	3.8	4.7	1.7	6	1.7	5.6	ns
t <sub>PLZ</sub>			1.5	3.2	4.7	1.5	5.7	1.5	5.6	

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

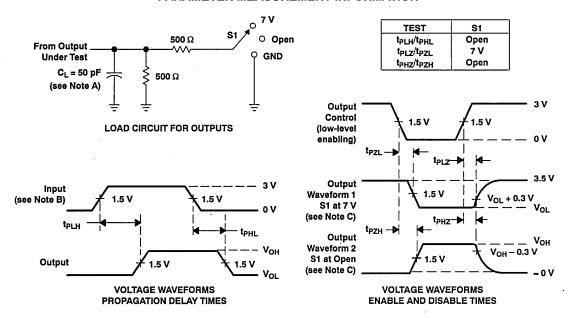
<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT16245, SN74ABT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS084A-D3712, JANUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink
   Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

#### SN54ABT16245... WD PACKAGE SN74ABT16245... DGG OR DL PACKAGE (TOP VIEW)

		_	
1DIR [	₁ ∪	48	] 10E
1B1 [	2	47	] 1A1
1B2 [	3	46	] 1A2
GND [	4		] GND
1B3 [		44	1A3
1B4			] 1A4
V <sub>CC</sub>	7	42	] v <sub>cc</sub>
1B5		41	] 1A5
1B6		40	1A6
GND [			GND
1B7			] 1A7
1B8			1A8
2B1 [			2A1
2B2 [			2A2
GND [		34	GND
2B3 [			2A3
2B4 [	17		2A4
V <sub>CC</sub>	18	31	] v <sub>cc</sub>
2B5 [	19		2A5
2B6			2A6
GND [			GND
2B7 [			2A7
2B8 [			2A8
2DIR [	24	25	20E

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16245 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16245 is characterized for operation from  $-40^{\circ}$ C to 85°C.

## FUNCTION TABLE (each 8-bit section)

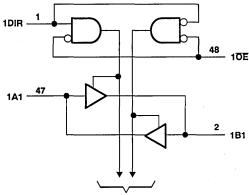
INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

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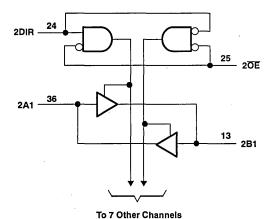
Texas Instruments

#### logic symbol† G3 10E 1DIR 3 EN1 [BA] 3 EN2 [AB] 25 20E G6 24 2DIR 6 EN4 [BA] 6 EN5 [AB] 2 1**B**1 ٥ 2∇ 46 1A2 1B2 44 5 1A3 1B3 43 6 1A4 1**B**4 41 8 1B5 1A5 9 1A6 1**B**6 38 11 1A7 1**B**7 37 12 1A8 1B8 36 13 **▽ 4** 2A1 2B1 ◁ 5▽ Þ 35 14 2A2 2B2 33 16 2A3 2B3 32 17 2A4 2B4 30 19 2A5 2B5 29 20 2A6 2B6 27 22 2A7 2**B**7 26 23 2A8 2B8

logic diagram (positive logic)



To 7 Other Channels



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		. −0.5 V to 7 V
Input voltage range, VI (except I/O ports) (see	Note 1)	. $-0.5 V$ to $7 V$
Voltage range applied to any output in the high	state or power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, Io: SI	N54ABT16245	96 mA
SI	N74ABT16245	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)		50 mA
Maximum power dissipation at $T_A = 55$ °C (in st	till air): DGG package	0.6 W
	DL package	0.85 W
Storage temperature range		-65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



## SN54ABT16245, SN74ABT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS084A-D3712, JANUARY 1991-REVISED OCTOBER 1992

### recommended operating conditions (see Note 2)

			SN54ABT1624		SN74ABT16245		TINU
			MIN	MAX	MIN	MAX	UNII
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	.0	Vcc	V
ГОН	High-level output current		1	-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT16245		SN74ABT16245		UNIT
PARAMETER	"5	TEST CONDITIONS			TYP†	MAX	MIN	MAX	MIN	MAX	O. T.
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA					2.5		2.5		
V <sub>OH</sub>	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3		l <sub>v</sub>
	V <sub>CC</sub> = 4.5 V,	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA					2				1 °
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55	İ		v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	ľ
1.	V <sub>CC</sub> = 5.5 V, Control inputs					±1		±1		±1	μА
l <sub>1</sub>	$V_I = V_{CC}$ or GND				±100		±100		±100	μ.	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	$V_0 = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
lo¶	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$		~50	-100	-180	-50	-180	-50	-180	mA
	$V_{CC} = 5.5 \text{ V},$		Outputs high			2		2		2	
lcc	$I_0 = 0$ ,	A or B ports	Outputs low			32		32		32	mΑ
	$V_I = V_{CC}$ or GND		Outputs disabled			2		, 2		2	
	V <sub>CC</sub> = 5.5 V, One	Data innuta	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		1		0.05	mA
	V <sub>CC</sub> or GND	Control input	s			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	0.5 V Control inputs			3						pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,	A or B ports		8.5		-				pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

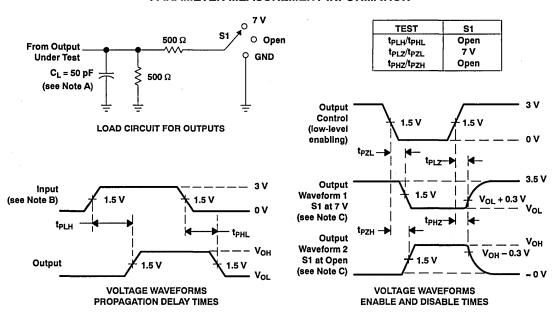
<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS084A-D3712, JANUARY 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16245		SN74ABT16245		UNIT	
	( 0.)	(551.51)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	2.2	3.4	1	4	1	3.9	ns
t <sub>PHL</sub> ·			1	2.1	3.8	1	4.6	1	4.5	
t <sub>PZH</sub>	ŌĒ	B or A	1	3.1	4.4	1	5.5	1	5.4	ns
t <sub>PZL</sub>	OE .		1	3	6.1	1	7.3	1	7.2	1115
t <sub>PHZ</sub>	Œ	B or A	1.3	3.5	4.7	1.3	5.6	1.3	5.5	ns
t <sub>PLZ</sub>			1.4	3.2	4.7	1.4	5.3	1.4	5.2	

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT16260, SN74ABT16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Lavout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

SN54ABT16260...WD PACKAGE SN74ABT16260...DL PACKAGE (TOP VIEW)

	┎	U		L
OEA	1	_	56	OE2B
LE1B	2			LEA2B
2B3	]3		54	]2B4
GND	]4		53	] GND
2B2 (	<b>]</b> 5		52	]2B5
2B1 [	]6		51	]2B6
V <sub>cc</sub> [	<b>1</b> 7		50	]v <sub>cc</sub>
A1 [	8		49	]2B7
A2 [	]9			] 2B8
A3	10			]2B9
GND			46	] GND
A4			45	]2B10
A5			44	]2B11
A6				]2B12
A7	15		42	] 1B12
A8				] 1B11
A9				] 1B10
GND	18			] GND
A10	19			] 1B9
A11 [	20			] 1B8
A12	21		36	] 1B7
Vcc				]v <sub>cc</sub>
1B1 (	23			] 1B6
1B2 (	24		33	] 1B5
GND [	25			] GND
1B3 [	26			] 1B4
LE2B [	27			]LEA1B
SEL[	28		29	OETB

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. These control signals also allow byte control of the most significant byte and least significant byte for each bus.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16260 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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# SN54ABT16260, SN74ABT16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

### description (continued)

The SN54ABT16260 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16260 is characterized for operation from  $-40^{\circ}$ C to 85°C.

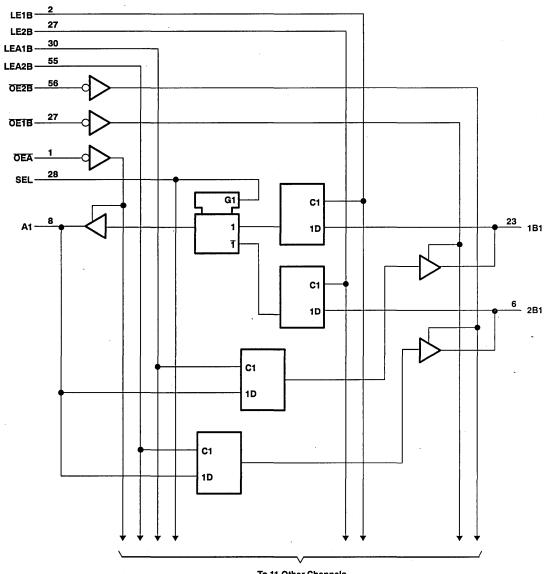
#### **FUNCTION TABLES**

		ОИТРИТ				
1B	2B	SEL	LE1B	LE2B	OEA	Α
Н	Х	Н	Н	Х	L	Н
L	X	Н	н	Х	L	L
X	X	н	L	X	L	Ao
×	Н	L	X	Н	L	Н
x	L	L	X	Н	L	L
x	X	L	X	L	L	A <sub>o</sub>
X	X	Х	Х	Х	Н	z

		INPUTS			OUTI	PUTS
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L	Н	Н	L	L	L	L
ļн	Н	L	L	L	н	2B <sub>0</sub>
L	Н	L	L	L	L	2B <sub>0</sub>
Н	L	Н	L	L	1B <sub>0</sub>	Н
L	L	н	L	L	1B <sub>0</sub>	L
×	L	L	L	L	1B <sub>0</sub>	2B <sub>0</sub>
x	X	X	Н	н	z	Z
x	X	X	L	н	Active	Z
x	Х	х	Н	L	z	Active
×	Х	X	L	L	Active	Active

## logic diagram (positive logic)

401.00



To 11 Other Channels

## SN54ABT16260, SN74ABT16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16260
SN74ABT16260
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

			SN54AB	T16260	SN74ABT16260		UNIT
			MIN	MIN MAX MIN MAX		MAX	
Vcc	Supply voltage		4.5	<b>5</b> .5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2	N.	2		٧
V <sub>IL</sub>	Low-level input voltage			<i>‰</i> 0.8		0.8	٧
V <sub>I</sub>	Input voitage		0,5	₹ v <sub>cc</sub>	0	Vcc	V
Гон	High-level output current		<u>,Q</u>	-24		-32	mA
loL	Low-level output current		S	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S. S.	10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

## SN54ABT16260, SN74ABT16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIO	NC .	Т	A = 25°0	>	SN54AB	T16260	SN74AB	T16260	UNIT	
PANAMETEN	lesi condino	145	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	I ONII	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V.	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5	-		
V	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3		l v	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		2			2				· V	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = - 32 mA		2‡					2			
.,	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡		-		0.55		
	V SEV V V COND	Control inputs			±1		<b>∠</b> 4±1		±1		
lį	$V_{CC} = 5.5 \text{ V},  V_I = V_{CC} \text{ or GND}$	A or B ports			±100		<b>4</b> 100		±100	μΑ	
1	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V	A or B ports				,Q*		100		^	
hold	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V	A or B ports				Ú.	•	-100		μΑ	
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50	Š	50		50	μΑ	
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50	<i>&amp;</i>	-50		-50	μA	
I <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μА	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА	
lo <sup>§</sup>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-100	-225	-50	-225	-50	-225	mA	
	V 55V 1 0	Outputs high			1.5		1.5		1.5		
lcc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			63		63		63	mΑ	
	AT ACC OF CIVE	Outputs disabled			1		1		1		
Δlcc¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			3			-			pF	
Cio	V <sub>O</sub> = 2.5 V or 0.5 V			11.5						pF	

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC} = 5 \text{ V}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	SN54ABT16260	SN74ABT16260	UNIT
Į		MIN MAX	MIN) MAX	MIN MAX	1
t <sub>w</sub>	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3	3.3 🔊	3.3	ns
t <sub>su</sub>	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5	्रा.इट	1.5	ns
t <sub>h</sub>	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1	1	1	ns

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT16260, SN74ABT16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

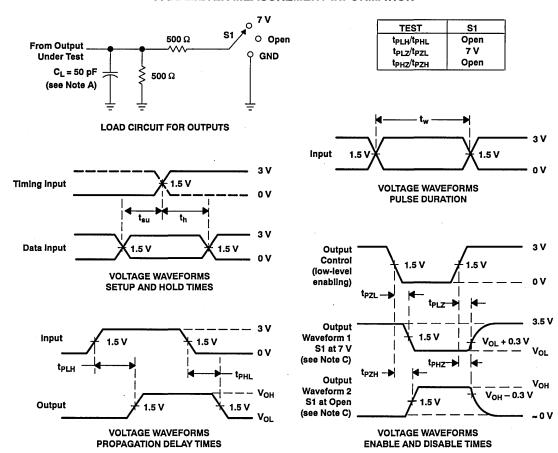
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER FROM (INPUT)		TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54ABT16260		SN74ABT16260		UNIT
	) ( 5.)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	}
tpLH	A or B	B or A	1	3.1	4.8	1	5.9	1	5.6	ns
t <sub>PHL</sub>	1 ^0''	BUIA	1	3.4	5	1	6.3	1	5.9	115
t <sub>PLH</sub>	Œ	A or B	1.1	3.2	4.9	1.1	€,6.6	1.1	5.8	ns
t <sub>PHL</sub>	]	A 01 B	1.1	3.3	4.9	1.1	5.9	1.1	5.3	115
•	SEL (B1)		1.3	3.2	4.6	1.3	₹ 5.4	1.3	5.3	
<sup>t</sup> PLH	SEL (B2)	· A	1.1	3.4	4.9	1.15	6.3	1.1	6	ns
•	SEL (B1)	^	1.5	3.1	4.4	1,3	4.7	1.5	4.4	115
t <sub>PHL</sub>	SEL (B2)		1.6	3.6	5.1	<u>,</u> C1.6	6.2	1.6	5.9	1
t <sub>PZH</sub>	ŌĒ	A or B	. 1	3.3	4.7	Q 1	6.4	1	5.7	
t <sub>PZL</sub>	]	AUID	1.6	3.8	5.1	1.6	6.1	1.6	5.8	ns
t <sub>PHZ</sub>	OE .	A or B	2.2	4.1	5.4	2.2	6.6	2.2	6.4	
t <sub>PLZ</sub>	1	AOIB	1.3	3.2	4.4	1.3	5.4	1.3	4.8	ns



JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

3–32

## SN54ABT16373, SN74ABT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3793, FEBRUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments
  Widebus™ Family
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16373 is a 16-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT16373...WD PACKAGE SN74ABT16373...DL PACKAGE (TOP VIEW)

		П		1
10E [	1	O		] 1LE
1Q1 [				] 1D1
1Q2 [				] 1D2
GND [				GND
1Q3 [				] 1D3
1Q4 [			43	] 1D4
v <sub>cc</sub> [	7		42	] v <sub>cc</sub>
1Q5 [			41	1D5
1Q6 [			40	1D6
GND [			39	GND
1Q7 [			38	] 1D7
1Q8 [				D8 [
2Q1 [				2D1
202				] 2D2
GND [				GND
2Q3 [				2D3
2Q4 [			32	2D4
v <sub>cc</sub> [	18			] v <sub>cc</sub>
2Q5 [	19			2D5
2Q6 [				2D6
GND [				GND
2Q7 [				2D7
2Q8 [				2D8
20E [	24		25	2LE
	_			1

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components

The output enable (OE) does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16373 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16373 is characterized for operation from –40°C to 85°C.

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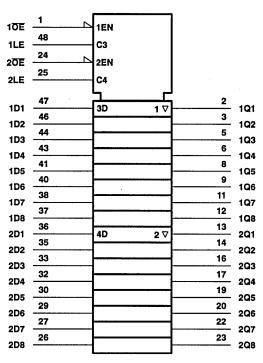


## SN54ABT16373, SN74ABT16373 **16-BIT TRANSPARENT D-TYPE LATCHES** WITH 3-STATE OUTPUTS D3793, FEBRUARY 1991—REVISED OCTOBER 1992

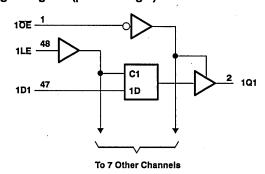
#### **FUNCTION TABLE** (each latch)

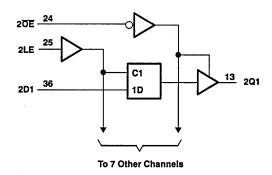
	INPUTS	OUTPUT	
QE	LE	D	a
- L	Н	Н	Н
L	Н	L	L
L	L	X	Q <sub>0</sub>
Н	X	X	z

## logic symbol†



## logic diagram (positive logic)





<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## SN54ABT16373, SN74ABT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3793, FEBRUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub>
Current into any output in the low state, Io: SN54ABT16373
SN74ABT16373
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)
Storage temperature range -65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

				SN54ABT16373		SN74ABT16373	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage			34	2		V
VIL	Low-level input voltage			<i>5</i> ⊈ 0.8		0.8	V
VI	Input voltage		0,4	₹ V <sub>CC</sub>	0	Vcc	V
Гон	High-level output current		T Q	-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate Outputs enabled			10		10	ns/V
TA	Operating free-air temperature			125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## SN54ABT16373, SN74ABT16373 **16-BIT TRANSPARENT D-TYPE LATCHES** WITH 3-STATE OUTPUTS D3793, FEBRUARY 1991-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	75	CT CONDITIO	Ne	T	A = 25°(	2	SN54AB	Г16373	SN74ABT16373		UNIT
PARAMETER	'5	ST CONDITIO	NO .	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		1.2	V
	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA	<b>\</b>	3			3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>OH</sub> = -24 m	A	2			2				ľ
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	A	2‡					2		1
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	1	
1	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = V_{CC} \text{ or GND}$				±1		.31		±1	μΑ	
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		₹50		50	μΑ	
lozL	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		<u>∜</u> –50		-50	μΑ	
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100	_4			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Ç	50		50	μΑ
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	- <del>,</del> 50	-180	50	-180	. mA
			Outputs high			2	Q.F	2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			85	*	85		85	mΑ
	AL - ACC OF CIAD		Outputs disabled			2		2		2	ĺ
ΔI <sub>CC</sub> <sup>N</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3.5						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 \	/			9.5						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

	·		SN54ABT16373	SN74ABT16373	UNIT
L		MIN MAX	MIN (C) MAX	MIN MAX	
t <sub>w</sub>	Pulse duration, LE high	3.3	3,8)* (47	3.3	ns
t <sub>su</sub>	Setup time, data before LE↓	1.5	4.5 G	1.5	ns
t <sub>h</sub>	Hold time, data after LE↓	1	42,	1	ns

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

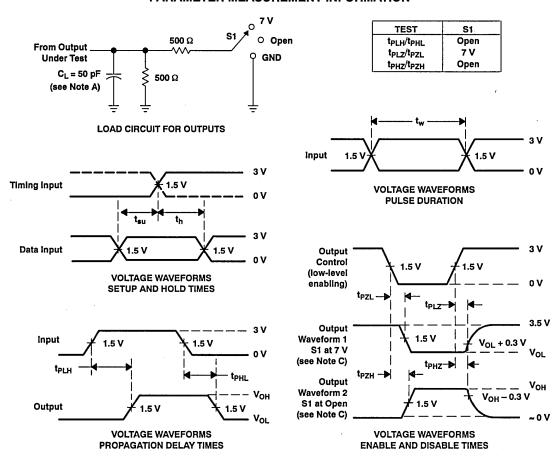
# SN54ABT16373, SN74ABT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS D3793, FEBRUARY 1991—REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	•	<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB1	16373	SN74AB	SN74ABT16373	
	(111701)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	a	1.9	4.1	5.3	1.9	6.5	1.9	6.3	ns
t <sub>PHL</sub>		٧	2.3	4.3	5.4	2.3	₹6.5	2.3	6.2	115
t <sub>PLH</sub>	LE	Q	2.1	4.5	5.7	2.1	7	2.1	6.7	ns
t <sub>PHL</sub>	LE	٧	2.6	4.5	5.6	2.6, 4	6.3	2.6	6.1	115
t <sub>PZH</sub>	OE .	Q	1.5	3.9	5	1.5	6.4	1.5	6.1	
t <sub>PZL</sub>	]	<u> </u>	1.8	3.8	4.9	4)8	5.8	1.8	5.6	ns
t <sub>PHZ</sub>	OE .	Q	2.4	6.5	8.8	₹2.4	10.8	2.4	10.3	no
t <sub>PLZ</sub>	OE	ų u	2.3	5.3	7.6	<b>2.3</b>	8.7	2.3	8.1	ns

D3793, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



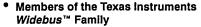
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT16374, SN74ABT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3855, APRIL 1991-REVISED OCTOBER 1992



- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Lavout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54ABT16374... WD PACKAGE SN74ABT16374... DL PACKAGE (TOP VIEW)

		1 1		1
10E		U	48	1CLK
1Q1			47	] 1D1
1Q2				] 1D2
GND				GND
1Q3				[] 1D3
1Q4				] 1D4
Vcc			42	2 v <sub>cc</sub>
1Q5			41	D5 1D5
1Q6			40	1D5 1D6
GND			39	∐ GND
1Q7			38	D7
1Q8			37	D8 1D8
2Q1			36	2D1
2Q2	14		35	2D2
GND			34	GND
2Q3			33	2D3
2Q4			32	] 2D4
Vcc	18			] v <sub>cc</sub>
2Q5			30	2D5
2Q6			29	2D6
GND			28	GND
2Q7				2D7
2Q8				2D8
20E	24		25	2CLK
				ı

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components

The output enable (OE) does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16374 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16374 is characterized for operation from –40°C to 85°C.

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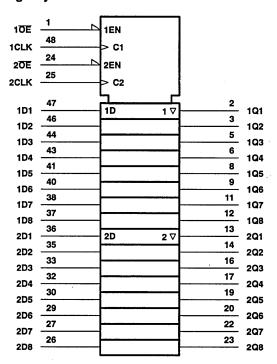
## SN54ABT16374, SN74ABT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3855, APRIL 1991-REVISED OCTOBER 1992

## FUNCTION TABLE (each flip-flop)

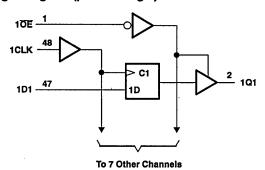
	INPUTS	OUTPUT	
ŌĒ	CLK	D	a
L	Ť	Н	Н
L	Ť	L	L
L	L	X	Q <sub>0</sub>
н	X	X	z

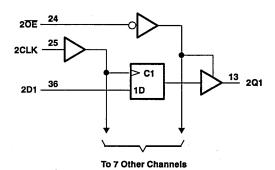
## logic symbol†



## <sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)





D3855, APRIL 1991-REVISED OCTOBER 1992

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7	' V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7	' V
Voltage range applied to any output in the high state or power-off state, Vo		
Current into any output in the low state, Io: SN54ABT16374	96 n	nΑ
SN74ABT16374	128 n	nΑ
Input clamp current, $I_{IK}(V_I < 0)$	–18 n	nΑ
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	50 n	nΑ
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85	W
Storage temperature range	-65°C to 150	°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54AB	SN54ABT16374		SN74ABT16374	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage			5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage			37	2		V
VIL	Low-level input voltage			<i>‰</i> 0.8		0.8	V
Vı	Input voltage			<sup>₹</sup> V <sub>CC</sub>	0	V <sub>CC</sub>	٧
IOH	High-level output current .			-24		-32	mA
loL	Low-level output current		1 20	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	55	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## SN54ABT16374, SN74ABT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3855, APRIL 1991-REVISED OCTOBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

BARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54ABT16374		SN74ABT16374		UNIT			
PARAMETER			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII			
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18$	mA			-1.2		-1.2		-1.2	V			
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -	3 mA	2.5			2.5		2.5					
V	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$					3		3		l <sub>v</sub> l			
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA					2				· •			
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -	32 mA	2‡					2		1			
V	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 48$	3 mA			0.55		0.55			V			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55				
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V}, \qquad V_I = V_{CC} \text{ or GND}$				±1		1چ. ٠		. ±1	μΑ			
l <sub>ozh</sub>	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7$	/ <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50		≪50		50	μΑ			
lozL	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		<i>‰</i> –50	Ì	-50	μА			
l <sub>OFF</sub>	$V_{CC} = 0 V$ , $V_i \text{ or } V_C$	/, V <sub>1</sub> or V <sub>0</sub> ≤ 4.5 V			±100				±100	μА			
I <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 5.5 \text{ V}$	5 V Outputs high			50	<u>ي</u> رد)	50		50	μА			
lo <sup>§</sup>	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.5 \text{ V}$	5 V	50	-100	-180	-50 -50	-180	-50	-180	mA			
		Outputs high			2	Ş.	2		2	2			
Icc	$V_{CC} = 5.5 \text{ V}, \qquad I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low			67		67		67	mA			
	Outputs disabled				2		2		2				
Δl <sub>CC</sub> <sup>†</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA			
CI	V <sub>I</sub> = 2.5 V or 0.5 V			3.5						pF			
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V			9.5						pF			

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	SN54ABT16374	SN74ABT16374	UNIT	
		MIN MAX	MIN AMAX	MIN MAX		
fclock	Clock frequency	0 150	0 5 ,350	0 150	MHz	
t <sub>w</sub>	Pulse duration, CLK high or low	3.3	3.30	3.3	ns	
t <sub>su</sub>	Setup time, data before CLK↑	1.1	14, 55	1.1	ns	
t <sub>h</sub>	Hold time, data after CLK†	1.3	1.3	1.3	ns	

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

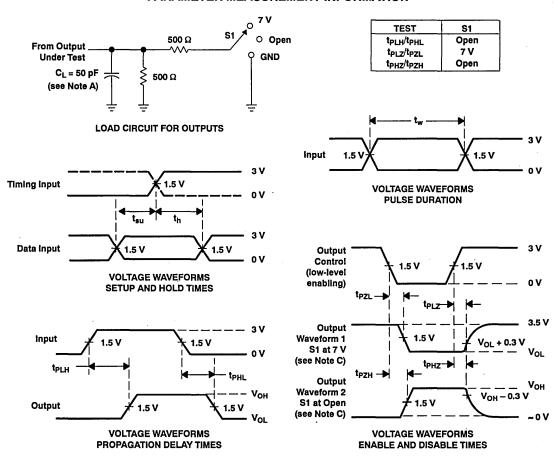
# SN54ABT16374, SN74ABT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS D3855, APRIL 1991—REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM		METER FROM (INPUT)	METER			<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54ABT16374		SN74ABT16374		UNIT
	(intr-01)	(001/01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX				
f <sub>max</sub>			150			150		150		MHz			
t <sub>PLH</sub>	CLK	Q	1.8	4.3	5.4	1.8	∠ 6.4	1.8	6.2	ns			
t <sub>PHL</sub>		"	2.7	4.5	5.6	2.7	<b>%\6.4</b>	2.7	5.9	115			
t <sub>PZH</sub>	ŌĒ	Q	1.4	3.6	4.8	1,0	6.1	1.4	5.7				
t <sub>PZL</sub>	OE.	4	1.7	3.5	4.6	49X4	5.5	1.7	5.3	ns			
t <sub>PHZ</sub>	OE	Q	2.2	5.4	8.4	2.2	10.5	2.2	10				
tpLZ		۱ ۷	2.3	4.6	7.7	2.3	9.8	2.3	8.7	ns			

D3855, APRIL 1991-REVISED OCTOBER 1992

### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

### SN54ABT16377, SN74ABT16377 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

OCTORER 1992

- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

### description

The 'ABT16377 is a 16-bit positive-edge-triggered D-type flip-flop with a clock (1CLK or 2CLK) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

SN54ABT16377...WD PACKAGE SN74ABT16377...DL PACKAGE (TOP VIEW)

_		U		L
1CLKEN		_	48	] 1CLK
1Q1 L	2		47	1D1
	3		46	D2 1D2
GND [				[] GND
1Q3 🏻				] 1D3
1Q4 [				] 1D4
v <sub>cc</sub> [	7			□ v <sub>cc</sub>
1Q5 [				1D5
1Q6 [				1D6
GND [				] GND
1Q7 🛚				D7 []
1Q8 🛚				D8 1
2Q1 [				2D1
2Q2 [			35	2D2
GND [			34	GND
2Q3 [	16		33	2D3
2Q4 [				2D4
v <sub>cc</sub> [			31	□ v <sub>cc</sub>
2Q5 [	19		30	2D5
2Q6 [	20		29	2D6
GND [	21		28	GND
2Q7 [			27	2D7
2Q8 [	23		26	] 2D8
2CLKEN [	24		25	2CLK

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

Data input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable (1CLKEN or 2CLKEN) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at CLKEN.

The SN74ABT16377 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16377 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16377 is characterized for operation from  $-40^{\circ}$ C to 85°C.

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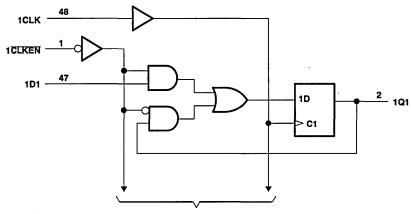


# SN54ABT16377, SN74ABT16377 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS OCTOBER 1992

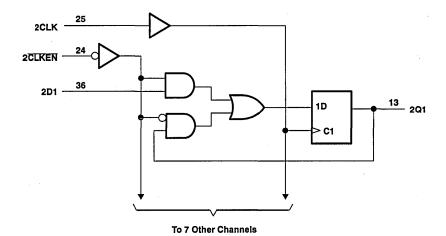
### **FUNCTION TABLE** (each flip-flop)

ii	OUTPUT		
CLKEN	CLK	D	Q
Н	Х	Х	Q <sub>0</sub>
L	Ť	Н	н
L	Ť	L	L
Х	L	Х	_ Q <sub>0</sub>

### logic diagram (positive logic)



To 7 Other Channels



# SN54ABT16377, SN74ABT16377 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

OCTOBER 1992

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	$\dots$ -0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub>	
Current into any output in the low state, Io: SN54ABT16377	96 mA
SN74ABT16377	128 mA
Input clamp current, $I_{IK}(V_I < 0)$	
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85 W
Storage temperature range	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

	•		SN54AB	T16377	SN74ABT16377		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage				2		٧
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage	0	Vcc	0	V <sub>CC</sub>	V	
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48	ļ	64	mA
Δt/Δν	Input transition rise or fall rate Outputs enabled			10		10	ns/V
T <sub>A</sub>	Operating free-air temperature			125	-40	85	ŷ

NOTE 2: Unused or floating inputs must be held high or low.

# SN54ABT16377, SN74ABT16377 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS		T <sub>A</sub> = 25°C			SN54ABT16377		SN74ABT16377		UNIT	
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3	_	3		l v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	i <sub>OH</sub> = -24 m/	4	2			2				ľ
-	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m}.$	A	2‡				-	2		
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			V	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>				0.55	*	
l <sub>1</sub>	$V_{CC} = 5.5 \text{ V}, \qquad V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ	
lozh	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V					50		50		50	μΑ
lozL	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ	
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
			Outputs high			2		2		2	
lcc	V <sub>CC</sub> = 5.5 V <sub>1</sub> V <sub>1</sub> = V <sub>CC</sub> or GND	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, Outputs low	Outputs low	1		67		67		67	mA
	AI = ACC or GIAD		Outputs disabled			2		2		2	
Δl <sub>CC</sub> <sup>3</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>i</sub> = 2.5 V or 0.5 V										pF
Co	Vo = 2.5 V or 0.5 \	<del>/</del>									pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

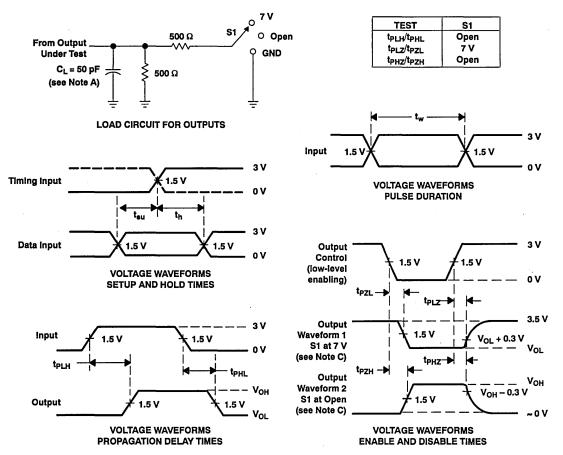
<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SN54ABT16377, SN74ABT16377

# PARAMETER MEASUREMENT INFORMATION

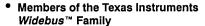


NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>1</sub> ≤ 2.5 ns, t<sub>1</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

OCTOBER 1003



- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

### description

The 'ABT16460 is a 4-bit-to-1-bit multiplexed registered transceiver used in applications where four separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

SN54ABT16460...WD PACKAGE SN74ABT16460...DL PACKAGE (TOP VIEW)

LEAB1	Į, ∪	56	OEBT
LEAB2	3		OEB2
LEBA [			SELO
GND [			GND
LEB1		52	1B1
LEB2			1B2
V <sub>CC</sub> [		50	Vcc
CLKBA [			1B3
OEB [			1B4
CLKAB [			2B1
GND [			GND
1A [			[] 2B2
2A [			[]2B3
CE_SEL0[			[]2B4
CE_SEL1			[]3B1
	16		[] 3B2
4A [			[] звз
GND [	18		GND
CLKENAB [	19		] 3B4
CLKENB [			[] 4B1
CLKENBA [	21	36	] 4B2
V <sub>cc</sub> [		35	]v <sub>cc</sub>
LEB3 [		34	] 4B3
LEB4 [	24	33	] 4B4
GND [		32	GND
OEA [		31	SEL1
LEAB3 [			OEB3
LEAB4 [	28	29	OEB4

Five 4-bit I/O ports (1A-4A, 1B1-4, 2B1-4, 3B1-4, and 4B1-4) are available for address and/or data transfer. The output-enable (OEB, OEB1-OEB4, and OEA) inputs control the bus transceiver functions. These control signals also allow 4-bit or 16-bit control depending on the OEB level.

Address and/or data information can be stored using the internal storage latches/flipflops. The latch-enable (LEB1-LEB4, LEBA, and LEAB1-LEAB4) and clock/clock-enable (CLK/CLKEN) inputs are used to control data storage. When either one of the latch-enable inputs is high, the latch is transparent (clock is a don't care as long as the latch-enable is high). When the latch-enable input goes low (providing that the clock does not transit from low to high), the data present at the inputs is latched and remains latched until the latch-enable input is returned high. When the clock-enable is low and all the latch-enables are low, data can be clocked on the low to high transition of the clock. When either the clock-enable or one latch-enable is high, the clock is a don't care.

Four select pins (SEL0, SEL1, CE\_SEL0, and CE\_SEL1) are provided to multiplex data (A port), or to select one of four clock-enables (B port). This allows the user to have the flexibility of controlling one bit at a time.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

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### description (continued)

To ensure the high-impedance state during power-up or power-down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16460 is packaged in Ti's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16460 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16460 is characterized for operation from –40°C to 85°C.

#### A-TO-B OUTPUT-ENABLE TABLE†

INP	OUTPUT	
OEB	<b>OEB</b> n	Bn
Н	Н	Z
Н	L	z
L	н	z
L	L.	Active

† n = 1, 2, 3, 4

#### A-TO-B STORAGE TABLE (ASSUMING OEB = L, OEBn = L)‡

			INPUTS						OUTI	PUTS	
CLKENAB	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
Х	Х	Х	X	Н	L	L	Ļ	Α	A <sub>0</sub>	A <sub>0</sub>	A <sub>0</sub>
x	X	X	X	н	н	Н	L	Α	Α	Α	A <sub>0</sub>
L	X	Х	L	L	L	· L	L	A <sub>0</sub>	$A_0$	$A_0$	A <sub>0</sub>
L	L	L	<b>†</b>	Ļ	L	L	L	Α	Ao	$A_0$	A <sub>0</sub>
L	L	Н	<b>†</b>	L	L	L	L	A <sub>0</sub>	Α	$A_0$	A <sub>0</sub>
<u> </u> L	Н	L	Ť	L	L	L	L	Ao	Ao	Α	A <sub>0</sub>
L	Н	Н	<b>†</b>	L	Ļ	L	L	Ao	Ao	$A_0$	Α
Н	Х	· X	<u> </u>	L	L	L	L	A <sub>0</sub>	Ao	Ao	Ao

<sup>‡</sup> This table does not cover all the latch-enable cases since they have similar results.

### B-TO-A STORAGE TABLE (BEFORE POINT "P")

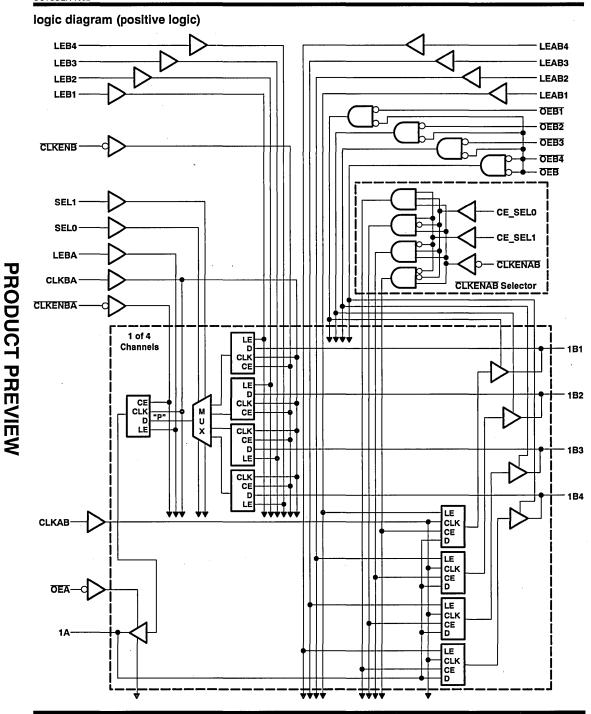
			INPUTS	3				"p"						
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	] [						
X	Х	Н	L	L	L	L	L	B1						
x	X	L	Н	L	L	L	н	B2						
X	X	L	L	Н	L	Н	L	В3						
Х	X	L	L	L	н	Н	Н	B4						
			L					L	L	B1				
١,						L	н	B2						
-	I	L		_	_	_	_	_	_	_	_	_	н	L
						н	Н	B4						
						L	L	B1₀ <sup>†</sup>						
Ι,					,	L	н	B2 <sub>0</sub> †						
	_	L	L	L	L I	_	н	L	B3₀†					
				Н	Н	B4 <sub>0</sub> †								

#### **B-TO-A STORAGE TABLE (AFTER POINT "P")**

Die Aerenaar indee (Airen einer 17)							
	INPUTS						
CLKENBA	CLKBA	LEBA	OEA	В	Α		
X	Х	Х	Н	Х	Z		
х	X	Н	L	L	L		
Х	X	Н	L	Н	н		
н	X	L	L	X	A <sub>0</sub> †		
L	1	L	L	L	L		
L	t	L	L	. Н	н		
L	L	L	L	X	A <sub>0</sub> †		

<sup>†</sup> Output level before the indicated steady-state input conditions were established.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, $V_0$ $-0.5$ V to $5.5$ V
Current into any output in the low state, Io: SN54ABT16460
SN74ABT16460 128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

			SN54AB	T16460	SN74AB	T16460	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage		2		2		V
ViL	Low-level input voltage			0.8		0.8	٧
Vi	Input voltage		0	Vcc	0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		.10		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	750	T CONDITIO	NO	Ţ	A = 25°C	;	SN54AB	T16460	SN74ABT16460		UNIT
PARAMETER	168	T CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = 3 m/	4	2.5			2.5		2.5		
١,,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 m/	Α	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 n	1A	2			2				V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 n	ıΑ	2‡					2		
.,	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡	ĺ			0.55	V
•	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
lş .	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V <sub>1</sub>	$V_1$ or $V_0 \le 4$	.5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-200	-50	-200	-50	-200	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	ports	Outputs low			35		35		35	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			2		2		2	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					1.5	,	1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V	I = 2.5 V or 0.5 V Control inputs									pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V	,	A or B ports								pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54AB	Г16460	SN74AB	Γ16460	LIMIT
				MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
	Pulse duration	LEAB or LEBA high				4		
t <sub>w</sub>	Puise duration	CLKAB or CLKBA high or low			4		ns	
		Before CLK†	A or B			2		
	Setup time	Belore CLKT	CLKEN			3		
t <sub>su</sub>	Setup time	A before LEAB↓ or B before LEBA↓*	CLK high			2	MAX	ns
		A pelote CEART of B pelote CERAT.	CLK low			2		
t <sub>h</sub> Hold time		After CLK†	A or B			. 2		
	Hold time	VIII OFICE	CLKEN			2		ns
		A after LEAB or B after LEBA				3		

<sup>\*</sup> Tight parameters



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>mbox{\$}$  The parameters  $\mbox{I}_{\mbox{\scriptsize OZH}}$  and  $\mbox{I}_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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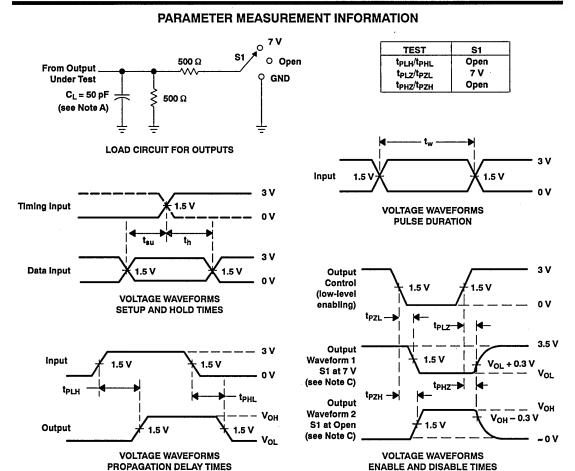
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

	- · · · · · · · · · · · · · · · · · · ·									
PARAMETER	FROM (INPUT)	TO (OUTPUT)		cc = 5 V \ = 25°C		SN54ABT	Г16460	SN74AB	Г16460	UNIT
	(1117-01)	(0011-01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A							7*	ns
t <sub>PHL</sub>	7 701 5	B 01 A							7*	113
t <sub>PLH</sub>	CLKAB	В								ns
t <sub>PHL</sub>	OLIVID									
t <sub>PLH</sub>	CLKBA	A								ns
t <sub>PHL</sub>	OLINO/	^								
t <sub>PLH</sub>	LEAB	В							7	ns
t <sub>PHL</sub>	22,0								7	
t <sub>PLH</sub>	LEBA	A							6	ns
t <sub>PHL</sub>	LED, (	,	<u></u>						6	
t <sub>PLH</sub>	LEB	A							8	ns
t <sub>PHL</sub>		^	l						8	,,,,
t <sub>PLH</sub>	SEL	Α							8	ns
t <sub>PHL</sub>		^							8	
t <sub>PLH</sub>	CE_SEL	В								ns
t <sub>PHL</sub>	02_022									
t <sub>PZH</sub>	OE	A or B							10	ns
t <sub>PZL</sub>	"	7.015							10	
t <sub>PHZ</sub>	OE .	A or B							10	ns
t <sub>PLZ</sub>	1 6	7.57 B							10	

<sup>\*</sup> Tight parameters



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NOTES: A. C. includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

### SN54ABT16470, SN74ABT16470 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments
   Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

### description

The 'ABT16470 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16470 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate clock (CLKAB or CLKBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

To avoid false clocking of the flip-flops, CE should not be switched from high to low while CLK is high.

SN54ABT16470...WD PACKAGE SN74ABT16470...DL PACKAGE (TOP VIEW)

2CLKAB 27 30 2CLKE			TT		
1CLKAB 2 55 1CLKAB 1CEAB 3 54 1CEB 3 54 1CEB 3 1CEB	10EAB	1	O	56	10EBA
1CEAB 3 54 1 1CEB GND 4 53 GND 1A1 5 52 1B1 1A2 6 51 1B2 VCC 7 50 VCC 1A3 8 49 1B3 1A4 9 48 1B4 1A5 10 47 1B5 GND 11 46 GND 1A6 12 45 1B6 1A7 13 44 1B7 1A8 14 43 1B8 2A1 15 42 2B1 2A2 16 41 2B2 2A3 17 40 2B3 GND 18 39 GND 2A4 19 38 2B4 2A5 20 37 2B5 2A6 21 36 2B6 VCC 22 35 VCC 2A7 23 34 2B7 2A8 24 33 2B8 GND 25 32 GND 2CEAB 26 31 2CEB	1CLKAB	2			
GND					
1A2	GND	4			
V <sub>CC</sub> 7       50       V <sub>CC</sub> 1A3       8       49       1B3         1A4       9       48       1B4         1A5       10       47       1B5         GND       11       46       GND         1A6       12       45       1B6         1A7       13       44       1B7         1A8       14       43       1B8         2A1       15       42       2B1         2A2       16       41       2B2         2A3       17       40       2B3         GND       18       39       GND         2A4       19       38       2B4         2A5       20       37       2B5         2A6       21       36       2B6         V <sub>CC</sub> 22       35       V <sub>CC</sub> 2A7       23       34       2B7         2A8       24       33       2B8         GND       25       32       GND         2CEAB       26       31       2CEB         2CLKAB       27       30       2CLKE	1A1 [	5		52	1B1
1A3  8	1A2[	6		51	1B2
1A3  8	V <sub>CC</sub> [	7		50	0 v <sub>cc</sub>
1A4	1A3[	8			
1A5				48	] 1B4
1A6	1A5[	10			
1A7 [ 13	GND[	11		46	] GND
1A8	1A6[	12		45	] 1B6
2A1	1A7[	13			
2A2	1A8[	14			
2A3	2A1 [	15			
GND	2A2[	16		41	] 2B2
2A4	2A3[	17		40	] 2B3
2A5					
2A6				38	] 2B4
V <sub>CC</sub> 22 35 V <sub>CC</sub> 2A7 2B7 2A8 2A8 2A7 2A8 2A8 3A 2B8 3A 2B8 3A 2CEAB 2CLKAB 27 30 2CLKAB 27 30 2CLKAB 2A 35 2CLKAB 3A 35 2	2A5[]	20			
2A7 [ 23 34 ] 2B7 2A8 [ 24 33 ] 2B8 GND [ 25 32 ] GND 2CEAB [ 26 31 ] 2CEB 2CLKAB [ 27 30 ] 2CLKE					
2AB 24 33 28B GND 25 32 GND 2CEAB 26 31 2CEB 2CLKAB 27 30 2CLKB					
GND   25 32   GND 2CEAB   26 31   2CEB 2CLKAB   27 30   2CLK					
2CEAB 26 31 2CEB 2CLKAB 27 30 2CLK					€
2CLKAB 27 30 2CLKE					
3 6					2CEBA
					=
20EAB [ 28 29 ] 20EB	2OEAB	28		29	20EBA

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16470 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

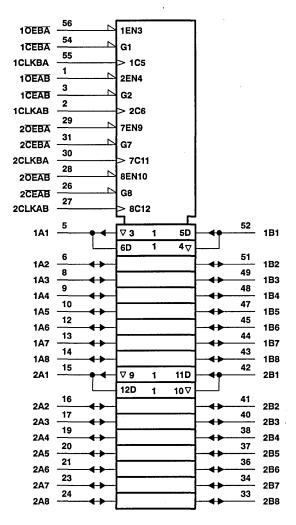
The SN54ABT16470 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16470 is characterized for operation from –40°C to 85°C.

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# SN54ABT16470, SN74ABT16470 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

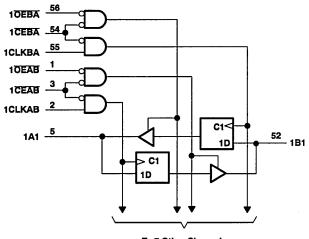
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### logic symbol†

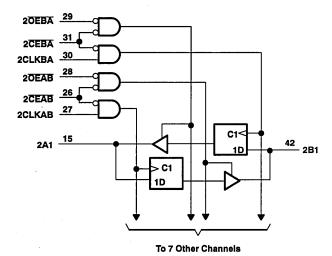


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



To 7 Other Channels



#### FUNCTION TABLE<sup>†</sup>

	INPU	TS		OUTPUT			
CEAB	CEAB CLKAB OEAB A						
Н	Х	Х	Х	Z			
X	X	. <b>H</b>	X	z			
L	L	L.	Х	B₀‡			
L	<b>†</b>	L	L	L			
L	Ť	L	н	н			

<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses CEBA, CLKBA, and OEBA.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
, , , , , , , , , , , , , , , , , , , ,	
Voltage range applied to any output in the high state or power-off state, VO	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16470	96 mA
SN74ABT16470	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	

<sup>§</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

			SN54AB	T16470	SN74AB	T16470	UNIT
İ			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2	84	2		٠V
VIL	Low-level input voltage	•		<i>‰</i> 0.8		8.0	٧
VI	Input voltage		0,5	₹ V <sub>CC</sub>	0	Vcc	٧
loн	High-level output current		30	-24		-32	mA
lor	Low-level output current		N.	48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
T <sub>A</sub>	Operating free-air temperature	~55	125	-40	85	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

Output level before the indicated steady-state input conditions were established.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		T CONDITIO	NO	T	A = 25°C	;	SN54AB	T16470	SN74ABT16470		UNIT
PARAMETER	159	T CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONII
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 m.	A	2.5			2.5		2.5		
l .,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 m.	A	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 n	nA	2			2				V
	V <sub>CC</sub> = 4.5 V,		nA	2‡					2		
,,	$V_{CC} = 4.5 \text{ V},$					0.55		0.55			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA	\			0.55‡		1		0.55	V
	""		Control inputs			±1		€ ±1		±1	μА
l <sub>1</sub>			A or B ports			±100		\$₹±100		±100	μА
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			•	50	<u> </u>			50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	$V_{CC} = 0 V$	$V_1$ or $V_0 \le 4$	.5 V			±100	₹ <sup>6</sup>			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Q,	50		50	μА
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-200	50	-200	-50	-200	mA
	V <sub>CC</sub> = 5.5 V,	A D	Outputs high			2		2		2	
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low			35		35		35	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			2		2		2	
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					0.5		0.5		0.5	mÀ
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	I = 2.5 V or 0.5 V Control inputs			3						pF
Cio	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		A or B ports		8.5						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16470	SN74AB1	Γ16470	UNIT
		MIN	MAX	MIN 🙏 MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	05° منز 150	0	150	MHz
twll	Pulse duration, CLKAB or CLKBA high or low	3.3		33 5	3.3		ns
t <sub>su</sub>	Setup time, data before CLKAB† or CLKBA†	4		Q* 4:*	4		ns
th	Hold time, data after CLKAB↑ or CLKBA↑	1		*	11		ns

Il This parameter is specified by design but not tested.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

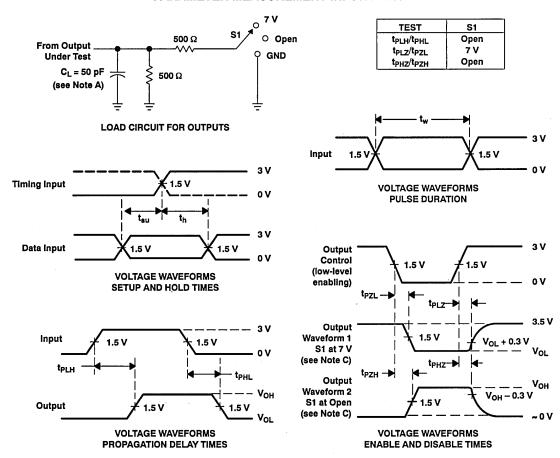
# SN54ABT16470, SN74ABT16470 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS085A-D3794, FEBRUARY 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			T <sub>4</sub> = 25°C			SN54AB1	Г16470	SN74AB	UNIT	
	( 0.)	( 5.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>			150			150		150		MHz	
t <sub>PLH</sub>	CLK	A or B	1.4	3.1	4.8	1.4	5.1	1.4	4.9		
t <sub>PHL</sub>	OLK	Aorb	1.3	3.2	4.6	1.3	<i>j</i> ;5.1	1.3	4.9	ns	
t <sub>PZH</sub>	ŌĒ	A or B	1	3.1	4.3	1	5	1	4.9	ns	
t <sub>PZL</sub>	OE	7016	1.2	3.6	5.8	1.2		1.2	6.8	"5	
t <sub>PHZ</sub>	Œ		1.9	3.7	4.9	1.95	6	1.9	5.5	ns	
t <sub>PLZ</sub>	OE.	A or B	1.6	3.3	4.8	1,8	5.4	1.6	5.3	ns	
t <sub>PZH</sub>	CE	A a s D	1	3.4	4.6 0 1 5.8	1	5.7				
t <sub>PZL</sub>	CE	A or B	1.2	3.9	6	Q 1.2	7.3	1.2	7.2	ns	
t <sub>PHZ</sub>	CE	A B	1.7	3.9	5.2	1.7	6.2	1.7	5.8		
t <sub>PLZ</sub>	CE	A or B	1.5	3.6	5.3	1.5	5.5	1.5	5.4	ns	



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\leq}$  10 MHz,  $Z_{0}$  = 50  $\Omega$ ,  $t_{f}$   $_{\leq}$  2.5 ns,  $t_{f}$   $_{\leq}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

SN54ABT16500A... WD PACKAGE SN74ABT16500A... DL PACKAGE (TOP VIEW)

	_	7 7		1		
OEAB[	1	U	56	b	GND	
LEAB[	2			_	CLKA	В
A1[			54	6	B1	
GND[	4			_	GND	
A2[	5		52		B2	
A3[	6		51		ВЗ	
V <sub>cc</sub> [	7		50	<u>י</u>	$V_{CC}$	
A4[			49		B4	
A5[	9		48	ו	B5	
A6[	10		47	ו	B6	
GND[	11		46	<u>ו</u>	GND	
A7[			45		B7	
A8[			44		B8	
A9[	14		43	<u>ן</u>	B9	
A10[	15		42	֓֞֞֞֜֞֜֞֜֓֓֓֓֟֜֝֟֟֝ <del>֡</del>	B10	
A11 [	16		41	ו	B11	
A12[	17		40	ַו [	B12	
GND[	18		39	]	GND	
A13[	19		38		B13	
A14[	20		37	ו	B14	
A15[	21		36	ו	B15	
V <sub>CC</sub> [	22		35	<u>י</u> [	Vcc	
A16[	23		34		B16	
A17[	24		33		B17	
GND[	25		32	]	GND	
A18[	26		31	]	B18	
OEBA[	27		30	]	CLKB	Ā
LEBA[	28		29	]	GND	

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16500A is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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# SN54ABT16500A, SN74ABT16500A **18-BIT UNIVERSÁL BUS TRANSCEIVERS** WITH 3-STATE OUTPUTS SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

### description (continued)

The SN54ABT16500A is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT16500A is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

	INPUTS							
OEAB	LEAB	CLKAB	Α	В				
L	Х	Х	X	Z				
н	Н	X	L	L				
н	Н	X	н	н				
н	L	<b>↓</b>	L	L				
Н	L	<b>↓</b>	Н	н				
н	L	Н	X	B <sub>0</sub> ‡ B <sub>0</sub> §				
н	L	L	X	B <sub>0</sub> §				

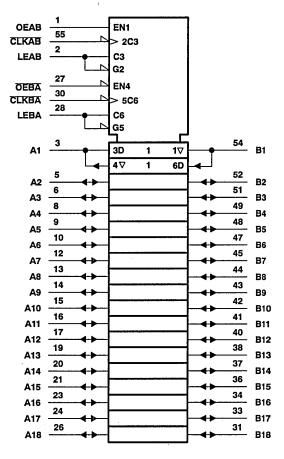
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

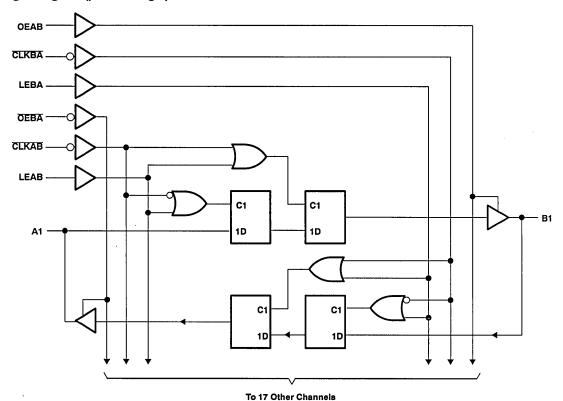
# logic symbol†



 $<sup>^\</sup>dagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

### logic diagram (positive logic)



#### 10 17 Other Chairners

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	. −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16500A	96 mA
SN74ABT16500A	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

### recommended operating conditions (see Note 2)

			SN54ABT	16500A	SN74ABT	16500A	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	.,√5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	32	2		٧
VIL	Low-level input voltage		ź	<b>4</b> 0.8		0.8	٧
Vı	Input voltage		0,4	Vcc	0	Vcc	V
Іон	High-level output current		, Ç	-24		-32	mA
loL	Low-level output current		N.	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	SE	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T	T <sub>A</sub> = 25°C			SN54ABT16500A		SN74ABT16500A	
PAHAMETER	'ES	I CONDIII	JNS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},$	l <sub>I</sub> = -18 m/	4			-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 r	nA	2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	l <sub>OH</sub> = -3 r	nA	3			3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24	mA	2			2				
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32	mA	2‡					2		1
.,	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 m	Α			0.55‡		G.		0.55	
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
"	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100	8	±100		±100	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$				50	4	50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	్రస్	-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤	4.5 V			±100	, O			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> =	5.5 V	Outputs high			50	Q*	50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	180	-50	-180	mΑ
	V <sub>CC</sub> = 5.5 V,		Outputs high			3		3		3	
Icc	i <sub>O</sub> = 0,	A or B ports	Outputs low			76		76		76	mΑ
	$V_I = V_{CC}$ or GND	Ports	Outputs disabled			3.3		3.3		±1 ±100 50 -50 ±100 50 -180	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
Cio	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		A or B ports		8						рF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT	16500A	SN74ABT	16500A	115117
			MIN MAX				MAX	UNIT
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
. +	Dulas duration	LEAB or LEBA high		3.3	G.	3.3		
tw <sup>†</sup>	Pulse duration	Pulse duration CLKAB or CLKBA high or low	_	3.3 4.5	<i>2</i> 2,	3.3		ns
		A before CLKAB↓	A before CLKAB↓  B before CLKBA↓			4.5		
	Setup time	B before CLKBA↓				4		ns
t <sub>su</sub>	Setup time	A hefere I EARL or R hefere I ERAL	CLK high	1:5	,	1.5		115
		A before LEAB or B before LEBA	CLK low	(4.5		4.5		
	Hold time	A after CLKAB t or B after CLKBA t		₹ 0		0		
t <sub>h</sub>	Hold time	A after LEAB tor B after LEBA		1.5		1.5		ns

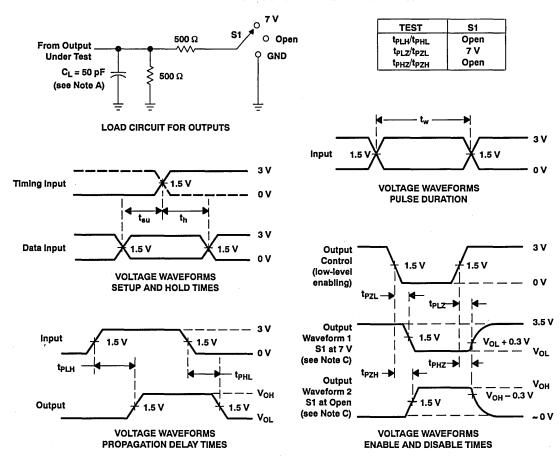
<sup>†</sup> This parameter is specified by design but not tested.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16500A		SN74ABT16500A	
	( 5.)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150	200		150		150		MHz
t <sub>PLH</sub>	A or B	B or A	1.1	2.7	3.6	1.1	4.4	1.1	4	ns
t <sub>PHL</sub>	7016	BUIA	1	2.9	3.9	1	4.6	1	4.6	115
t <sub>PLH</sub>	LEAB or LEBA	B or A	1	3.4	4.7	1	5.6	1	5.3	ns
t <sub>PHL</sub>	LEAD OF LEBA	BUIA	1	3.4	4.7	1 ,	<b>₹</b> 5.4	1	5	113
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	1	3.1	4.4	1/5	5.4	. 1	5.3	ns
tpHL	CLINAD OF CLINDA	BUIA	1	3.1	4.3	72	5.2	1	5	115
tpzH	OEAB or OEBA	B or A	1	2.9	4.1	,O1	4.8	1	4.8	ns
t <sub>PZL</sub>	OEAB OF OEBA	B OF A	2.5	4.5	5.7	<b>ℚ</b> ~2.5	6.9	2.5	6.6	115
t <sub>PHZ</sub>	OEAB or OEBA	OEBA B or A	1.5	4.5	5.2	1.5	6.6	1.5	6.2	ns
t <sub>PLZ</sub>	] OLAB OI OLBA	BUIA	1.4	3.4	4.7	1.4	5.8	1.4	5.4	118

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{<}$  10 MHz,  $Z_{0}$  = 50  $\Omega$ ,  $t_{1}$   $_{<}$  2.5 ns,  $t_{1}$   $_{<}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS086A-D3795, FEBRUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Filp-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

SN54ABT16501 ... WD PACKAGE SN74ABT16501 ... DL PACKAGE (TOP VIEW)

ï		П		1	
OEAB[	1	U	56	þ	GND
LEAB[	2		55	þ	CLKAB
A1[	3		54	þ	B1
GND[	4		53	þ	GND
A2[	5		52	þ	B2
A3[	6		51	1	B3
V <sub>CC</sub> [	7		50	þ	Vcc
A4[	8		49		B4
A5[	9		48	0	B5
A6[	10		47	0	B6
GND[	11		46		GND
A7[	12		45		B7
]8A	13		44		B8
A9[	14		43	þ	B9
A10[	15		42	1	B10
A11[	16		41	þ	B11
A12[	17		40	þ	B12
GND[	18		39	ן	GND
A13[	19		38	ן	B13
A14[	20				B14
A15[	21		36		B15
Vcc	22		35		$V_{CC}$
A16[]	23		34		B16
A17[]	24			_	B17
GND	25		32	D	GND
A18[]	26		31		B18
OEBA[]	27			2	CLKBA
LEBA[	28		29	0	GND

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16501 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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# SN54ABT16501, SN74ABT16501 **18-BIT UNIVERSAL BUS TRANSCEIVERS** WITH 3-STATE OUTPUTS SCBS086A-D3795, FEBRUARY 1991-REVISED OCTOBER 1992

### description (continued)

The SN54ABT16501 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT16501 is characterized for operation from -40°C to 85°C.

### **FUNCTION TABLE<sup>†</sup>**

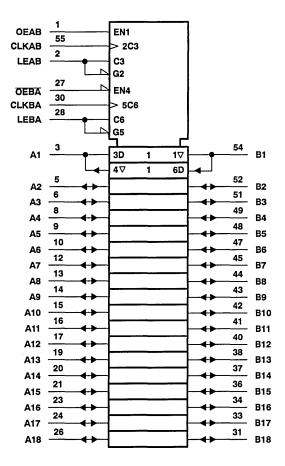
	INPUTS							
OEAB	LEAB	CLKAB	Α	В				
L	Х	Х	X	Z				
Н	Н	X	L	L				
Н	Н	X	Н	н				
н	L	†	L	L				
н	L	<b>†</b>	Н	н				
Н	L	Н	X	В <sub>о</sub> ‡ Во§				
Н	L	L	X	B <sub>0</sub> §				

<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

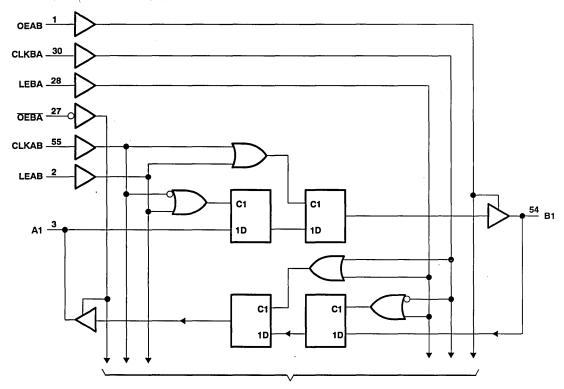
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS086A-D3795, FEBRUARY 1991-REVISED OCTOBER 1992

### logic diagram (positive logic)



To 17 Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	$\dots$ -0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$\dots$ -0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16501	96 mA
SN74ABT16501	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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### recommended operating conditions (see Note 2)

			SN54AB	T16501	SN74AB	UNIT	
İ		•	MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	<b>,</b> ₹5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	74	2		V
VIL	Low-level input voltage			<b>ॐ</b> 0.8		0.8	V
Vı	Input voltage		9,9	· Vcc	0	Vcc	٧
Іон	High-level output current		- 8	-24		-32	mA
loL	Low-level output current		8	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	85	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			Т	T <sub>A</sub> = 25°C			T16501	SN74ABT16501		UNIT
PARAMETER				MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	\	2.5			2.5		2.5			
.,	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3			3		3		l v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,						2				
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	Α	2‡			-		2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0,55			V
$V_{OL}$	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡		ii.		0.55	l
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1 كري		±1	
l <sub>l</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100	Á	₹ ±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	<i></i>	50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	,5"	-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100	,0'			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Q.	50		50	μА
10 <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A D	Outputs high			3		5		3	· ·
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			76		76		76	mΑ
	V <sub>I</sub> = V <sub>CC</sub> or GND	ports	Outputs disabled			3.3		5.3		3.3	
A1#	V <sub>CC</sub> = 5.5 V, One ir	put at 3.4 V,	Control inputs			5		6		5	mA
ΔI <sub>CC</sub> #	Other inputs at V <sub>CC</sub> or GND		A or B ports			1.5		1.5		1.5	IIIA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		8						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $<sup>^{\#}</sup>$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54AB	T16501	SN74AB1	UNIT	
				MIN	MAX	MIN	וואט	
f <sub>clock</sub>	Clock frequency, (	CLKAB or CLKBA		0	105	0	105	MHz
tT Pulse duration I	LEAB or LEBA high	LEAB or LEBA high			3.3			
	CLKAB or CLKBA high or low	4.7 8	¥	4.7		ns		
		A before CLKAB† or B before CLKBA†		42		3.5		
t <sub>su</sub>	Setup time	A before LEAB L or B before LEBA L	CLK high	. ÇA		4		ns
		A perote CEART of B perote CERAT	CLK low	<b>,</b> \$7.5		1.5		-
	Hold time	A after CLKAB† or B after CLKBA†	A after CLKAB† or B after CLKBA†			1		
t <sub>h</sub> Hold time	A after LEAB or B after LEBA		2.5		2.5		ns	

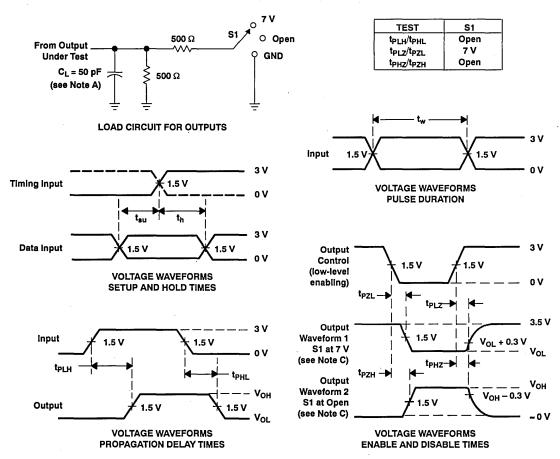
<sup>&</sup>lt;sup>†</sup> This parameter is specified by design but not tested.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO $T_A = 25^{\circ}C$			SN54ABT16501		SN74ABT16501		UNIT	
	(14701)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MIN MAX	
f <sub>max</sub>	CLKAB or CLKBA		105	160		105		105		MHz
t <sub>PLH</sub>	A or B	B or A	1	2.6	3.4	1	3.9	1	3.7	ns
t <sub>PHL</sub>	7 ^0' 6	D OF A	1	2.6	3.4	1	<i>3</i> ,4.1	1	4	ns
t <sub>PLH</sub>	LEAB or LEBA	B or A	1.3	3.3	4.3	1.3	5.4	1.3	5.1	ns
t <sub>PHL</sub>	T LEAB OI LEBA		1.4	3.1	4.1	1.4	🌣 4.6	1.4	4.4	
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	1.5	3.5	4.5	1.5	5.3	1.5	5	ns
t <sub>PHL</sub>	CLIVAB OF CLIVBA	BUIA	1.3	3.1	4.1	1,3	4.6	1.3	4.4	115
t <sub>PZH</sub>	OEAB or OEBA	B or A	1	3	4	<u>,0</u> 1	4.8	1	4.7	
t <sub>PZL</sub>	OEAB OF OEBA	B or A	2.6	4.9	5.9	Q 2.6	6.6	2.6	6.5	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A	1.6	3.9	4.9	1.6	5.9	1.6	5.8	ns
t <sub>PLZ</sub>	7 OEAB UT OEBA	BOTA	1.1	3.4	4.4	1.1	5.1	1.1	4.9	

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns.}$   $t_f \leq 2.5 \text{ ns.}$
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

### SN54ABT16540, SN74ABT16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

D3796, FEBRUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all corresponding outputs are in the high-impedance state.

SN54ABT16540 ... WD PACKAGE SN74ABT16540 ... DL PACKAGE (TOP VIEW)

	-		
10E1[	1 ·	48	10E2
1Y1 [	2	47	] 1A1
1Y2[	3	46	1A2
GND[	4	45	
1Y3[	5	44	] 1A3
1Y4[	6	43	
v <sub>cc</sub> [	7	42	$]_{V_{CC}}$
1Y5[		41	] 1A5
1Y6	9		1A6
GND	10	39	GND
1Y7[		38	] 1A7
1Y8[			] 1A8
2Y1 [	13	36	] 2A1
2Y2[	14	35	2A2
GND[	15	34	GND
2Y3[	16	33	2A3
2Y4[		32	2A4
v <sub>cc</sub> [	18	31	$v_{cc}$
2Y5[		30	,
2Y6	20	29	2A6
GND	21		GND
2Y7	1		2A7
2Y8	3	26	2A8
20E1	24	25	2 <del>0E</del> 2

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16540 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16540 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16540 is characterized for operation from -40°C to 85°C.

# FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
OET	OE2	Α	Υ
L	L	L	Н
L	L	Н	L
н	Χ	X	z
х	Н	X	z

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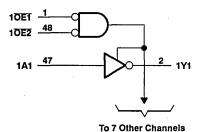
# SN54ABT16540, SN74ABT16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

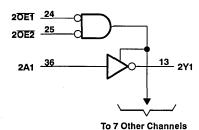
D3796, FEBRUARY 1991-REVISED OCTOBER 1992

# logic symbol†

#### 10E1 EN1 10E2 24 & 20E1 EN2 25 20E2 47 1A1 1∇ 46 1A2 1Y2 44 5 1Y3 1A3 43 6 1A4 1Y4 41 1A5 1Y5 40 9 1A6 **1Y6** 38 11 1A7 **1Y7** 37 12 1Y8 1A8 36 13 2∇ 2A1 2Y1 35 14 2A2 2Y2 33 16 2A3 2Y3 32 17 2A4 2Y4 30 19 2A5 2Y5 29 20 2A6 2Y6 27 22 2A7 2Y7 26 23 2A8 2Y8

#### logic diagram (positive logic)





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16540	96 mA
SN74ABT16540	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85 W
Storage temperature range	

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### recommended operating conditions (see Note 2)

			SN54AB	SN54ABT16540		SN74ABT16540	
	<b>\</b>		MIN MAX		MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5,5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	39	2		V
VIL	Low-level input voltage			<i>(</i> 4 0.8	<u> </u>	0.8	V
VI	Input voltage		0,5	Vcc	0	Vcc	V
Іон	High-level output current		- 5	-24	<u> </u>	-32	mA
I <sub>OL</sub>	Low-level output current		- S	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	SE.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TE	ST CONDITIO	NO.	Т	A = 25°(	•	SN54AB	T16540	SN74ABT16540		UNIT
PANAMETER	'5	SI CONDIIIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	וואט
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			2.5			2.5		2.5		
V	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, l <sub>OL</sub> = 48 mA					0.55		0.55			V
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or C	ND			±1		<u>*</u> 1		±1	μА
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		≪50		50	μA
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		<i>5</i> 4-50		-50	μΑ
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100	2.	ξ.		±100	μА
ICEX	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50	Q	50		50	μΑ
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-5D	-180	-50	-180	mA
	V 55V	1 0	Outputs high			2	Ŗ	2		2	
Icc .	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0,$	Outputs low		-	32		32		32	mA
	11 - 100 or and		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data innuta	Outputs enabled			1		1		1	
ΔICCT	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control input	s			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	*			7			-			pF
C <sub>o</sub> _	V <sub>O</sub> = 2.5 V or 0.5 V	/			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air

temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		cc = 5 V 4 = 25°C		SN54ABT16540		SN74ABT16540		UNIT	
	(1141 01)	(66.1.61)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	А	^	V	1	2.3	3.3	1	4.2	1	4.1	
t <sub>PHL</sub>		, T	1.1	2.5	4.1	1.1	<b>⊘</b> , 4.4	1.1	4.3	ns	
t <sub>PZH</sub>	ŌĒ		1.1	3.1	4.2	1,10	<b>5.2</b>	1.1	5.1		
t <sub>PZL</sub>	OE	1 .	1.6	3.7	4.8	ું ૧.6૯		1.6	5.9	ns	
t <sub>PHZ</sub>	OE	Y	1.6	3.4	4.6	146	5.4	1.6	5.3	ns	
t <sub>PLZ</sub>			1.4	2.9	4.1	1.4	4.7	1.4	4.4		

#### PARAMETER MEASUREMENT INFORMATION TEST S1 **500** Ω t<sub>PLH</sub>/t<sub>PHL</sub> Open From Output t<sub>PLZ</sub>/t<sub>PZL</sub> 7 V GND **Under Test** t<sub>PHZ</sub>/t<sub>PZH</sub> Open $C_L = 50 pF$ **500** Ω (see Note A) 3 V Output Control LOAD CIRCUIT FOR OUTPUTS (low-level enabling) 3.5 V Output Input Waveform 1 V<sub>OL</sub> + 0.3 (see Note B) S1 at 7 V (see Note C) t<sub>PHZ</sub>→ Output VoH Waveform 2 V<sub>OH</sub> - 0.3 V S1 at Open Output (see Note C) ~ 0 V **VOLTAGE WAVEFORMS** VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

**ENABLE AND DISABLE TIMES** 

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

PROPAGATION DELAY TIMES

Figure 1. Load Circuit and Voltage Waveforms



# SN54ABT16541, SN74ABT16541 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS118A-D3797, FEBRUARY 1991-REVISED OCTOBER 1992

- **Members of the Texas Instruments** Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design **Significantly Reduces Power Dissipation**
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA lot)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance SN54ABT16541...WD PACKAGE SN74ABT16541... DL PACKAGE (TOP VIEW)

		1-1		l .
10E1[	1	<u> </u>	48	10E2
1Y1[	2		47	] 1A1
1Y2[	3		46	] 1A2
GND	4		45	] GND
1Y3[	5		44	] 1A3
1Y4[]	6		43	] 1A4
Vcc	7		42	□ v <sub>cc</sub>
1Y5	8		41	1A5
1Y6	9		40	1A6
GND	10		39	] GND
1Y7[]	11		38	] 1A7
1Y8	12		37	] 1A8
2Y1	13		36	2A1
2Y2	14		35	2A2
GND[]	15		34	GND
2Y3	16		33	2A3
2Y4[]	17		32	2A4
Vcc	18		31	□ v <sub>cc</sub>
2Y5	19		30	2A5
2Y6	20		29	2A6
GND	21		28	GND
2Y7	22		27	2A7
2Y8	23		26	2A8
20E1[	24		25	20E2
				l

The SN74ABT16541 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16541 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16541 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE** (each 8-bit section)

		INPUTS		OUTPUT
	OE1	OE2	Α	Y
1	L	L	L	L
1	L	L	Н	н
I	н	X	Χ	z
l	Х	Н	X	z

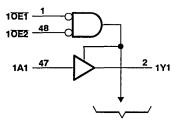
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### SN54ABT16541, SN74ABT16541 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

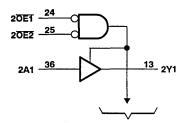
SCBS118A-D3797, FEBRUARY 1991-REVISED OCTOBER 1992

#### logic symbol† EN1 48 10E2 24 20E1 EN2 25 20E2 47 1 🗸 **1Y1** 1A1 46 3 1A2 1Y2 44 5 1Y3 1A3 43 6 1A4 1Y4 41 8 1A5 **1Y5** 40 9 1Y6 1A6 11 38 **1Y7** 1A7 37 12 1A8 1Y8 36 13 2A1 2 ▽ 2Y1 35 14 2Y2 2A2 33 16 2A3 2Y3 32 17 **2Y4** 2A4 30 19 2A5 2Y5 29 20 2A6 2Y6 27 22 2Y7 **2A7** 26 23 2A8 2Y8

#### logic diagram (positive logic)



To 7 Other Channels



To 7 Other Channels

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16541	
SN74ABT16541	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85 W
Storage temperature range	65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### recommended operating conditions (see Note 2)

			SN54ABT165		SN74AB	T16541	UNIT
1			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	8	2		V
VIL	Low-level input voltage			<i>&amp;</i> 0.8		0.8	٧
VI	Input voltage		0,4	₹ V <sub>CC</sub>	0	·Vcc	V
Іон	High-level output current		- 5	-24		-32	mA
loL	Low-level output current		20	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	55	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	75	T CONDITIO	NO	Т	A = 25°0		SN54AB	T16541	SN74ABT16541		UNIT
PARAMETER	'5	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA	2.5			2.5		2.5			
\	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		v I
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	Α	2			2				, v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	2‡					2			
V	V <sub>CC</sub> = 4.5 V,	<sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	_ *
l <sub>L</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND				±1		<u>*</u> 1		±1	μA
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		≪50		50	μА
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-	-50		<i>&amp;</i> 4−50		-50	μА
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±100		Σ,		±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Ş	50		50	μА
lo <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-5D	-180	-50	-180	mA
	V 55V		Outputs high			2	-50	2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			32	,	32		32	mA
	11-10001010		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data issues	Outputs enabled			1	-	1.5		1	
Δlcc¶	input at 3.4 V, Other inputs at	nput at 3.4 V, Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND					1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				7						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$				7						pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $<sup>^{\</sup>P}$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

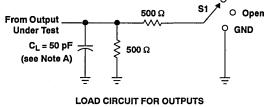
SCBS118A-D3797, FEBRUARY 1991-REVISED OCTOBER 1992

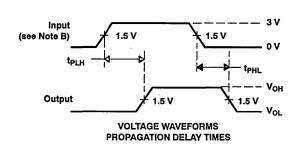
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

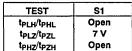
PARAMETER	FROM (INPUT)	то (оитрит)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16541		SN74ABT16541	
	( 01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	V	1	2.1	3	1	, 3.5	1	3.4	ns
t <sub>PHL</sub>	^	'	1	2.5	3.6	1,5	4.3	1	4.2	115
tpzH	OE	Y	1.3	3.2	4.3	10%	5.3	1.3	5.2	
t <sub>PZL</sub>	OE .		1.6	3.8	4.7	Q1,6 <sup>©</sup>	6.2	1.6	6	ns
t <sub>PHZ</sub>	Z OE	V	1.3	3.4	4.4	1.3	5.4	1.3	5.1	ns
t <sub>PLZ</sub>	. 01		1	2.7	3.6	1	4.3	1	3.9	

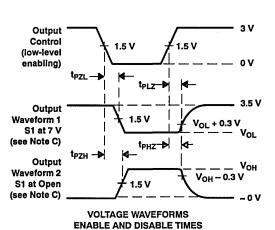
PARAMETER MEASUREMENT INFORMATION

# 7 V S1 Open t<sub>p</sub>









NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_r \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54ABT16543, SN74ABT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS087A-D3798, FEBRUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. The 'ABT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

SN54ABT16543... WD PACKAGE SN74ABT16543... DL PACKAGE (TOP VIEW)

			1
10EAB[	1	56	10EBA
1LEAB[	2	55	] 1LEBA
1CEAB[	3	54	] 1CEBA
GND[	4	53	] GND
1A1[	5	52	] 1B1
1A2[	6	51	] 1B2
Vcc[	7	50	] v <sub>cc</sub>
1A3[]	8	49	] 1B3
1A4[	9		] 1B4
1A5[]	10	47	] 1B5
GND[]	11	46	] GND
1A6[]	12	45	] 1B6
1A7[	13	44	] 1B7
1A8[]	14		
2A1 🛛	15	42	] 2B1
2A2[]	16	41	2B2
2A3[]	17	40	] 2B3
GND[]	18	39	] GND
2A4[]	19	38	] 2B4
2A5[	20	37	2B5
2A6	21	36	
Vcc	22	35	] v <sub>cc</sub>
2A7	23	34	] 2B7
2A8[]	24	33	] 2B8
GND	25	32	] GND
2CEAB[]	26	31	2CEBA
2LEAB	27	30	2LEBA
20EAB[	28	29	] 20EBA

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16543 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16543 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16543 is characterized for operation from -40°C to 85°C.

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# SN54ABT16543, SN74ABT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS087A-D3798, FEBRUARY 1991-REVISED OCTOBER 1992

#### **FUNCTION TABLE†** (each 8-bit section)

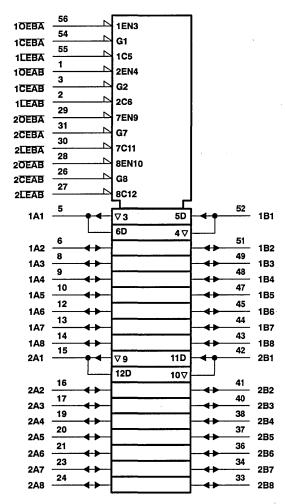
	INPL		OUTPUT	
CEAB	LEAB	OEAB	Α	В
Н	X	X	Х	Z
×	X	н	X	Z
L	Н	L	X	B <sub>0</sub> ‡
L	L	Ł	L	L
L	L	L	Н	н

<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

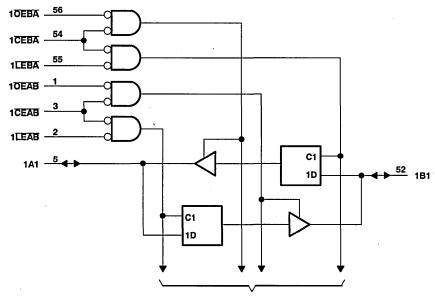
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# logic symbol†

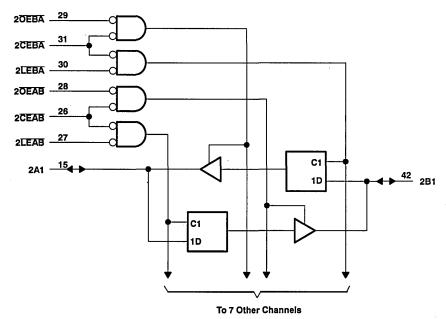


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



To 7 Other Channels



### SN54ABT16543, SN74ABT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS087A-D3798, FEBRUARY 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, $V_0$ $-0.5$ V to 5.5 V
Current into any output in the low state, Io: SN54ABT16543
SN74ABT16543
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air)
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16543	SN74ABT16543		UNIT
			MIN	MIN MAX MIN MAX			
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V	
VI	Input voltage		0	Vcc	0	Vcc	V
1он	High-level output current			-24		-32	mA
loL	Low-level output current		Ti	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# SN54ABT16543, SN74ABT16543 **16-BIT REGISTÉRED TRANSCEIVERS** WITH 3-STATE OUTPUTS

SCBS087A-D3798, FEBRUARY 1991-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	750	T CONDITIO	NO.	T	A = 25°C	;	SN54AB	T16543	SN74ABT16543		
PARAMETER	155	T CONDITIO	ons	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 m/	A	2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 m/	A	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 n	nA	2			2				· •
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 n	nA	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA	\			0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA		\			0.55‡				0.55	\ \ \
	$V_{CC} = 5.5 \text{ V},$		Control inputs			±1		±1		±1	μА
li li	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μ.Α.
I <sub>OZH</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$				50		50		50	μА	
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				50		-50		-50	μΑ	
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$	.5 V			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	$V_0 = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 \text{ V}$		-50	-100	-200	50	-200	-50	-200	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	ports	Outputs low			35		35		35	mA
	$V_I = V_{CC}$ or GND	Ports	Outputs disabled			2		2		2	
Δlcc#	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				0.5		0.5		0.5	mA	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs			3						pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		8.5						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> =	= 5 V, 25°C	SN54AB	Г16543	SN74AB	16543	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LEAB or LEBA low		4		4		4		ns
	Setup time, data before LEAB† or LEBA†	High	1.5		1.5		1.5		ns
t <sub>su</sub>	Setup time, data before LEAB   or LEBA	Low	3.5		3.5		3.5		
t <sub>h</sub> Hold time, data after LEAB↑ or LEB	Hold time, data after LEADA or LEDAA	High	1.5		1.5		1.5		ns
	Hold time, data after LEAD   Of LEBA	Low	2		2		2		115

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.
 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

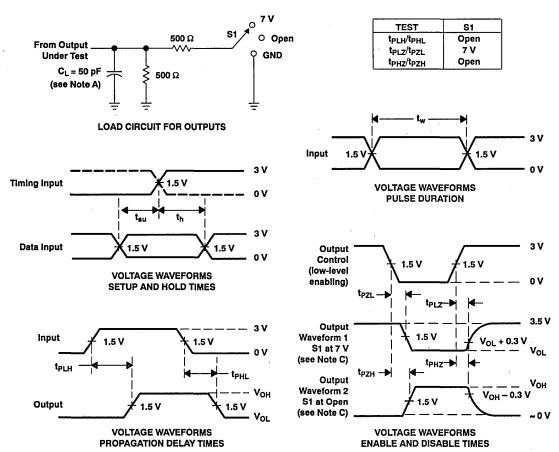
<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT16543, SN74ABT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS087A-D3798, FEBRUARY 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то (оитрит)		V <sub>CC</sub> = 5 V, T <sub>Δ</sub> = 25°C			SN54ABT16543		SN74ABT16543	
	(INPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	2.5	3.3	1	3.9	1	3.8	
t <sub>PHL</sub>	AOFB	B of A	1	2.7	4.4	1	5.2	1	5.1	ns
t <sub>PLH</sub>	LE .	A or B	1	3.1	4.3	1	5.3	1	5.2	ns
t <sub>PHL</sub>	LE	A OI B	1.2	3.3	4.8	1.2	5.7	1.2	5.6	115
t <sub>PZH</sub>	OE	A or B	1	3.4	4.3	1	5.3	1	5.2	ns
t <sub>PZL</sub>	OE.	AOIB	1.1	3.8	5.9	1.1	7.1	1.1	7	
t <sub>PHZ</sub>	ŌĒ	A or B	1.9	4	5	1.9	7.2	1.9	5.7	ns
t <sub>PLZ</sub>	OE.	Aorb	1.6	3.3	4.2	1.6	5	1.6	4.6	115
t <sub>PZH</sub>	CE	A or D	1	3.8	4.9	. 1	6.3	1	6.2	
t <sub>PZL</sub>	CE	A or B	1.2	4.2	6.5	1.2	7.9	1.2	7.8	ns
t <sub>PHZ</sub>	hu -	A D	2	4.5	5.6	2	7.3	2	6.6	
t <sub>PLZ</sub>	CE	A or B	1.7	3.9	5.1	1.7	5.6	1.7	5.4	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

SN54ABT16600...WD PACKAGE SN74ABT16600...DL PACKAGE (TOP VIEW)

	_	_	_	•
OEABI	1	U	56	H CEKENAB
LEAB	2		55	CLKAB
	3		54	2
GND	4		53	F
A2 🛚			52	Б B2
A3 🗍	6		51	Б вз
V <sub>cc</sub> ]	7		50	[] v <sub>cc</sub>
A4 🗍	8		49	
A5 🛚	9		48	B5
A6[	10		47	B6
GND [	11		46	] GND
A7 [	12		45	B7
A8[	13		44	] B8
A9[	14		43	B9
A10[	15		42	<u>Б</u> В10
A11 [	16		41	B11
A12[	17		40	] B12
GND [	18		39	] GND
A13[	19		38	] B13
A14[	20		37	] B14
A15[	21		36	] B15
Vcc[	22		35	] v <sub>cc</sub>
A16[	23		34	] B16
A17[	24		33	B17
GND [	25		32	] GND
A18[	26		31	] B18
OEBA [	27		30	] CEKBA
LEBA[	28		29	CLKENBA
				•

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16600 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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JUNE 1992-REVISED OCTOBER 1992

#### description (continued)

The SN54ABT16600 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT16600 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

	INPUTS								
CLKENAB	OEAB	LEAB	CLKAB	Α	В				
Х	Н	Х	Х	×	Z				
Х	L	Н	X	L	L				
Х	L	н	Х	Н	н				
н	L	L	X	X	B₀‡				
Н	L	L	Х	X	B₀‡				
L	L	L	1	L	L				
L	L	L	1	Н	н				
L	L	L	Н	X	В <sub>0</sub> ‡				
L	L	L	L	X	B <sub>o</sub> §				

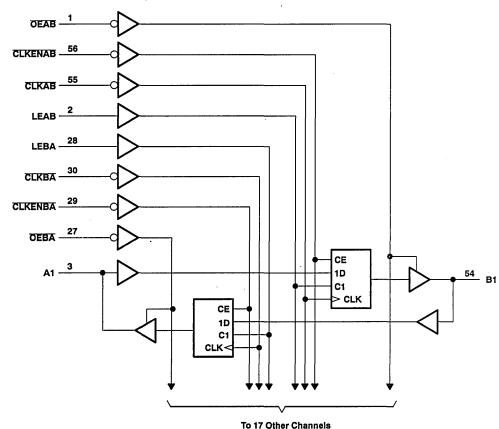
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

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#### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	$\dots$ –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$\dots$ -0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	. $$ $-0.5$ V to 5.5 V
Current into any output in the low state, Io: SN54ABT16600	96 mA
SN74ABT16600	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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#### recommended operating conditions (see Note 2)

			SN54ABT16600		SN74AB	SN74ABT16600	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage `		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	750	TEST CONDITIONS			A = 25°0	•	SN54ABT	16600	SN74ABT16600		UNIT
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	MAX	MIN	MAX	וואטן
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 3 m	nA	2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 m	ıA	3			3		3		<sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24	mA	2			2				1 * I
	V <sub>CC</sub> = 4.5 V,	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA							2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 m	A			0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55 <sup>‡</sup>				0.55	1 * I
lį	V <sub>CC</sub> = 5.5 V, Control inputs				±1		±1		±1	μА	
	$V_I = V_{CC}$ or GND A or B ports					±100		±100		±100	ן איין
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤	4.5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 9	5.5 V	Outputs high			50		50,		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A D	Outputs high			2		2		2	
Icc	$I_{O}=0$ ,	A or B	Outputs low			35		35		35	mA
	$V_I = V_{CC}$ or GND	Ports	Outputs disabled			. 2		2		2	j l
Δl <sub>CC</sub> #	$V_{CC} = 5.5 \text{ V}$ , One in Other inputs at $V_{CC}$		•			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs									pF
C <sub>lo</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	<i>'</i>	A or B ports								pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

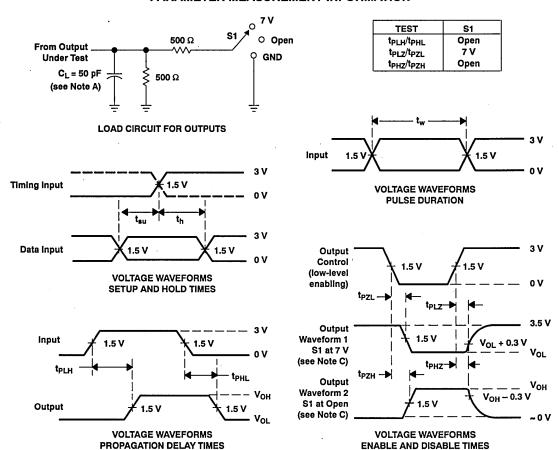
JUNE 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		1		SN54ABT16600		SN74AB	UNIT	
				MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
	Dulas dimedias	LEAB or LEBA high						`
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low	igh or low					ns
		A before CLKAB						
	O a to on the a	B before CLKBA↓						
t <sub>su</sub>	Setup time	A hefere I FARL or B hefere I FRAI	CLK high					ns
		A before LEAB↓ or B before LEBA↓	CLK low					
	11-14-2	A after CLKAB tor B after CLKBAt						
t <sub>h</sub>	Hold time	A after LEAB1 or B after LEBA1						ns

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

JUNE 1992-REVISED OCTOBER 1992

- **Members of the Texas Instruments** Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- **UBT** ™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 5 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

SN54ABT16601...WD PACKAGE SN74ABT16601...DL PACKAGE (TOP VIEW)

			1
OEAB [	<sub>1</sub> U	56	CLKENAB
LEAB [	2	55	] CLKAB
A1 [		54	] B1
GND [	4	53	GND
A2 [		52	] B2
A3 [			] B3
Vcc [		50	]V <sub>cc</sub>
A4 [			] B4
A5 [	9	48	] B5
A6 [	10	47	] B6
GND [	11	46	GND
A7 [	12	45	] B7
A8 [	13	44	] B8
A9 [	14.	43	] B9
A10 [	15	42	] B10
A11 [	16	41	] B11
A12 [			B12
GND [	18		] GND
A13 [	19	38	] B13
A14 [	20	37	] B14
A15 [	21	36	B15
Vcc [	22	35	] v <sub>cc</sub>
A16 [	23	34	] B16
A17 [	24	33	B17
GND [	25	32	GND
A18 [	26	31	B18
OEBA [	27	30	CLKBA
LEBA [	28	29	CLKENBA

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down, OE should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16601 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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# SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### description (continued)

The SN54ABT16601 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT16601 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

	INPUTS						
CLKENAB	OEAB	LEAB	CLKAB	Α	В		
Х	Н	Х	Х	Х	Z		
Х	L	Н	X	L,	L		
Х	L	Н	X	Н	н		
н	,L	L	X	X	B₀‡		
н	L	L	X	X	В <sub>0</sub> ‡ В <sub>0</sub> ‡		
L	L	L	<b>†</b>	L	L		
L	L	L	†	н	н		
L	L	L	L	X	B₀‡		
L	L	L	Н	X	B₀§		

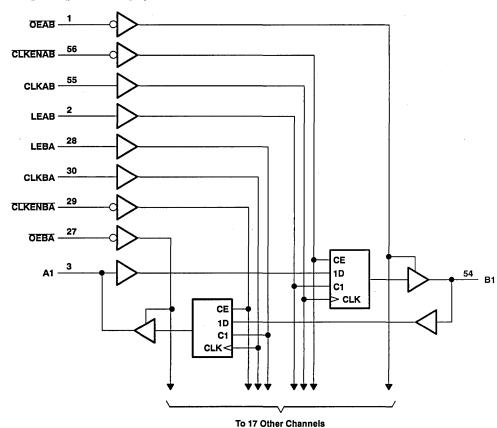
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

D3855, APRIL 1991-REVISED OCTOBER 1992

#### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	. $-0.5 \text{ V}$ to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16601	96 mA
SN74ABT16601	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	−50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

JUNE 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54ABT16601		SN74AB	T16601	UNIT
		•	MIN	MAX	MIN	MAX	UNII.
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		٧
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current		Î	-24		-32	mA
loL .	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	i	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				T	A = 25°0	2	SN54ABT	16601	SN74ABT16601		
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 m/	4			-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 r	nA	2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 r	nA	3			3		3		1 <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24	mA	2			2				1 °
	V <sub>CC</sub> = 4.5 V,	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$					<del></del>		2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 m	A			0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55 <sup>‡</sup>				0.55	1 °
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
lį	V <sub>I</sub> = V <sub>CC</sub> or GND A or B ports					±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.7 V	•			50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		50		-50	μА
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤	4.5 V			±100	, ,			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> =	5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	•	50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			35		35		35	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	Ports	Outputs disabled			2		2		2	1
Δl <sub>CC</sub> #	$V_{CC}$ = 5.5 V, One in Other inputs at $V_{CC}$		,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs									pF	
C <sub>io</sub>	Vo = 2.5 V or 0.5 V	/	A or B ports								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

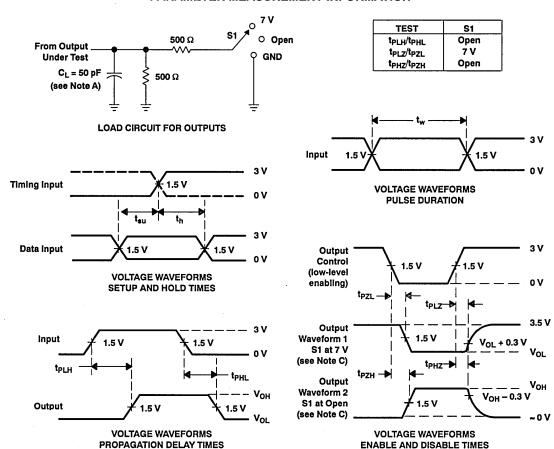
# SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT16601		SN74AB	UNIT	
				MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
A	Pulse duration	LEAB or LEBA high						
t <sub>w</sub>	ruise duration	CLKAB or CLKBA high or low		1			ns	
•		A before CLKAB↑					,	
	Catum times	B before CLKBA↑						
t <sub>su</sub>	Setup time	A before I EARL or B before I ERAL	CLK high					ns
		A before LEAB or B before LEBA	CLK low					Ì
4.	Hold time	A after CLKAB† or B after CLKBA†						
th	חטום נוווופ	A after LEAB or B after LEBA		Ī				ns

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

### SN54ABT16623, SN74ABT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3799, FEBRUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16623 is a 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'ABT16623 provides true data at its outputs.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and OEBA. Each output reinforces its input in this configuration. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (32 in all) will remain at their last states.

SN54ABT16623...WD PACKAGE SN74ABT16623...DL PACKAGE (TOP VIEW)

	-		
10EAB[	<sub>1</sub> 0		1 <del>OEBA</del>
1B1 [			] 1A1
1B2			] 1A2
GND [			GND
1B3			] 1A3
1B4			] 1A4
v <sub>cc</sub> [			] ∨ <sub>cc</sub>
1B5 🏻			1A5
1B6			1A6
GND [			GND
1B7			] 1A7
1B8			] 1A8
2B1 🛚			2A1
2B2 🛚			2A2
GND			] GND
2B3 🛚			2A3
2B4 🛚			] 2A4
v <sub>cc</sub> [			] v <sub>cc</sub>
2B5 🛚			2A5
2B6 🛚			2A6
GND			GND
2B7			2A7
2B8 [			2A8
20EAB [	24	25	20EBA

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16623 is packaged in Ti's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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#### description (continued)

The SN54ABT16623 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16623 is characterized for operation from  $-40^{\circ}$ C to 85°C.

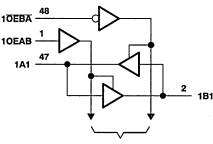
FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION
OEBA	OEAB	PERATION
L	L	B data to A bus
L	н	B data to A bus, A data to B bus
Н	L	Isolation
Н	Н	A data to B bus

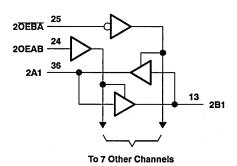
# logic symbol†

#### 10EBA EN1 1 10EAB EN<sub>2</sub> 25 20EBA EN<sub>3</sub> 24 20EAB EN4 2 1B1 1A1 **⊽ 1** 1 1 2 🗸 46 1A2 1B2 44 1A3 1B3 43 6 1A4 1B4 41 8 1A5 1B5 40 9 1A6 1B6 38 1A7 1B7 37 12 1A8 1B8 36 13 2A1 2B1 1 4 ▽ 35 14 2B2 2A2 33 16 **2A3** 2B3 32 17 2A4 2B4 30 19 2A5 2B5 29 20 2A6 2B6 27 22 2B7 2A8 2B8

# logic diagram (positive logic)



To 7 Other Channels



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### SN54ABT16623, SN74ABT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3799, FEBRUARY 1991-REVISED OCTOBER 1992

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	−0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16623	96 mA
SN74ABT16623	
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		-	SN54AB	T16623	SN74ABT16623		UNIT
			MIN	MAX	MIN	MAX	ONII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2	34	2		V
V <sub>IL</sub>	Low-level input voltage			<i>‰</i> 0.8		0.8	V
VI	Input voltage		0,4	₹ V <sub>CC</sub>	0	Vcc	V
Юн	High-level output current		Ş	-24		-32	mA
loL	Low-level output current		N.	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S. T.	5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# SN54ABT16623, SN74ABT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3799, FEBRUARY 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT16623		SN74ABT16623		UNIT	
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	٧		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5			2.5		2.5			
	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3		v	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				, v	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA			2‡					2			
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA					0.55		0.55			· · ·	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55 <sup>‡</sup>			Ì	0.55	٧	
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1				±1	J	
l <sub>i</sub>	$V_I = V_{CC}$ or GND		A or B ports			±100		₹100		±100	μА	
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	= 5.5 V, V <sub>O</sub> = 2.7 V				50		<i>5</i> 4 50		50	μА	
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V					-50	^ ا	∛` –50		-50	μА	
loff	$V_{CC} = 0 \text{ V}, \qquad V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$					±100	્ડ			±100	μА	
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ	
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	100	-180	€50	180	-50	-180	mA	
	V <sub>CC</sub> = 5.5 V,	A or B ports	Outputs high			2	-	2	,	2		
lcc	$I_{O} = 0$ ,		Outputs low			35		35		35	mA	
	$V_i = V_{CC}$ or GND		Outputs disabled			2		2		2		
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One	V, Data inputs	Outputs enabled			1		1.5		1		
	input at 3.4 V, Other inputs at		Outputs disabled			0.05		0.05		0.05	mA	
	V <sub>CC</sub> or GND Control inputs					1.5		1.5		1.5		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inp		Control inputs		3						pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		8						pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (INPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16623		SN74ABT16623		UNIT	
	( 51)	(00.1.0.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A or B	B or A	1	2	3.2	1 ,	3.7	1	3.6	ns	
t <sub>PHL</sub>			1	2.2	3.4	1,0	4.4	1	4.3		
t <sub>PZH</sub>	OEBA or OEAB	A or B	A or B 1.1 3 4 1.0 8		1.1	4.9	ns				
t <sub>PZL</sub>		AUID	1.4	3.3	4.9	21:4/4	6.2	1.4	6	113	
t <sub>PHZ</sub>	OEBA or OEAB	OEBX or OEAB	A or B	1	3.5	4.9	` €`	6.2	1	6	ns
t <sub>PLZ</sub>		7010	1.4	2.8	4.7	1.4	5.6	1.4	5.4	113	

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

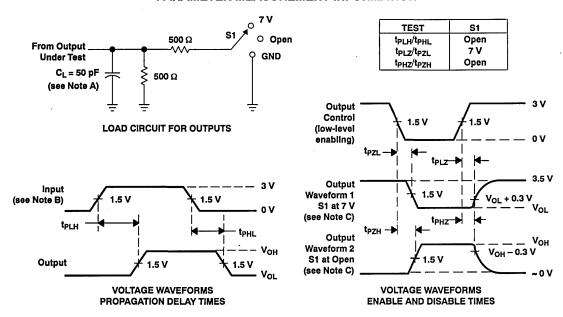
<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT16640, SN74ABT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS107A-D3999, APRIL 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable (1OE and 2OE) inputs can be used to disable the device so that the buses are effectively isolated.

SN54ABT16640... WD PACKAGE SN74ABT16640... DL PACKAGE (TOP VIEW)

1DIR[	1		10E
1B1[	2	47	] 1A1
1B2[	3	46	] 1A2
GND[	4	45	GND
1B3[	5	44	] 1A3
1B4[	6		] 1A4
Vcc	7		] v <sub>cc</sub>
1B5	8		] 1A5
1B6	9	40	] 1A6
GND[	10	39	GND
1B7[	11	38	] 1A7
1B8	12	37	] 1A8
2B1[	13	36	] 2A1
2B2	14	35	] 2A2
GND[	15		GND
2B3		33	2A3
2B4			2A4
Vcc			] v <sub>cc</sub>
2B5			2A5
2B6	20		2A6
GND[]	21		] GND
2B7	22		2A7
2B8[]	23		2A8
2DIR[]	24	25	20E

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16640 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16640 is characterized for operation from –40°C to 85°C.

## FUNCTION TABLE (each section)

INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

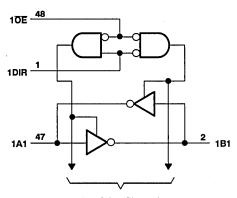
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## SN54ABT16640, SN74ABT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

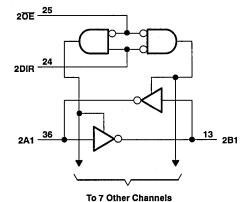
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#### logic symbol<sup>†</sup> 10E G3 1DIR 3 EN1 [BA] 3 EN2 [AB] 25 G6 20E 24 2DIR 6 EN4 [BA] 6 EN5 [AB] 1B1 1A1 1 2 ▽ 1B2 1A2 44 5 1A3 1**B**3 6 43 1A4 1**B**4 8 1A5 1**B**5 9 40 1A6 1**B**6 38 11 1A7 **1B7** 37 12 1B8 1A8 36 13 2A1 **⊽**4 2B1 1 1 5 ▽ 35 14 2B2 2A2 16 33 2A3 2B3 17 32 2A4 2B4 30 19 2B5 2A5 29 20 2A6 2B6 27 22 2A7 2B7 23 2A8 2B8

### logic diagram (positive logic)



To 7 Other Channels



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16640	96 mA
SN74ABT16640	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	0.85 W
Storage temperature range	-65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16640	SN74AB	T16640	UNIT
			MIN	MAX	MIN	MAX	ONII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage		2	8	√2		٧
V <sub>IL</sub>	Low-level input voltage			<i>‰</i> 0.8		8.0	٧
V <sub>i</sub>	Input voltage		0,5	V <sub>CC</sub>	0	Vcc	٧
loH	High-level output current		ζ.	-24		-32	mA
loL	Low-level output current		, Q	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	SE	10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		~55	125	-40	85	ပ္

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T	A = 25°C	;	SN54ABT16640		SN74ABT16640		UNIT
PARAMETER	'E	SI CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	וואט
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		l v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m.	A	2			2				
	$V_{CC} \approx 4.5 \text{ V},$	I <sub>OH</sub> = - 32 m.	A	2‡					2		I
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
VoL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡		4		0.55	ľ
	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		Control inputs			±1		<u></u> ≪±1		±1	μА
11			A or B ports		±10		<u>≪</u> ≇100			±100	μ.
l <sub>ozh</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	V <sub>O</sub> = 2.7 V			50				50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50	Ç	-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100	TO ONLY			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Ŗ	50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	~50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			32		32		32	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data innut-	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	nput at 3.4 V, Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND Control inputs		s			1.5		1.5		1.5	1
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	•	Control inputs		3						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V	,	A or B ports		8						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

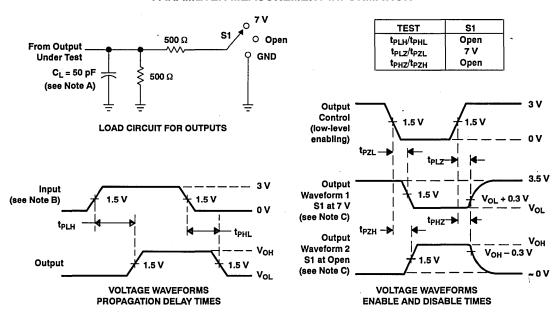
<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS107A-D3999, APRIL 1992-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER ·	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16640		SN74ABT16640	
	( 51)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1	2.5	3.4	1 人	4.4	1	4.3	ns
t <sub>PHL</sub>	] ^015		1.1	2.8	3.6	1.18	\$ 4	1,1	3.9	
t <sub>PZH</sub>	ŌĒ	A or B	1.2	3.5	4.5	1825	5.6	1.2	5.5	ns
t <sub>PZL</sub>			1.5	3.9	5	<b>⊘</b> 1.5%	6.4	1.5	6.3	115
t <sub>PHZ</sub>	ÖΕ	ŌE A or B	1.8	3.8	4.8	1.8	6.5	1.8	6.3	ns
t <sub>PLZ</sub>			1.5	3	3.9	1.5	4.4	1.5	4.2	

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

JUNE 1992-REVISED OCTOBER 1992

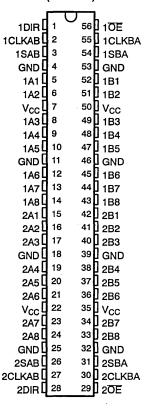
- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16646.

SN54ABT16646...WD PACKAGE SN74ABT16646...DL PACKAGE (TOP VIEW)



Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16646 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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## SN54ABT16646, SN74ABT16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### description (continued)

The SN54ABT16646 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16646 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE**

INPUTS						DAT	A I/O	OPERATION OR FUNCTION		
ŌĒ	OE DIR CLKA		LKAB CLKBA		SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTIO		
X	×	Ť	Х	×	X	Input	Unspecified <sup>†</sup>	Store A, B unspecified†		
Х	X	X	1	X	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified†		
Н	Х	Ť	1	Х	Х	Input	Input	Store A and B data		
Н	X	L	L	Х	Х	Input disabled	Input disabled	Isolation, hold storage		
L	L	. X	Х	×	L	Output	Input	Real-time B data to A bus		
L	L	X	L	X	Н	Output	Input	Stored B data to A bus		
L	Н	X	Х	L	Х	Input	Output	Real-time A data to B bus		
L	Н	Ł	X	н	Х	Input	Output	Stored A data to B bus		

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



JUNE 1992-REVISED OCTOBER 1992 BUS B CLKAB CLKBA SAB SBA OE DIR CLKBA SBA х L L Н Х Х Х **REAL-TIME TRANSFER REAL-TIME TRANSFER BUS B TO BUS A BUS A TO BUS B** BUSA BUSB  $\boldsymbol{\omega}$ CLKAB CLKBA SAB SBA ŌΕ DIR CLKAB CLKBA SAB SBA Х Х Х Х Н

Н

X

TRANSFER STORED DATA

TO A AND/OR B

Х

BUSA

OE

**BUSA** 

OE X

Х

DIR

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t STORAGE FROM

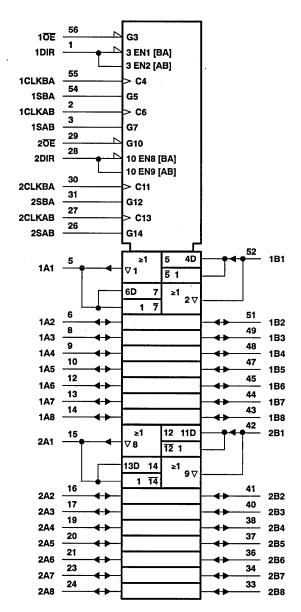
A, B, OR A AND B

Figure 1. Bus Management Functions



JUNE 1992-REVISED OCTOBER 1992

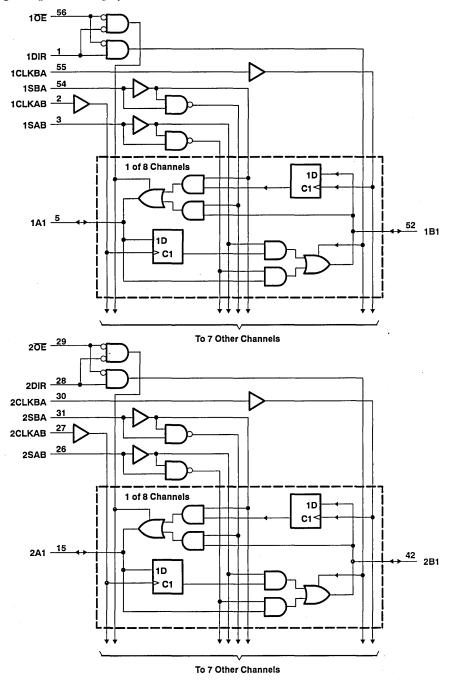
logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



### logic diagram (positive logic)





JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings	over operating tree-air	temperature range	(unless otherwise noted)
Supply voltage range, Voc.			0 5 V to 7 V

Supply voltage range, vcc	-0.5 V to / V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16646	96 mA
SN74ABT16646	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	18 mA
Output clamp current, $I_{OK}(V_O < 0)$	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54AB	T16646	SN74AB	UNIT	
İ			MIN	MAX	MIN	MAX	ONII
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TEST CONDITIONS			A = 25°C	;	SN54ABT16646		SN74ABT16646		דואט
PARAMETER	lest conditions			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	ONIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m	A	2			2	-			•
1	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m}.$	A	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	l <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
1.	V <sub>CC</sub> = 5.5 V,	Control inputs			±1		±1		±1	μА	
lı 	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	[ [
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
I <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ	
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μA
1 <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			72		72		30	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data innuts	Outputs enabled			1		1.5		1	
Δlcc#	input at 3.4 V, Data inputs Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND Control input		3			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs								pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,	A or B ports								pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

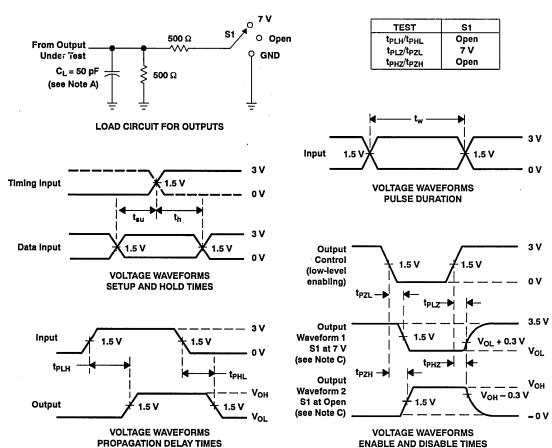
<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>&</sup>lt;sup>¶</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Lavout
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16648 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16648.

SN54ABT16648...WD PACKAGE SN74ABT16648...DL PACKAGE (TOP VIEW)

1DIR [	, U	56	10E
1CLKAB			1CLKBA
1SAB			1SBA
GND [			GND
1A1 [			1B1
1A2 [			1B2
v <sub>cc</sub> [		50	V <sub>cc</sub>
1A3 🛚	8	49	1B3
1A4 [	9	48	] 1B4
1A5 🛚	10		] 1B5
GND [	11		] GND
1A6 🛚	12	45	] 1B6
1A7 [			1B7
1A8 [			1B8
2A1 [			] 2B1
2A2 🛚			2B2
2A3 🛚		40	2B3
GND [			] GND
2A4 🛚			2B4
2A5 🛚			2B5
2A6 🛚			2B6
v <sub>cc</sub> [		35	V <sub>cc</sub>
2A7 🛚			2B7
2A8 🛚			2B8
GND			GND
		31	2SBA
2CLKAB			2CLKBA
2DIR L	28	29	20E

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus will receive data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16648 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16648 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16648 is characterized for operation from  $-40^{\circ}$ C to 85°C.

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# SN54ABT16648, SN74ABT16648 16-BIT TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SEPTEMBER 1992-REVISED OCTOBER 1992

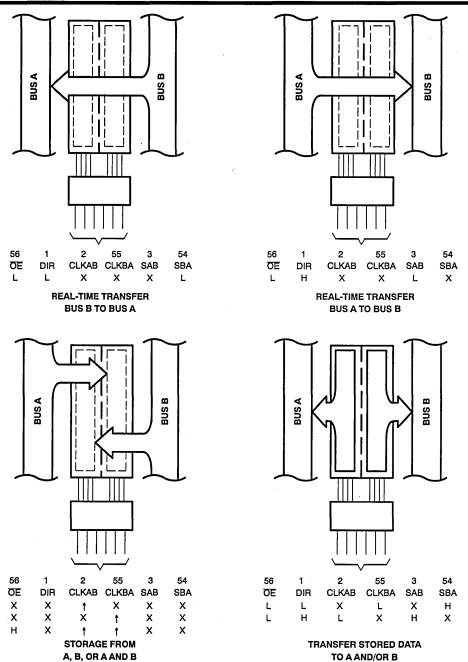
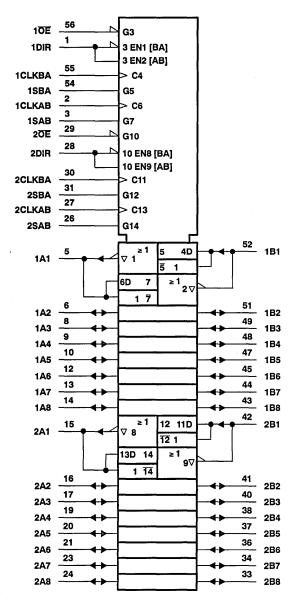


Figure 1. Bus-Management Functions



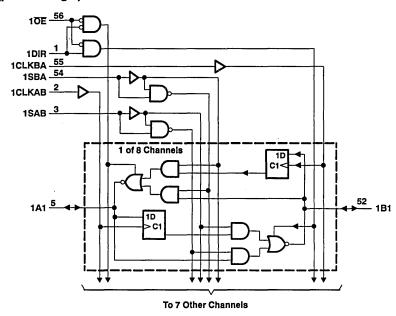
## logic symbol†

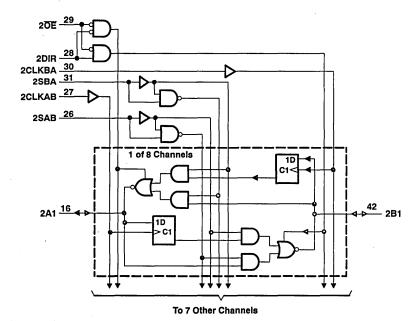


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT16648, SN74ABT16648 16-BIT TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SEPTEMBER 1992-REVISED OCTOBER 1992

## logic diagram (positive logic)







SEPTEMBER 1992-REVISED OCTOBER 1992

## FUNCTION TABLE (each 8-bit section)

-		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION
ŌE	DIR	CLKAB	CLKBA	SAB SBA		A1 THRU A8	B1 THRU B8	OPERATION OF FUNCTION
X	Х	<b>†</b>	X	Х	Х	Input	Unspecified <sup>†</sup>	Store A, B unspecified†
x	Х	X	1	X	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>
Н	Х	<b>†</b>	†	X	X	Input	Input	Store A and B data
н	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L.	L	Х	Х	X	L	Output	Input	Real-time B data to A bus
L	L	X	Ł	X	Н	Output	Input	Stored B data to A bus
L	н	X	X	L	X	Input	Output	Real-time A data to B bus
L_L	Н	L	Х	н	Х	Input	Output	Stored A data to B bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16648	96 mA
SN74ABT16648	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range –	65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16648	SN74AB	UNIT	
		MIN	MAX	MIN MAX		] "	
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		T <sub>A</sub> = 25°C			SN54ABT16648		SN74ABT16648				
PARAMETER	'E	TEST CONDITIONS					MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA	I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	2.5			2.5		2.5				
V	V <sub>CC</sub> = 5 V,	3			3		3				
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	. 2			2				V		
	V <sub>CC</sub> = 4.5 V,	2‡					2				
	V <sub>CC</sub> = 4.5 V,			0.55		0.55			·		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>				0.55	V
1.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	4
lį	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			72		72		30	mA
	$V_I = V_{CC}$ or GND		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Detectorists	Outputs enabled			1		1.5		1	
Δlcc#	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled	Outputs disabled 0.05			0.05		0.05	mA	
	V <sub>CC</sub> or GND	Control inputs	3			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			_			_			pF	
Cio	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports								pF

 $<sup>^\</sup>dagger$  All typical values are at V<sub>CC</sub> = 5 V.  $^\ddagger$  On products compliant to MIL-STD-883, Class B, this parameter does not apply.

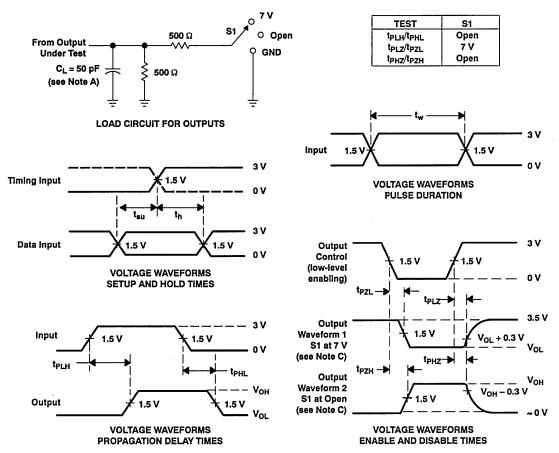
<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SEPTEMBER 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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OCTOBER 1992

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- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16651 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16651.

SN54ABT16651... WD PACKAGE SN74ABT16651... DL PACKAGE (TOP VIEW)

1			
10EAB	1	56	10EBA
ICLKAB	2		1CLKBA
1SAB	3	54	] 1SBA
GND [	4	53	GND
1A1 [		52	] 1B1
1A2 🛚		51	] 1B2
v <sub>cc</sub> [	7	50	] v <sub>cc</sub>
1A3 L	8	49	] 1B3
1A4 🛭	9		] 1B4
1A5 🛚	10		] 1B5
GND [	11	46	GND
1A6 🛚			] 1B6
1A7 🛭	13	44	
1A8 🛚			] 1B8
2A1 🛚		42	2B1
2A2 🛚		41	] 2B2
2A3 🛚		40	2B3
GND 🛚		39	] GND
2A4 🏻		38	2B4
2A5 🏻			2B5
2A6 🛚			2B6
v <sub>cc</sub> [		35	
2A7 🛚		34	
2A8 🛚	24	33	2B8
GND [		32	GND
2SAB 🛚		31	2SBA
CLKAB			2CLKBA
20EAB [	28	29	20EBA

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

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#### description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT16651 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16651 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16651 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

		INPU	TS			DAT	A I/O	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA A1 THRU A8 B1 THRU B8		OPERATION ON FUNCTION	
L	Н	H or L	H or L	X	X	Input	Input	Isolation
L	Н	1	t	X	X	Input	Input	Store A and B data
×	Н	t	H or L	X	Х	Input	Unspecified <sup>†</sup>	Store A, hold B
н	Н	t	t	X <sup>‡</sup>	Х	Input	Output	Store A in both registers
L	X	H or L	t	x	×	Unspecified <sup>†</sup>	Input	Hold A, store B
L	L	<b>†</b>	t	×	X‡	Output	input	Store B in both registers
L	L	X	X	×	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	×	н	Output	Output	Stored B data to A bus
Н	Н	X	X	L	×	Input	Output	Real-time A data to B bus
Н	Н	H or L	X	н	×	Input	Output	Stored A data to B bus
н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

<sup>\*</sup> When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.

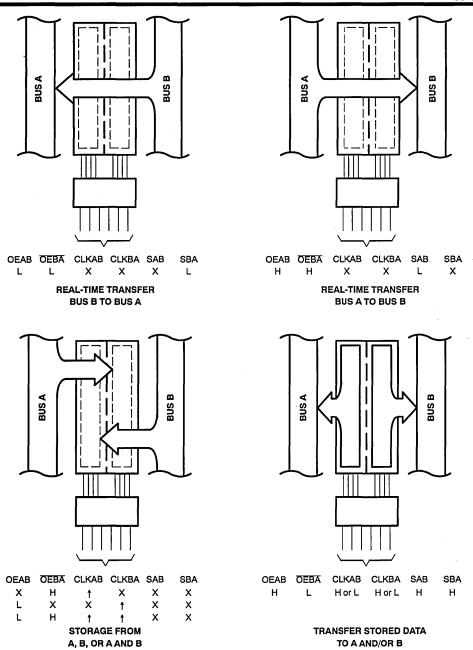
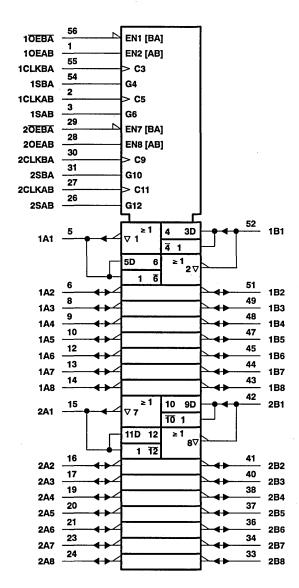


Figure 1. Bus-Management Functions



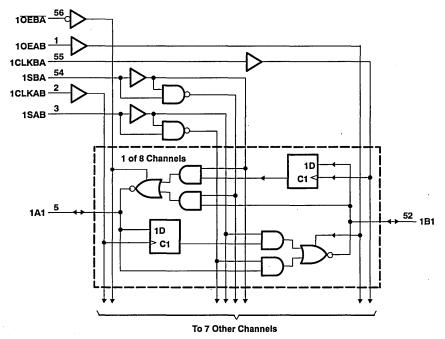
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### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



20EBA 20EAB -28 2CLKBA 30 2SBA 31 2CLKAB 1 of 8 Channels 15 2A1 42 2B1 1D To 7 Other Channels



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>1</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo	
Current into any output in the low state, Io: SN54ABT16651	
SN74ABT16651	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16651	SN74AB	T16651	UNIT
			MIN	MAX	MIN	MAX	ONIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	٧
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		55	125	-40	85	ů

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

BARAMETER		T	A = 25°C	;	SN54AB	T16651	SN74ABT16651		UNIT		
PARAMETER	123	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA		_		-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	2.5			2.5		2.5				
l v.	V <sub>CC</sub> = 5 V,	l <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	2			2				•		
	V <sub>CC</sub> = 4.5 V,	l <sub>OH</sub> = - 32 m	A	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	·
1	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	μА
h h	$V_I = V_{CC}$ or GND		A or B ports			±100		±100		±100	μΛ
I <sub>OZH</sub> \$	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	' <sub>O</sub> = 0.5 V			-50		-50		-50	μA
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μA
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low			72		72		30	mΑ
	$V_I = V_{CC}$ or GND		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data innuta	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control inputs	S			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs								pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	<i>-</i>	A or B ports								pF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

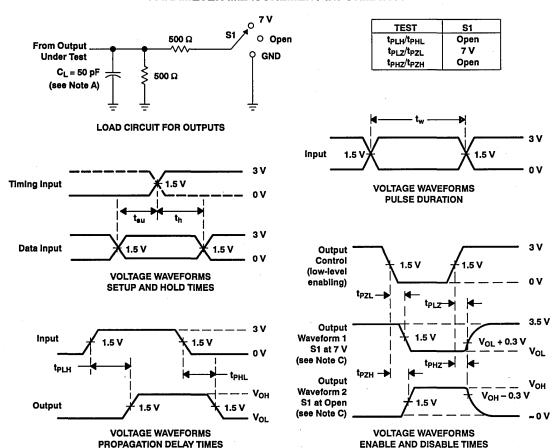
<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{<}$  10 MHz,  $Z_{o}$  = 50  $\Omega$ ,  $t_{f}$   $_{<}$  2.5 ns,  $t_{f}$   $_{<}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16652 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16652.

SN54ABT16652...WD PACKAGE SN74ABT16652...DL PACKAGE (TOP VIEW)

	_	_		
10EAB[	1	U	56	10EBA
1CLKAB	2		55	
1SAB [	3		54	_
GND [	4		53	GND
1A1 [	5		52	] 1B1
1A2 🗍	6		51	
V <sub>CC</sub> [	.7			] v <sub>cc</sub>
1A3 [	8			1B3
1A4 [	9		48	] 1B4
1A5 [	10		47	] 1B5
GND [	11		46	] GND
1A6 [	12		45	] 1B6
1A7 [	13		44	] 1B7
1A8 [	14		43	] 1B8
2A1 [	15		42	] 2B1
2A2 [	16		41	] 2B2
2A3 [	17		40	] 2B3
GND [	18		39	] GND
2A4 [	19		38	] 2B4
2A5 [	20		37	2B5
2A6 [	21		36	] 2B6
V <sub>CC</sub> [	22		35	] v <sub>cc</sub>
2A7 🛛	23		34	] 2B7
2A8 🛛	24		33	] 2B8
GND [	25			GND
2SAB[	26		31	] 2SBA
2CLKAB[	27			] 2CLKBA
20EAB [	28		29	20EBA

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

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#### description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN74ABT16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16652 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16652 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE**

		INPU	TS			DATA	A I/O†	ODERATION OR EUNOTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION		
L	Н	L	L.	×	Х	Input	Input	Isolation		
L	Н	1	1	X	Х	Input	Input	Store A and B data		
X	Н	1	L	X	х	Input	Unspecified <sup>‡</sup>	Store A, hold B		
Н	Н	1	1	X <sup>‡</sup>	x	Input	Output	Store A in both registers		
L	X	L	<b>†</b>	X	х	Unspecified <sup>‡</sup>	Input	Hold A, store B		
L	L	1	<b>†</b>	X	X‡	Output	Input	Store B in both registers		
L	Ĺ	X	X	X	L	Output	Input	Real-time B data to A bus		
L	L	X	L	X	н	Output	Input	Stored B data to A bus		
Н	Н	X	Х	L	×	Input	Output	Real-time A data to B bus		
Н	Н	L	X	Н	Х	Input	Output	Stored A data to B bus		
Н	L	L	L	н	н	Output	Output	Stored A data to B bus and stored B data to A bus		

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

Select control = H; clocks must be staggered in order to load both registers.

<sup>&</sup>lt;sup>‡</sup> Select control = L; clocks can occur simultaneously.

## SN54ABT16652, SN74ABT16652 **16-BIT BUS TRANSCEIVERS AND REGISTERS** WITH 3-STATE OUTPUTS D3800, FEBRUARY 1991-REVISED OCTOBER 1992

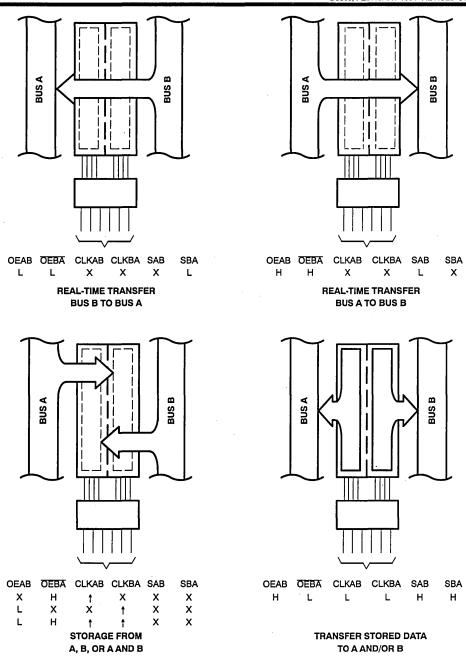
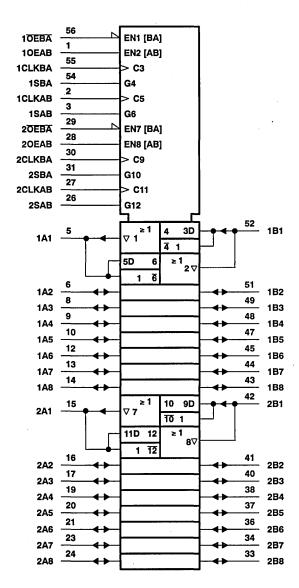


Figure 1. Bus-Management Functions



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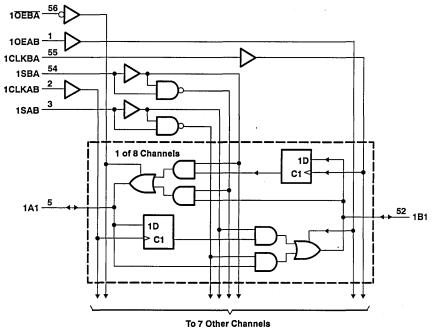
### logic symbol†

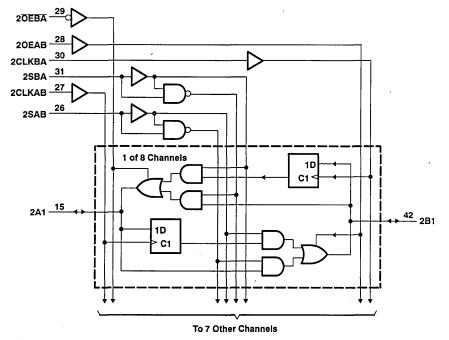


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



## logic diagram (positive logic)







D3800, FEBRUARY 1991-REVISED OCTOBER 1992

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16652	
SN74ABT16652	128 mA
Input clamp current, $I_{IK}$ ( $V_1 < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16652	SN74ABT16652		UNIT	
			MIN	MAX	MIN	MAX	UNII	
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage		2		2		٧	
VIL	Low-level input voltage			0.8		0.8	٧	
Vi	Input voltage		0	Vcc	0	Vcc	٧	
Іон	High-level output current			-24		-32	mA	
loL	Low-level output current			48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Î	10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETIONS		T <sub>A</sub> = 25°C			SN54ABT16652		SN74ABT16652		·		
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_1 = -18 \text{ mA}$					-1.2		-1.2		-1.2	V	
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			2.5			2.5		2.5		٧	
<sub>V</sub>	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3			
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -24 \text{ mA}$			2			2					
ļ	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2			
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55		0.55			٧	
V <sub>OL</sub>						0.55‡				0.55		
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1		
l <sub>l</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ	
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V					50		50		50	μΑ	
I <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$					-50		-50		-50	μА	
loff	V <sub>CC</sub> = 0 V,	5 V			±100				±100	μА		
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ	
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	100	-180	50	-180	-50	-180	mA	
	V <sub>CC</sub> = 5.5 V,	A or B ports	Outputs high			2		2		2	mA	
Icc	I <sub>O</sub> = 0,		Outputs low			72		72		30		
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			2		2		2		
	V <sub>CC</sub> = 5.5 V, One	Outputs enabled			1		1.5		1			
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA	
	V <sub>CC</sub> or GND Control inputs		S			1.5		1.5		1.5		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Cor		Control inputs								pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	1	A or B ports								pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>mbox{\$}$  The parameters  $\mbox{I}_{\mbox{\scriptsize OZH}}$  and  $\mbox{I}_{\mbox{\scriptsize OZL}}$  include the input leakage current.

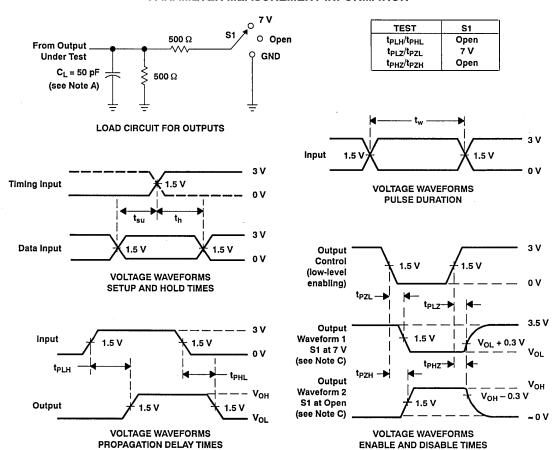
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

### SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

D3800, FEBRUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0$  = 50  $\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

### SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive (1T/R or 2T/R) input determines the direction of data flow. When 1T/R (or 2T/R) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/R (or 2T/R) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable (1ŌE or 2ŌE) input is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

SN54ABT16657...WD PACKAGE SN74ABT16657...DL PACKAGE (TOP VIEW)

	ľ	1 1		
10E[			56	] 1T/R
NC	2		55	10DD/EVEN
1ERR[	3		54	] 1PARITY
GND	4		53	GND
1A1[	5		52	] 1B1
1A2[	6		51	] 1B2
Vcc	7		50	] v <sub>cc</sub>
1A3[	8		49	] 1B3
1A4[	9		48	] 1B4
1A5[	10		47	] 1B5
GND	11		46	] GND
1A6[			45	] 1B6
1A7[	13		44	] 1B7
1A8[	14		43	] 1B8
2A1[	15		42	] 2B1
2A2[	16		41	] 2B2
2A3[	17			] 2B3
GND	18		39	] GND
2A4[	19		38	] 2B4
2A5[	20		37	] 2B5
2A6[	21			] 2B6
V <sub>CC</sub> [	22		35	] v <sub>cc</sub>
2A7[	23		34	] 2B7
2A8[	24		33	] 2B8
GND[	25		32	] GND
2ERR[			31	2PARITY
NC[	27			20DD/EVEN
20E[	28		29	] 2T/R

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/EVEN (or 2ODD/EVEN) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/EVEN (or 2ODD/EVEN) input. For example, if 1ODD/EVEN is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1ERR (or 2ERR) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/EVEN is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1ERR is low, indicating a parity error.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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## SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

#### description (continued)

The SN74ABT16657 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

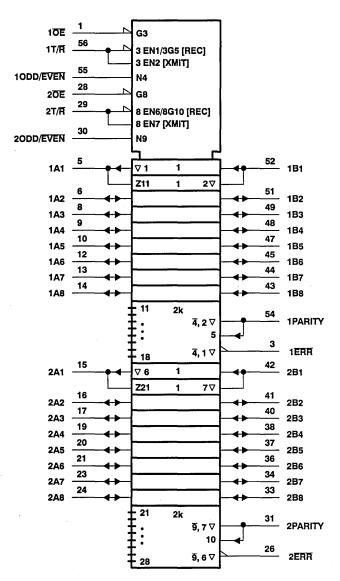
The SN54ABT16657 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16657 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE** (each 8-bit section)

NUMBER OF A OR B		INPUT	S	INFOI/OUTFOI		OUTPUTS
INPUTS THAT ARE HIGH	ŌE	T/R	ODD/EVEN	PARITY	ERR	OUTPUT MODE
	L	Н	Н	Н		Transmit
	L	н	L	L	z	Transmit
00468	L	L	н	н	н	Receive
0, 2, 4, 6, 8	L	L	н	L	L	Receive
	L	L	L	н	L	Receive
	L	L	L	L	н	Receive
	L	Н	Н	L	Z	Transmit
	L	Н	L	н	z	Transmit
1057	L	L	н	• н	L	Receive
1, 3, 5, 7	L	L	Ή	L	н	Receive
	L	L	L	н	Н	Receive
	L	L	L	L	L '	Receive
Don't care	Н	Х	X	Z	Z	Z

SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

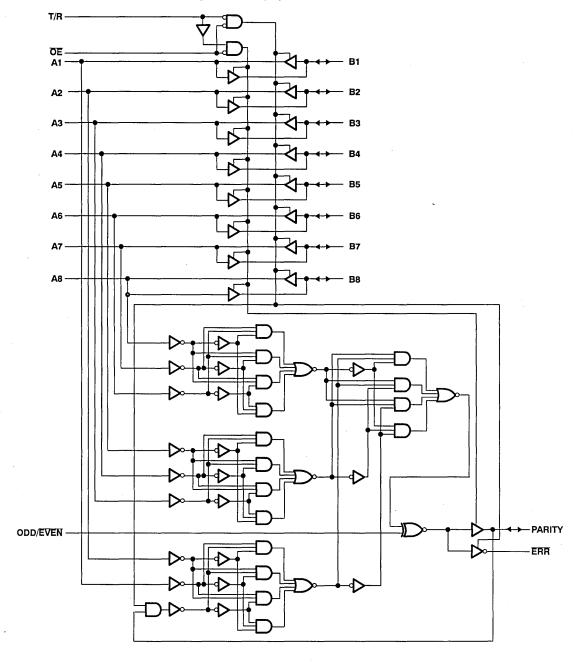
### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

### logic diagram, each transceiver (positive logic)



### SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>
Current into any output in the low state, Io: SN54ABT16657
SN74ABT16657
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54ABT	16657	SN74AB	Γ16657	1111
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	<sub></sub> 5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	24	2		V
V <sub>IL</sub>	Low-level input voltage	-	Á	0.8		0.8	V
Vı	Input voltage		0, 🔾	Vcc	0	Vcc	V
Гон	High-level output current		ڒؽۜ	-24		-32	mA
loL	Low-level output current		S	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Æ	10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS			A = 25°0	;	SN54AB	T16657	SN74ABT16657		UNIT
PARAMETER	163	SI CONDITIO	NS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5				V
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -		I <sub>OH</sub> = -24 mA				2				\ \
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m/s}$	\	2*					2		
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 24 mA					0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55*		40.		0.55	l *
1.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		<b>≪</b> 41		±1	μА
l <sub>l</sub>	$V_I = V_{CC}$ or GND		A or B ports			±100		<u>≪</u> ±100		±100	μ~
l <sub>IL</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> = GND	A or B ports			-50	,<			-50	μΑ
lozh‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	Ş	50		50	μΑ
l <sub>OZL</sub> ‡	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50	ŞÕ	-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	i V			±100	S.	±450		±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	- 14	50		50	μΑ
lo <sup>§</sup>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V		-50	-100	180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			36		36		36	mΑ
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			2		2		2	}
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>CC</sub>	One input at 3 or GND	.4 V,			50		50		50	μА
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs				3						pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		A or B ports		9						pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

<sup>\*</sup> On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

## SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

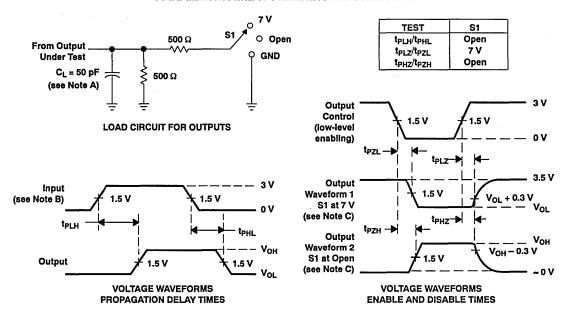
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

					_	•				
PARAMETER	FROM	FROM TO NPUT) (OUTPUT)		CC = 5 V A = 25°C		SN54ABT	16657	SN74AB	Γ16657	UNIT
	(INFOT)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	
t <sub>PHL</sub>	7 AUI B	BOLA	2	3.1	3.9	2	4.5	2	4.3	ns
t <sub>PLH</sub>	Α Α	PARITY	2	4.6	5.4	2	7	2	6.7	ns
t <sub>PHL</sub>	1 ^	PARITY	2	4.3	5.1	2	6.5	2	6.1	113
t <sub>PLH</sub>	ODD/EVEN	PARITY, ERR	2	4.6	5.4	2	, 7	2	6.7	ns
t <sub>PHL</sub>	ODD/EVEN	FARILT, ERR	2	4.3	5.1	2	<i>;</i> ;6.5	2	6.1	lis
t <sub>PLH</sub>	В	ERR	2	4.6	5.4	2	7	2	6.7	ns
t <sub>PHL</sub>	]	Enn	2	4.3	5.1	2 5	6.5	2	6.1	113
t <sub>PLH</sub>	PARITY	ERR	2	4.6	5.4	2.	7	2	6.7	ns
t <sub>PHL</sub>	- FADILI	Enn	2	4.3	5.1	2,32	6.5	2	6.1	
t <sub>PZH</sub>	- OE	A or B	2	3.9	4.9	,O*2	5.8	2	5.6	
t <sub>PZL</sub>	]	AOIB	2.5	4.3	5.1	Q 2.5	6.2	2.5	6	ns
t <sub>PHZ</sub>	OE	A or B	2	3.6	4.5	2	5.5	2	5.4	
t <sub>PLZ</sub>	]	A OF B	1.5	3	3.8	1.5	4.7	1.5	4.3	ns
t <sub>PZH</sub>	OE	PARITY, ERR	2	4	4.9	2	5.8	2	5.6	
t <sub>PZL</sub>	<u> </u>	FARILT, ERR	2.5	4.1	5.1	2.5	6.2	2.5	6	ns
t <sub>PHZ</sub>	ŌĒ	PARITY, ERR	1	3.5	4.5	1	5.5	1	5.4	
t <sub>PLZ</sub>	]	PARILIT, ERR	1.5	3	3.8	1.5	4.7	1.5	4.3	ns

### SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

SCBS103-D3983, FEBRUARY 1992-REVISED JUNE 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D4512, JUNE 1992-REVISED OCTOBER 1992

- **Members of the Texas instruments** Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF,
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V</li> at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA loi )
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 20-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The twenty flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

SN54ABT16821...WD PACKAGE SN74ABT16821 ... DL PACKAGE (TOP VIEW)

10E [	1	O	56	]1CLK
1Q1 [	2		55	] 1D1
1Q2 [	]з		54	1D2
GND [	4			GND
1Q3 [	5			] 1D3
1Q4 [	6		51	] 1D4
Vcc [	7		50	] v <sub>cc</sub>
1Q5 [	8		49	] 1D5
1Q6 [	9		48	] 1D6
1Q7 [	10		47	] 1D7
GND [	11			] GND
1Q8 [	12			] 1D8
1Q9 [				] 1D9
1Q10[	14		43	] 1D10
2Q1 [	15			]2D1
2Q2 [				] 2D2
2Q3 [				] 2D3
GND [	1			GND
2Q4 [	1			2D4
2Q5 [	1			2D5
2Q6				] 2D6
Vcc [				]V <sub>cc</sub>
2Q7 [			34	2D7
2Q8 [				2D8
GND [				] GND
2Q9 [	1			2D9
2Q10	1		30	2D10
20E [	28		29	]2CLK

A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16821 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16821 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16821 is characterized for operation from -40°C to 85°C.

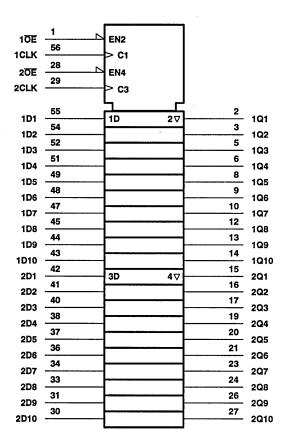
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D4512, JUNE 1992-REVISED OCTOBER 1992

## FUNCTION TABLE (each flip-flop)

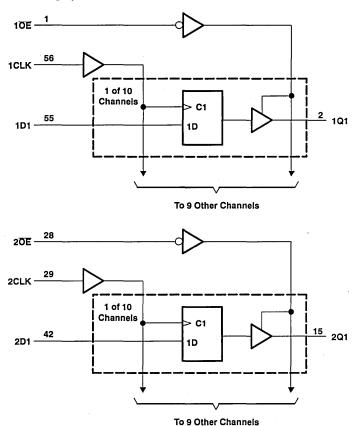
	INPUTS		OUTPUT
ŌĒ	CLK	D	a
L	t	Н	Н
L	<b>†</b>	L	L
L	L	Х	$Q_0$
н	X	X	z

### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	
Current into any output in the low state, Io: SN54ABT16821	96 mA
SN74ABT16821	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

D4512, JUNE 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16821	SN74AB	T16821	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	,25.5	4.5	5.5	V
VIH	High-level input voltage		2	S	2		V
VIL	Low-level input voltage			<b>9</b> 0.8		0.8	V
Vı	Input voltage		R.	Vcc	0	Vcc	٧
Тон	High-level output current		3	-24		-32	mA
loL	Low-level output current		् र	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Se.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T	T <sub>A</sub> = 25°C			T16821	SN74ABT16821		UNIT
PARAMETER	""	SI CONDIIIO	NS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	וואט
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA	\	2.5	-		2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA	\	3			3		3		ľv
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m.	A	2			2				ľ
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m}$	Α	2‡					2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡		ii.		0.55	ľ
l <sub>i</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or 0	GND			±1		_1± کیر		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.7 V				50	Ś	₹ 50		50	μΑ
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	$V_{CC} = 0 V$ ,	$V_1$ or $V_0 \le 4$ .	5 V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	,0"	50		50	μΑ
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.5 V		-50	-100	-200	₹ –50	-200	-50	-200	mA
	.,		Outputs high			500		500		500	μΑ
1 <sub>CC</sub>	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_0 = 0$ ,	Outputs low			89		89		89	mA
	A1 = ACC 01 C145		Outputs disabled			500		500		500	μΑ
ΔICC¶	$V_{CC} = 5.5 \text{ V}, O$ Other inputs at $V_{CC}$		V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3.5						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 \	/			7.5						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

D4512, JUNE 1992-REVISED OCTOBER 1992

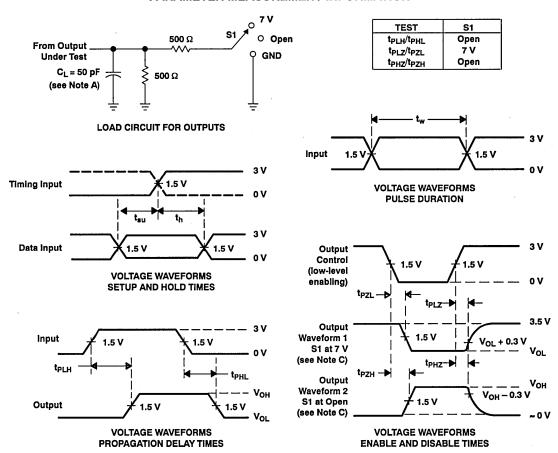
# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16821		SN74ABT16821		UNIT
		MIN I	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0,0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.80.	× -	3.3		ns
t <sub>su</sub>	Setup time, data before CLK†	1.8		\$17,80		1.8		ns
th	Hold time, data after CLK†	1.3		¥.š		1.3		ns

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO $T_A = 25^{\circ}C$			SN54ABT16821		SN74ABT16821		UNIT	
	( 01)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
f <sub>max</sub>			150			150	4	150		MHz
t <sub>PLH</sub>	CLK	Q	1.3	3.7	5.1	1.3	<i>∰</i> 6.7	1.3	6.1	ns
t <sub>PHL</sub>	CLK		1.6	3.9	5.1	1.6,	5.8	1.6	5.4	
t <sub>PZH</sub>	Œ	a	1.1	3.2	4.7	1,(1)	5.8	1.1	5.7	ns
t <sub>PZL</sub>	OE .	°	1.6	3.8	5	_	5.7	1.6	5.6	115
t <sub>PHZ</sub>	Œ	Q	2	4.5	5.7	Q. 2	6.6	2	6.5	ns
t <sub>PLZ</sub>	02	ŭ .	1.8	4.1	5.8	1.8	8.4	1.8	7.1	ris

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_r \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

SN54ABT16823...WD PACKAGE SN74ABT16823...DL PACKAGE (TOP VIEW)

1			1
ICLR [	<sub>1</sub> U	56	]1CLK
10E	2		1 CLKEN
1Q1 [			1D1
GND [	4	53	GND
1Q2 [	5	52	1D2
1Q3 [	6	51	] 1D3
V <sub>CC</sub> [	7	50	]v <sub>cc</sub>
1Q4 [		49	] 1D4
1Q5 [	9	48	] 1D5
1Q6[	10	47	] 1D6
GND [			] GND
1Q7 [	12		] 1D7
1Q8 🛚		44	] 1D8
1Q9 [		43	] 1D9
2Q1 [	15	42	]2D1
2Q2 [			]2D2
2Q3 [	17	40	] 2D3
GND [		39	]GND
2Q4 [			]2D4
2Q5 [	20	37	]2D5
2Q6 [		36	]2D6
Vcc [	22	35	]v <sub>cc</sub>
2Q7 [		34	2D7
`2Q8 [		33	]2D8
GND [			]GND
2Q9 [			]2D9
20E [		30	2CLKEN
CLR	28	29	12CLK

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16823 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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JUNE 1992-REVISED OCTOBER 1992

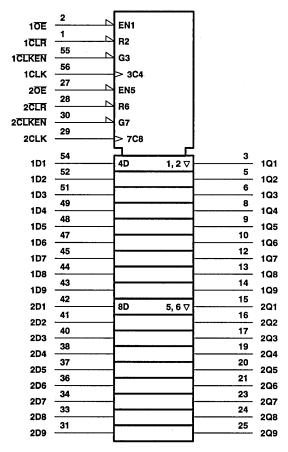
#### description (continued)

The SN54ABT16823 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16823 is characterized for operation from  $-40^{\circ}$ C to 85°C.

FUNCTION TABLE (each 9-bit stage)

			OUTPUT		
ŌE	CLR	CLKEN	CLK	D	Q
L	L	Х	X	Х	L
L	н	L	1	Н	н
L	н	L	1	L	L
L	н	L	L	X	Q <sub>0</sub>
L	Н	Н	X	X	Qo
н	×	X	X	X	z

### logic symbol<sup>†</sup>

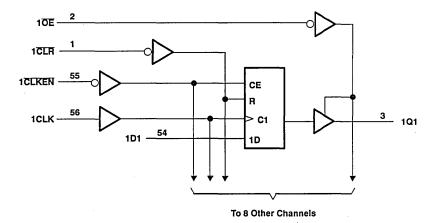


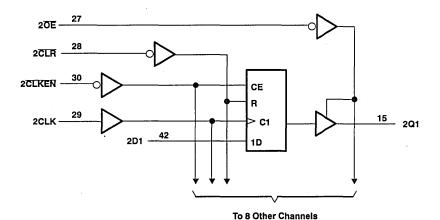
<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



JUNE 1992-REVISED OCTOBER 1992

### logic diagram (positive logic)





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO	0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub> : SN54ABT16823	96 mA
SN74ABT16823	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	−50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



## SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16823	SN74AB	T16823	
			MIN	MIN MAX		MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage				2		V
VIL	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	Vcc	V
Гон	High-level output current			-24	Ì	-32	mA
loL	Low-level output current			48	ĺ	64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TE	ET CONDITIO	Ne	T	A = 25°0	;	SN54AB	T16823	SN74AB	T16823	LINET	
PARAMETER	IE:	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V	
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5			
V <sub>OH</sub>	$V_{CC} = 5 V$ ,	$I_{OH} = -3 \text{ mA}$		3			3		3		<sub>v</sub>	
<b>▼</b> OH	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -24 m	Α	2			2				ľ	
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m}$	Α	2‡					2			
Vai	V <sub>CC</sub> = 4.5 V,					0.55		0.55			V	
VOL VCC	V <sub>CC</sub> = 4.5 V,	l <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>				0.55		
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or C	ND			±1		±1		±1	μА	
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА	
lozL	V <sub>CC</sub> = 5.5 V <sub>i</sub>	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА	
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	5 V			±100				±100	μΑ	
I <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ	
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-200	-50	-200	-50	-200	mA	
	V 55V		Outputs high			0.5		0.5		0.5		
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{L} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			80		80		80	mA	
	VI = VCC 01 GIVD		Outputs disabled	-		0.5		0.5		0.5		
Δlcc <sup>¶</sup>	$V_{CC} = 5.5 \text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND				1.5		1.5		1.5	mA		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			3.5						pF		
C <sub>o</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	'			7.5						pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

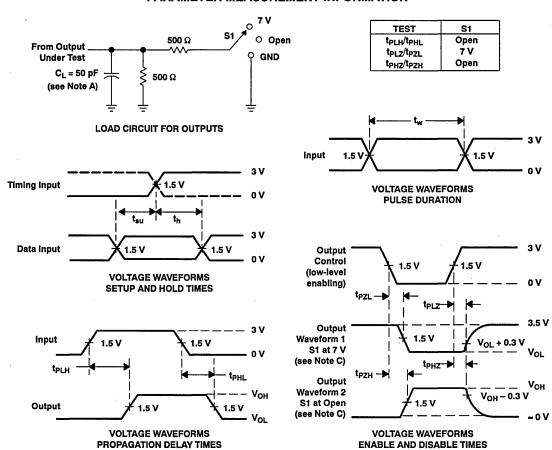
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16823		SN74ABT16823		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	i	
f <sub>clock</sub>	Clock frequency		0	150	0	150	0	150	MHz	
	Dulas duration	CLR low	3.3		3.3		3.3			
t <sub>w</sub>	Pulse duration	CLK high or low	3.3		3.3		3.3		ns	
		CLR inactive	1.6		1.6		1.6			
t <sub>su</sub>	Setup time before CLK†	Data	1.7		1.7		1.7		ns	
		CLKEN low	2.8		2.8		2.8			
	Lield No. 2 office OLIVA	Data	1.2		1.2		1.2			
th	Hold time after CLK†	CLKEN low	0.6		0.6		0.6		ns	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	Г16823	SN74ABT	Г16823	UNIT
	( 0.)	(55.1.5.1,	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
t <sub>PLH</sub>	CLK	Q	1.6	3.9	5.5	1.6	7.7	1.6	6.8	ns
t <sub>PHL</sub>	CLK		2.1	3.9	5.4	2.1	6.4	2.1	6	_ ''5
t <sub>PHL</sub>	CLR	Q	1.9	4.1	5.3	1.9	6.3	1.9	6.1	ns
t <sub>PZH</sub>	OE		1	3.1	4.2	1	5.1	1	4.9	
t <sub>PZL</sub>	OE	Q	1.5	3.5	4.6	1.5	5.7	1.5	5.5	ns
t <sub>PHZ</sub>	OE	Q	2.2	4.3	5.6	2.2	6.3	2.2	6.1	no
t <sub>PLZ</sub>	OE		1.6	4.3	6.4	1.6	10.5	1.6	8.7	ns

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16825 is an 18-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OET or OE2) input is high, all nine affected outputs are in the high-impedance state.

SN54ABT16825...WD PACKAGE SN74ABT16825...DL PACKAGE (TOP VIEW)

10E1	П.	U		Ь	10E2	
1Y1					1A1	•
1Y2					1A2	
					GND	
GND 1Y3					1A3	
			52	K	1A3	
1Y4						
Vcc					Vcc	
1Y5					1A5	
1Y6					1A6	
1Y7					1A7	
GND					GND	
1Y8				_	1A8	
1Y9					1A9	
GND					GND	
GND					GND	
2Y1					2A1	
2Y2					2A2	
GND					GND	
2Y3					2A3	
2Y4					2A4	
2Y5					2A5	
Vcc			35	0	$V_{CC}$	
2Y6					2A6	
2Y7					2A7	
GND					GND	
2Y8			31	0	2A8	
2Y9					2A9	
20E1	28		29	þ	20E2	

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16825 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16825 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16825 is characterized for operation from  $-40^{\circ}$ C to 85°C.

## FUNCTION TABLE (each 9-bit section)

	INPUTS		OUTPUT
OE1	OE2	Α	Υ
L	L	L	L
L	L	Н	Н
н	Х	Х	z
×	н -	X	z

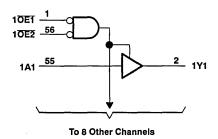
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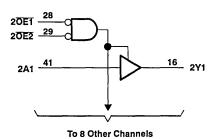
Texas VI Instruments

JUNE 1992-REVISED OCTOBER 1992

#### logic symbol<sup>†</sup> 10E1 EN1 56 10E2 28 & 20E1 29 EN2 20E2 55 2 1 🗸 **1Y1** 1A1 54 3 1A2 1Y2 5 52 1A3 1Y3 6 1Y4 1A4 49 8 1A5 1Y5 48 9 1A6 **1Y6** 10 1A7 **1Y7** 45 12 1A8 1Y8 13 44 1A9 1Y9 16 41 2A1 2 ▽ 2Y1 40 17 2A2 2Y2 38 19 2Y3 2A2 37 20 2A3 2Y4 36 21 2A4 2Y5 34 2Y6 2A5 33 24 2A6 2Y7 31 26 2A7 2Y8 27 2A8 2Y9

### logic diagram (positive logic)





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16825	96 mA
SN74ABT16825	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	-65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

JUNE 1992-REVISED OCTOBER 1992

### recommended operating conditions (see Note 2)

			SN54AB	T16825	SN74AB	T16825	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	٧ .
VI	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
IOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TEST CONDITIONS			T <sub>A</sub> = 25°C			T16825	SN74ABT16825		
PARAMETER	'5	SI CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V}, \qquad l_1 = -18 \text{ mA}$					-1.2		-1.2		-1.2	V
•	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5			
VoH	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
∨он	$V_{CC} = 4.5 \text{ V}, \qquad l_{OH} = -24 \text{ mA}$			2			2				٧
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2		
V	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	v
l <sub>l</sub>	$V_{CC} = 5.5 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ	
lozh	$V_{CC} = 5.5 \text{ V},$	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$				50		50		50	μА
lozL	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ	
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo§	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V		Outputs high		-	2		2		2	
lcc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_0 = 0$ ,	Outputs low			32		32		32	mA
·	V1 = VCC 01 GIVE		Outputs disabled			2		2		2	
Δlcc¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V										рF
Co	V <sub>O</sub> = 2.5 V or 0.5 \	/									pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

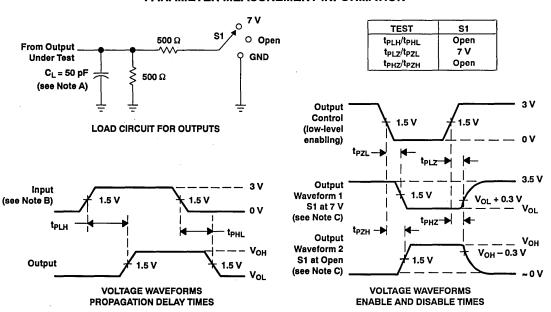
This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V T	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			T16825	SN74AB	UNIT	
	(1.41 01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	V						1	3.3	
t <sub>PHL</sub>		, T						1	4.1	ns
t <sub>PZH</sub>	ŌĒ	Y						1	5.1	— ns
t <sub>PZL</sub>	OE							1.2	5.6	
t <sub>PHZ</sub>	DE .	Y						2	6.3	ns
t <sub>PLZ</sub>	ŌĒ							1.9	6	

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\leq}$  10 MHz,  $Z_0 = 50~\Omega$ ,  $t_f \leq 2.5~ns$ ,  $t_f \leq 2.5~ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Members of the Texas Instruments
  Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16826 is an 18-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OET or OE2) input is high, all nine affected outputs are in the high-impedance state.

SN54ABT16826...WD PACKAGE SN74ABT16826...DL PACKAGE (TOP VIEW)

	_		_	
10ET	1	$\cup_{5}$	<u>Б</u>	10E2
1Y1	2	5	[[5	
1Y2	3	5	4[]	1A2
GND	4	5	з[]	GND
1Y3	5	5	2[]	1A3
	6	5		1A4
Vcc	7		٥Д	
	8	4	9[]	1A5
	9	4	8 <u>[</u> ]	1A6
1Y7	10			1A7
٠	] 11	4	6[]	GND
	12	4	5[]	1A8
	13	4	4[]	1A9
	14	4	3 <b>[</b> ]	GND
	15	4	2[]	GND
	16	4	10	2A1
	17	4	٥Į	2A2
	18	3	9[]	GND
	19	3	8[ <u>]</u>	2A3
2Y4	20	3	7[]	2A4
	21	3	6 []	2A5
	22		5[]	$V_{CC}$
	23	3	4[]	2A6
	24		з[]	2A7
GND	25		2[]	GND
	26		1 []	2A8
0	27	3		2A9
20E1	28	2	эþ	20E2
			_	

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16826 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16826 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16826 is characterized for operation from -40°C to 85°C.

## FUNCTION TABLE (each 9-bit section)

		INPUTS	OUTPUT	
ı	OE1	OE2	Α	Y
	L	L	L	Н
	L	Ľ	Н	Ĺ
	н	Х	X	Z
	_ X	н	Х	Z

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2A4

2A5

2A6

2A7

2A8

34

33

31

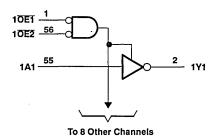
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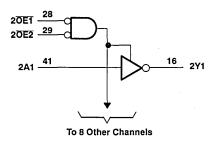
### SN54ABT16826, SN74ABT16826 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

D4512, JUNE 1992-REVISED OCTOBER 1992

#### logic symbol<sup>†</sup> 10E1 EN1 56 10E2 28 20ET & 29 EN2 20E2 55 2 1A1 1 ▽ 1Y1 54 1A2 1Y2 5 52 1Y3 1A3 51 6 1A4 **1Y4** 49 8 1A5 1Y5 48 9 1A6 1Y6 47 10 1A7 **1Y7** 45 12 1A8 1Y8 44 13 1A9 1Y9 41 16 2A1 2 ▽ 2Y1 40 17 2A2 2Y2 38 19 2A2 2Y3 37 20 2A3 2Y4 36 21

### logic diagram (positive logic)





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

2Y5

2Y6

2Y7

2Y8

2Y9

23

24

26

27

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	–0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16826	96 mA
SN74ABT16826	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

JUNE 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16826	SN74AB	T16826	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	Vcc	0	Vcc	٧
Юн	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature			125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	ļ <u>.</u> .	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT16826		SN74ABT16826	
PARAMETER	'5	SI CONDIIIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5			
V	V <sub>CC</sub> = 5 V,						3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -24 \text{ mA}$			2			2				<b>'</b>
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	1 <sub>OL</sub> = 48 mA				0.55		0.55			v
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	. •
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1		±1	μА
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
lozL	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	v 55V		Outputs high			2		2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			32		32		32	mΑ
	1 - 1 CC 01 C14D		Outputs disabled			2		2		2	
Δlcc¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V										pF
C <sub>o</sub>	Vo = 2.5 V or 0.5 \	/									pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

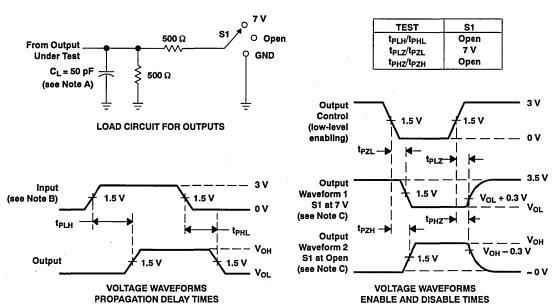
On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>1</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

### SN54ABT16826, SN74ABT16826 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

56 10E2

55 N 1A1

54 T 1A2

53 | GND

52 1A3

51 A14

50 [] V<sub>CC</sub>

49 1 1A5

48 1 1A6

47 🛭 1A7

46 | GND

45 N 1A8

44 🛮 1A9

42 2A1

41 N 2A2

40 🛮 2A3

39 🛮 GND

38 N 2A4

37 T 2A5

36 🛮 2A6

35 🛛 V<sub>CC</sub>

34 🛛 2A7

33 N 2A8

32 | GND

31 🛭 2A9

30 D 2A10

29 1 2<del>0E</del>2

43 ∏ 1A10

SN54ABT16827...WD PACKAGE SN74ABT16827...DL PACKAGE

(TOP VIEW)

10ET []

1Y1 🛮 2

1Y2 []3

GND II4

1Y3 🛮 5

1Y4 ∏6

V<sub>CC</sub> []7

1Y5 ∏8

1Y6 🛮 9

1Y7 [] 10

GND [] 11

1Y8  $\Pi_{12}$ 

1Y9 [13

1Y10 II 14

2Y1 15

2Y2 II 16

2Y3 [] 17

GND II 18

2Y4 [] 19

2Y5  $\Pi$ 20

2Y6 []21

V<sub>CC</sub> [] 22

2Y7 [] 23

2Y8 II 24

GND 1125

2Y9 [] 26

2Y10 127

20E1 | 28

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- **Members of the Texas Instruments** Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per **JEDEC Standard JESD-17**
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA IOH, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16827 is a noninverting 20-bit buffer composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance

To ensure the high-impedance state during power up or power down, OE should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16827 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin

The SN54ABT16827 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125 $^{\circ}$ C. The SN74ABT16827 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE** (each 10-bit section)

count and functionality of standard small-outline packages in the same printed-circuit-board area.

	INPUTS	OUTPUT							
OE1	OE2	Α	] Y						
L,	L	L	L						
L	L	Н	н						
н	X	Х	z						
×	Н	X	z						

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INSTRUMENTS

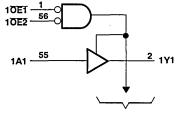
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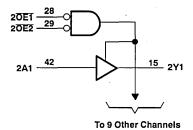
#### logic symbol†

#### 10E1 1 EN<sub>1</sub> 56 10E2 28 & 20E1 EN<sub>2</sub> 29 20E2 55 1 ▽ **1Y1** 1A1 54 3 1A2 1Y2 52 5 1Y3 1A3 51 6 1Y4 1A4 49 8 1A5 1Y5 48 9 1A6 1Y6 47 10 **1Y7** 1A7 45 12 1A8 1Y8 44 13 1Y9 1A9 43 14 1A10 1Y10 42 15 2A1 2∇ 2Y1 41 16 2A2 2Y2 40 17 2Y3 2A3 38 19 2A4 2Y4 37 20 2A5 2Y5 36 21 2A6 2Y6 34 23 2A7 2Y7 33 24 2A8 2Y8 31 26 2A9 2Y9 30 27 2A10 2Y10

### logic diagram (positive logic)



To 9 Other Channels



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub> : SN54ABT16827	96 mA
SN74ABT16827	128 mA
Input clamp current, $I_{ K }(V_{ I } < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

JUNE 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16827	SN74ABT16827		UNIT
	•		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT16827		SN74ABT16827		UNIT
PARAMETER	'E	SI CONDITIC	ons -	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V	
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA	4	2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 m/	4	3			3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -24 \text{ mA}$			2			2				°
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$								2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 64 \text{ mA}$					0.55 <sup>‡</sup>				0.55	L V
tı	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1		±1	μА
lozh	$V_{CC} = 5.5 \text{ V},$	5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
lozL	V <sub>CC</sub> = 5.5 V,	<sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μA
lo <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	v 55V		Outputs high			2		2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	l <sub>O</sub> = 0,	Outputs low			32		32		32	mΑ
	1 1 - 100 01 0110		Outputs disabled			2		2		2	
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V										pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	<del>/</del>									pF

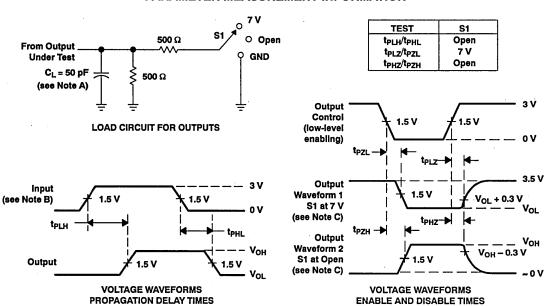
<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OI</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16828 is an inverting 20-bit buffer composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10ET and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT16828...WD PACKAGE SN74ABT16828...DL PACKAGE (TOP VIEW)

	$\overline{}$		_		
10ET	d 1	Ų,	56	Ь	10E2
1Y1	2		55	6	1A1
1Y2			54	6	1A2
GND			53	b	GND
1Y3	[5		52	þ	1A3
1Y4	<b>[</b> ]6		51	1	A14
Vcc	[]7		50	1	$V_{CC}$
1Y5	[]8		49		1A5
1Y6 1Y7	<b>[</b> ]9				1A6
					1A7
GND					GND
1Y8					1A8
1Y9	13				1A9
1Y10					1A10
	15	-			2A1
2Y2					2A2
2Y3					2A3
GND					GND
	19	;		_	2A4
2Y5	20				2A5
2Y6	-	;			2A6
Vcc					$V_{CC}$
	23			_	2A7
2Y8	_				2A8
GND			32	0	GND
2Y9	_				2A9
	27				2A10
20E1	28	2	29	Ц	2 <u>0E2</u>

The SN74ABT16828 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16828 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16828 is characterized for operation from  $-40^{\circ}$ C to 85°C.

## FUNCTION TABLE (each 10-bit section)

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	· H
L	L	н	L
н	X	X	z
×	Н	X	z

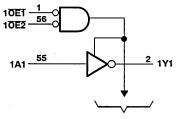
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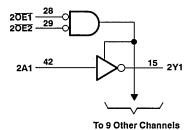
OCTOBER 1992

#### logic symbol<sup>†</sup> 10ET EN1 56 10E2 28 & 20E1 EN2 29 20E2 55 17 1A1 **1Y1** 54 3 1Y2 52 5 1A3 **1Y3** 51 6 1A4 1Y4 49 8 1A5 **1Y5** 48 9 1A6 **1Y6** 47 10 1A7 **1Y7** 45 12 1Y8 1A8 13 1A9 1**Y**9 14 43 1Y10 1A10 42 15 2A1 1 2∇ 2Y1 41 16 2A2 2Y2 40 17 2A3 2Y3 38 19 2A4 2Y4 37 20 2A5 2Y5 36 21 2A6 2Y6 34 23 2A7 2Y7 33 24 2A8 2Y8 31 26 2A9 2Y9 30 27 2A10 2Y10

### logic diagram (positive logic)



To 9 Other Channels



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	
Current into any output in the low state, Io: SN54ABT16828	96 mA
SN74ABT16828	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



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### recommended operating conditions (see Note 2)

			SN54AB	SN54ABT16828		SN74ABT16828	
			MIN	MAX	MIN	0.8 V <sub>CC</sub> -32	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	<u> </u>	2		2		
VIL	Low-level input voltage			0.8		0.8	
Vı	Input voltage		0	Vcc	0	Vcc	
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54ABT16828		SN74ABT16828		UNIT	
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	$l_1 = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
V <sub>ОН</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3			3		3		٧
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				
	V <sub>CC</sub> = 4.5 V,	= 4.5 V, I <sub>OH</sub> = - 32 mA							2		
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA					0.55		0.55			٧
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55 <sup>‡</sup>			0.	0.55	
l <sub>1</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = V <sub>CC</sub> or 0	GND			±1		±1		±1	μΑ
lozh	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	$V_{CC} = 0 \text{ V}$ , $V_1 \text{ or } V_0 \le 4.5 \text{ V}$				±100				±100	μА	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V		Outputs high			2		2		2	
Icc	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		32		32	mA					
	VI = VCC OI GIND		Outputs disabled			2		2		2	
Δlcc¶	Aloo! I TT				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V										pF
С。	V <sub>O</sub> = 2.5 V or 0.5 V										pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

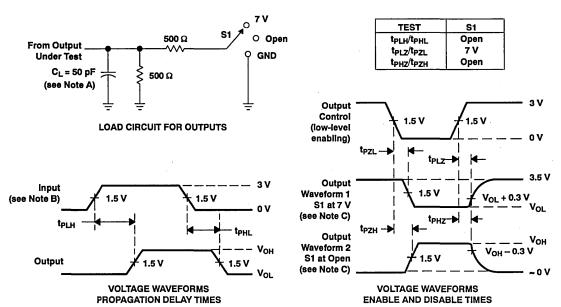
<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT16828, SN74ABT16828 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>1</sub> ≤ 2.5 ns, t<sub>2</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Parity Error Flag With Parity Generator/Checker
- Register for Storage of the Parity Error Flag
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16833 consists of two noninverting 8-bit to 9-bit parity bus transceivers and is designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

SN54ABT16833...WD PACKAGE SN74ABT16833...DL PACKAGE (TOP VIEW)

1OEB	1	U	56	10EA
1CLK[			55	1CLR
1ERR [				1PARITY
GND [				GND
1A1 [	5			1B1
1A2 [	6			1B2
Vcc [	7			[]∨ <sub>cc</sub>
1A3 [				] 1B3
1A4 [	9		48	] 1B4
1A5 [	10	,	47	] 1B5
GND [	11		46	] GND
1A6 [	12		45	] 1B6
1A7 [	13			1B7
1A8 [	14		43	] 1B8
2A1 [	15		42	] 2B1
2A2 [	16			] 2B2
2A3 [	17		40	] 2B3
GND [			39	] GND
2A4 [				] 2B4
2A5 [			37	] 2B5
2A6 [				] 2B6
Vcc [	22			] V <sub>CC</sub>
2A7 [	23			] 2B7
2A8 [				] 2B8
GND [				] GND
				2PARITY
				2CLR
OEB [	28		29	] 20EA

The error (1ERR or 2ERR) output is configured as an open-collector output. The B-to-A parity error flag is clocked into 1ERR (or 2ERR) on the low-to-high transition of the clock (1CLK or 2CLK) input. 1ERR (or 2ERR) is cleared (set high) by taking the clear (1CLR or 2CLR) input low.

The output-enable (OEA and OEB) inputs can be used to disable the device so that the buses are effectively isolated. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16833 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16833 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16833 is characterized for operation from -40°C to 85°C.

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#### **FUNCTION TABLE**

			INPUTS			1	OUTPUT AND I/O			
OEB	ÖEA	CLR	·CLK	Al Σ OF H's	Bi <sup>†</sup> Σ OF H's	Α	В	PARITY	ERR‡	FUNCTION
L	Н	х	x	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
Н	L	Н	t	NA	Odd Even	В	NA	NA	H	B data to A bus and check parity
Х	X	L	Х	X	X	×	NA	NA	Н	Check error flag register
н	н	Н Н Н	No† No† †	X X Odd Even	x	z	z	Z	NC H H L	Isolation <sup>§</sup>
L	L	×	х	Odd Even	NA	NA	Α	H L	NA	A data to B bus and generate inverted parity

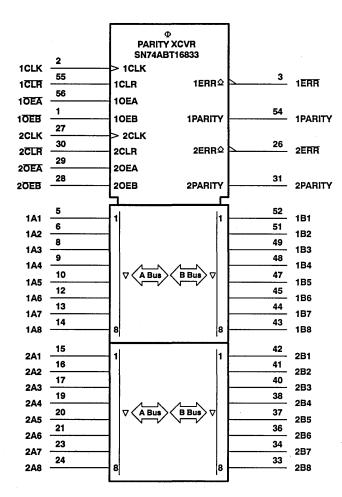
NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

Output states shown assume the ERR output was previously high.
 In this mode, the ERR output (when clocked) shows inverted parity of the A bus.

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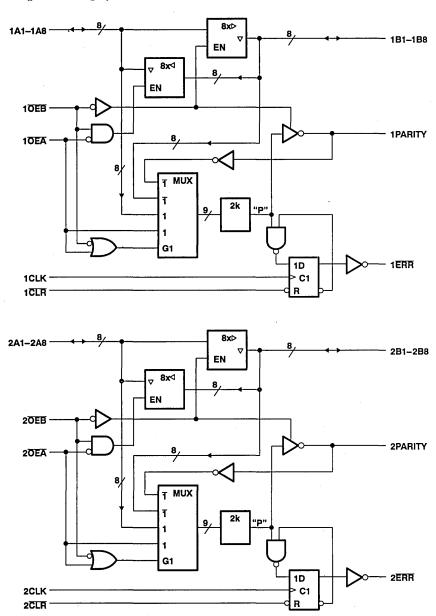
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



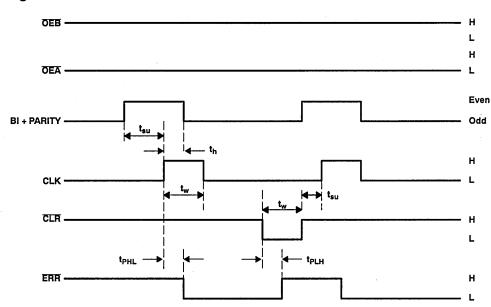
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#### **ERROR FLAG FUNCTION TABLE**

INP	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT "P"	ERR <sub>n-1</sub> †	ENN	
Н	Ť	Н	н	Н	
н	1	X	L	L	Sample
Н	1	L	X	L	•
L	X	X	X	Н	Clear

<sup>†</sup> The state of the ERR output before any changes at CLR, CLK, or point "P".

#### error-flag waveforms



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	$\dots$ $-0.5$ V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	. $-0.5 \text{ V}$ to $5.5 \text{ V}$
Current into any output in the low state, Io: SN54ABT16833	96 mA
SN74ABT16833	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	-65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SCBS097A-D3982, FEBRUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16833	SN74AB	T16833	
			MIN	MAX	MIN MAX		UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2	ű.	2		٧
$V_{IL}$	Low-level input voltage			0.8		0.8	٧
V <sub>I</sub>	Input voltage		0	ુ€ V <sub>CC</sub>	0	Vcc	V
V <sub>OH</sub>	High-level output voltage	ERR		5.5		5.5	٧
I <sub>OH</sub>	High-level output current		35	-24		-32	mA
loL	Low-level output current	Except ERR	Q	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		CT CONDITIO	NO	Т	A = 25°	С	SN54AB	T16833	SN74AB	T16833	UNIT
PARAMETER	16	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5	3		2.5				
V	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$	All outputs	3	3.4		3		3		l v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> =	-24 mA	except ERR				2				*
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> =	-32 mA	1	2‡	2.7				2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA			0.25	0.55		0.55			V
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA			0.3	0.55‡		_		0.55	ľ
Гон	V <sub>CC</sub> = 4.5 V,	V <sub>OH</sub> = 5.5 V	ERR			20		.20		20	μΑ
1.	V <sub>CC</sub> = 5.5 V,	CC = 5.5 V, Control inputs				±1		(/±1		±1	μА
l <sub>1</sub>	$V_I = V_{CC}$ or GND A or B ports					±100		€£100		±100	μ
I <sub>IL</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> = GND	A or B ports			-50	,<	₹ –50		-50	μΑ
lozн <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.7 V				50	ري.	50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 0.5 V$				-50	ನೆ	-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100	, Q			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	~	50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		1.5	2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low		28	36		36		36	mΑ
	V <sub>I</sub> = V <sub>CC</sub> or GND Outputs disabled			1	2		2		2		
41 #	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,									
Δl <sub>CC</sub> #	Other inputs at V <sub>CC</sub> or GND					50	1	50		50	μΑ
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs				3						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5	V	A or B ports		9						рF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>S$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS097A-D3982, FEBRUARY 1991-REVISED OCTOBER 1992

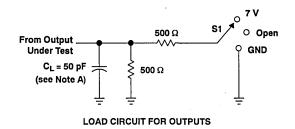
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	SN54ABT16833	SN74ABT16833	UNIT
İ			MIN MAX	MIN & MAX	MIN MAX	
t <sub>w</sub>	Pulse duration	CLK high or low	3	\$ 40	3	ns
	Saturations before CLVA	A port	4.5	£5.07	4.5	
t <sub>su</sub>	Setup time before CLK†	CLR	1	4.60	1	ns
th	Hold time after CLK↑	A port	0	0	0	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

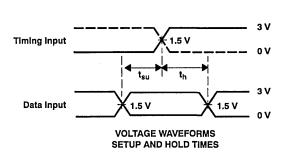
PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54ABT	16833	SN74AB	T16833	UNIT
	(1147-01)	(33.1.5.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	Ì
t <sub>PLH</sub>	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
tpHL	1 ^0'6	BUIA	2	3.1	3.9	2	4.5	2	4.3	115
t <sub>PZH</sub>	OE .	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t <sub>PZL</sub>	]	7018	2.5	4.3	5.1	2.5	6.2	2.5	6	1 115
tPHZ	ŌĒ	A or B	2	3.6	4.5	2	<b>.</b> ∜5.5	2	5.4	ns
t <sub>PLZ</sub>	]	AOIB	1.5	3	3.8	1.5	<b>4.7</b>	1.5	4.3	l ns
t <sub>PLH</sub>	A or OE	PARITY	2	4.6	5.4	2, ₹	~ 7	2	6.7	
t <sub>PHL</sub>	7 70105	FADILI	2	4.3	5.1	့လွ	6.5	2	.6.1	ns
t <sub>PZH</sub>	OE .	PARITY	2	3.6	5	<b>Q</b> 2	5.8	2	5.7	ns
t <sub>PZL</sub>	]	FADILI .	2.5	4.4	5.8	<b>Æ</b> 2.5	6.7	2.5	6.5	115
t <sub>PHZ</sub>	ΟE	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
t <sub>PLZ</sub>	OE .	FAMILI	1.5	2.9	3.7	1.5	4.2	1.5	4.1	115
t <sub>PLH</sub>	CLK, CLR	ERR	2	3.4	4.2	2	4.8	2	4.6	
t <sub>PHL</sub>	CLK		2	2.8	3.6	2	4.1	2	3.9	ns

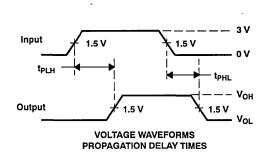
#### PARAMETER MEASUREMENT INFORMATION

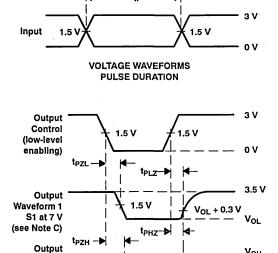


TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	7 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	Open

ERR	S1
t <sub>PHL</sub> (see Note E)	Open
t <sub>PLH</sub> (see Note F)	7 V







**VOLTAGE WAVEFORMS** 

**ENABLE AND DISABLE TIMES** 

 $v_{\text{oh}}$ 

V<sub>OH</sub> - 0.3 V

NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.

Waveform 2

S1 at Open

(see Note C)

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t<sub>PHL</sub> is measured at 1.5 V.
- F. t<sub>PLH</sub> is measured at V<sub>OL</sub> + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms



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	<ul> <li>Members of the Texas Instruments</li> <li>Widebus™ Family</li> </ul>	SN54ABT16841 WD PAC SN74ABT16841 DL PACI (TOP VIEW)	
A .	<ul> <li>State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation</li> </ul>	10E (1 56) 1LE	
ı	<ul> <li>ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF,</li> </ul>	1Q1	 
	R = 0)  Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17	1Q3	<b>;</b>
	<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> <li>&lt; 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C</li> </ul>	1Q5 [] 8 49 [] 1D5 1Q6 [] 9 48 [] 1D6	6
	<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise</li> </ul>	1Q7   10 47   1D7 GND   11 46   GNI 1Q8   12 45   1D8	D
	<ul> <li>Flow-Through Architecture Optimizes PCB Layout</li> </ul>	1Q9	)
	<ul> <li>High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)</li> </ul>	2Q1	<u>!</u>
	Packaged in Plastic 300-mil Shrink     Small-Outline Packages (DL) and 380-mil     Time Pitch Council Field Packages (MP)	2Q3 [ 17 40 ] 2D3 GND [ 18 39 ] GNI	D
	Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings	2Q4   19 38   2D4 2Q5   20 37   2D5 2Q6   21 36   2D6	;
de	scription	V <sub>CC</sub> 22 35 V <sub>CC</sub> 2Q7 23 34 2D7	;
	These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers 1/0 parts bidirectional bus drivers and	2Q7   23   34   2D7 2Q8   24   33   2D8 GND   25   32   GNI 2Q9   26   31   2D9 2Q10   27   30   2D1	) )
	registers, I/O ports, bidirectional bus drivers, and working registers.	20E 28 29 2LE	

The 'ABT16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable (10E or 20E) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16841 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16841 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16841 is characterized for operation from -40°C to 85°C.

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# SN54ABT16841, SN74ABT16841 20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS SEPTEMBER 1992-REVISED OCTOBER 1992

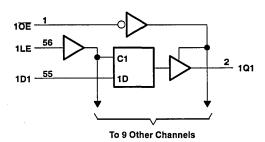
#### **FUNCTION TABLE** (each 10-bit latch)

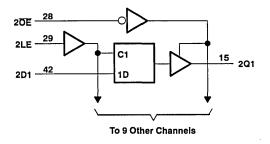
	INPUTS	OUTPUT	
ŌE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q <sub>0</sub>
Н	Х	Х	z

# logic symbol†

#### 10E EN2 56 1LE C1 28 EN4 20E 29 2LE СЗ 55 2 1D1 1D **1Q1** 2 ▽ 54 3 1D2 1Q2 5 1D3 1Q3 51 6 1D4 1Q4 49 8 1D5 **1Q5** 48 9 1D6 1Q6 47 10 1D7 1Q7 45 12 1D8 1Q8 44 13 1D9 1Q9 14 1D10 1Q10 42 15 2D1 3D 4 ▽ 2Q1 41 16 2D2 2Q2 40 17 2D3 2Q3 38 19 2D4 2Q4 37 20 2D5 2Q5 36 21 2D6 2Q6 34 23 2Q7 2D7 33 24 2D8 2Q8 31 26 2D9 2Q9 30 27 2D10 2Q10

# logic diagram (positive logic)





<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating	g free-air temperature range (unless otherwise noted).
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the h	nigh state or power-off state, V <sub>O</sub> 0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT16841 96 mA
	SN74ABT16841 128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16841	SN74AB	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage	· ·	0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ပ္

NOTE 2: Unused or floating inputs must be held high or low.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54AB	T16841	SN74ABT16841		UNIT
PARAMETER	TEST CONDITIONS				TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
VoH	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		] <sub>v</sub>
∨он	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -24 \text{ m}.$	Α	2			2			-	ľ
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	A	2‡					2		1
V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			V	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	<sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55 <sup>‡</sup>				0.55	·
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = V_{CC} \text{ or GND}$				±1		±1		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$				50		50		50	μΑ
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	50	-180	mA
			Outputs high			2		2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			85		85		85	mA
	AI = ACC OLGIAD		Outputs disabled			2		2		2	1
Δl <sub>CC</sub> <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V										pF
Со	V <sub>O</sub> = 2.5 V or 0.5 \	/									pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

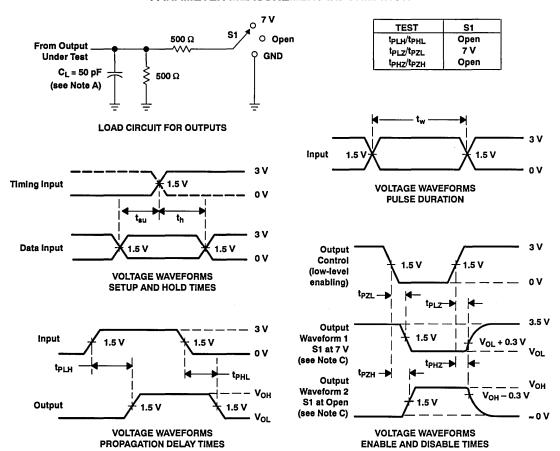
On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $<sup>\</sup>P$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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•	<b>Members of the Texas Instruments</b>
	Widebus™ Family

- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Lavout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16843 18-bit latch is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

THE 'ABT16843 can be used as two 9-bit latches or one 18-bit latch. The eighteen latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

SN54ABT16843...WD PACKAGE SN74ABT16843...DL PACKAGE (TOP VIEW)

	$\overline{}$		l .
1CER (	11 `	ے 56	1LE
10E	2	55	
1Q1 [	3	54	
GND (	4	53	GND
1Q2 [	5	52	] 1D2
1Q3 [	6	51	] 1D3
v <sub>cc</sub> [	7	50	] v <sub>cc</sub>
1Q4 (	8	49	1D4
1Q5 [	9	48	1D5
1Q6 [	10	47	
GND	] 11	46	
1Q7 [	12	45	1D7
1Q8 [	3	44	
1Q9 [	14	43	
2Q1 [	1	42	2D1
2Q2 [		41	2D2
2Q3 [	3	40	
GND [	1	39	
2Q4		38	
2Q5 [	3	37	
2Q6 [	21	36	
V <sub>CC</sub>	22	35	] v <sub>cc</sub>
2Q7 [	1	34	2D7
2Q8 [	1 ~ '	33	
GND L	25		GND
2Q9 [	1 - °	31	2D9
20E	27	30	_
2 <del>CLR</del> l	28	29	J 2LE

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16843 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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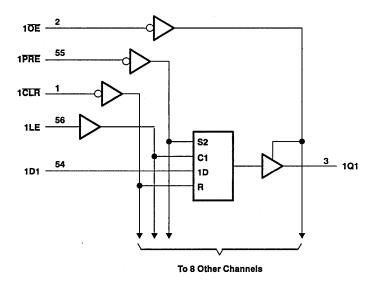
#### description (continued)

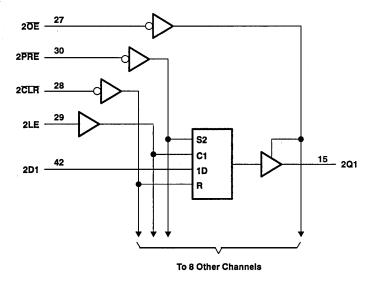
The SN54ABT16843 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16843 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE** (each 9-bit latch)

(ozon o zni izion)										
	INPUTS									
PRE	PRE CLR OE LE D									
L	Х	L	Х	X	н					
н	L	L	X	X	L					
Н	Н	L	Н	L	L					
н	Н	L	н	Н	Н					
н	Н	L	L	X	Q <sub>0</sub>					
×	X	H	×	X	z_					

# logic diagram (positive logic)





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub>	
Current into any output in the low state, Io: SN54ABT16843	96 mA
SN74ABT16843	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}(V_O < 0)$	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T16843	SN74AB	T16843	UNIT
			MIN	MAX	MIN	MAX	ONII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	٧
Vi	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54AB	T16843	SN74ABT16843		UNIT
PARAMETER	TEST CONDITIONS				TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = –18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = 3 mA	\ .	3			3		3		] ,
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> =24 m.	A	2			2				ľ
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	A	2‡					2		l
V	V <sub>CC</sub> = 4.5 V,	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA				0.55‡				0.55	ľ	
l <sub>i</sub>	V <sub>CC</sub> = 5.5 V,	$V_{CC} = 5.5 \text{ V}, \qquad V_I = V_{CC} \text{ or GND}$				±1		±1		±1	μА
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$ .	5 V			±100		•		±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
l <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50·	-100	-180	-50	-180	-50	-180	mA
			Outputs high			2		2		2	
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low			85		85		85	mA
	VI = VCC or GIAD		Outputs disabled			2		2		2	
ΔI <sub>CC</sub> <sup>T</sup>	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	V <sub>I</sub> = 2.5 V or 0.5 V									pF
C <sub>o</sub>	Vo = 2.5 V or 0.5 \	/									рF

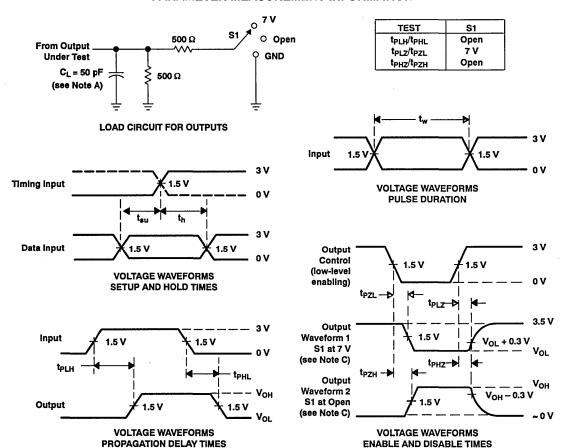
<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_f \leq 2.5 \ ns$ ,  $t_f \leq 2.5 \ ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Parity Error Flag With Parity Generator/Checker
- Latch for Storage of the Parity Error Flag
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16853 dual 8-bit to 9-bit parity transceiver is designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (ERR) output indicates whether or not an error in the B data has occurred. The output-enable (OEA and OEB) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT16853 provides true data at its outputs.

SN54ABT16853...WD PACKAGE SN74ABT16853...DL PACKAGE (TOP VIEW)

1OEB	1	O	56	10EA
1CE [	2		55	1CLR
1ERR 🛚				] 1PARITY
GND [				GND
1A1 [	5		52	] 1B1
1A2 [	6		51	] 1B2
Vcc [			50	] V <sub>CC</sub>
1A3 [	8			] 1B3
1A4 [				] 1B4
1A5 [	10			] 1B5
GND [			46	] GND
1A6 [			45	] 1B6
1A7 [				] 1B7
1A8 [				] 1B8
2A1 [				] 2B1
2A2 [	16			] 2B2
2A3 [				] 2B3
GND [				] GND
2A4 [				] 2B4
2A5 [				] 2B5
2A6 [				] 2B6
Vcc [				] V <sub>CC</sub>
2A7 []				] 2B7
2A8 []				] 2B8
GND [				] GND
ZERR [				2PARITY
	27		30	2CLR
SOEB [	28		29	20EA

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the ERR flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable (LE) and clear (CLR) control inputs. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16853 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16853 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16853 is characterized for operation from –40°C to 85°C.

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#### **FUNCTION TABLE**

			INPUTS	3			OUTP	UT AND I/O		
OEB	OEA	CLR	LE	Al Σ OF H's	Bi <sup>†</sup> Σ OF H's	A	В	PARITY	ERR‡	FUNCTION
L	Н	х	х	Odd Even	NA	NA	Α	L H	NA	A data to B bus and generate parity
Н	L	х	L	NA	Odd Even	В	NA	NA	H L	B data to A bus and check parity
Н	L	Н	Н	NA	X	X	NA	NA	NC	Store error flag
X	×	L	Н	X	×	X	NA	NA	Н	Clear error flag register
н	н	H L X	H H L	X X L Odd H Even	х	z	z	z	NC H H L	Isolation <sup>§</sup> (parity check)
L	L	×	X	Odd Even	NA	NA	Α	H L	NA NA	A data to B bus and generate inverted parity

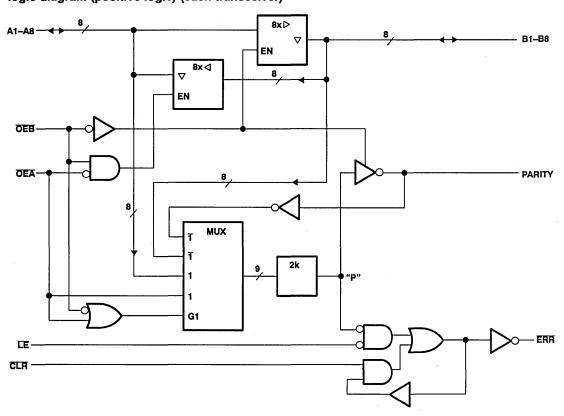
NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume the ERR output was previously high.

§ In this mode, the ERR output (when clocked) shows inverted parity of the A bus.

# logic diagram (positive logic) (each transceiver)

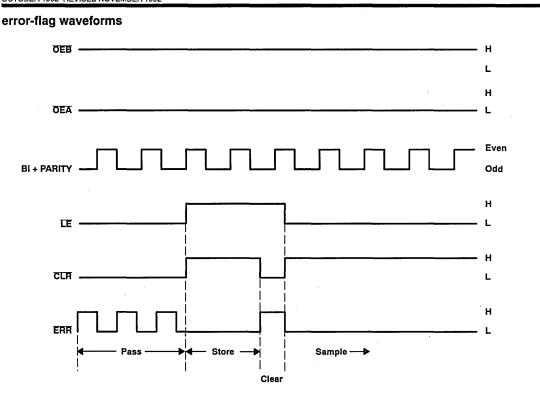


#### **ERROR FLAG FUNCTION TABLE**

Elifori Exa Tottoriot IASEE										
INPL	JTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION					
CLR	LE	POINT "P"	ERR <sub>n-1</sub> †	Enn						
L	L	L H	x	L H	Pass					
		L X	Х	L						
н	L		L	L	Sample					
		н	н	н						
L	Н	Х	Х	Н	Clear					
н	н	×	Н	L H	Store					

<sup>†</sup> The state of the ERR output before any changes at CLR, LE, or point "P".

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	−0.5 V to 7 V
Input voltage range, V <sub>1</sub> (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO	. −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16853	96 mA
SN74ABT16853	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	-65°C to 150°C

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



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#### recommended operating conditions (see Note 2)

			SN54AB1	Г16853	SN74AB	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5,5	4.5	5.5	V
VIH	High-level input voltage		2	Ú,	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0 ,	<sup>6</sup> ₹Vcc	0	Vcc	V
V <sub>OH</sub>	High-level output voltage	ERR	ć	5.5		5.5	V
ЮН	High-level output current		Ş	-24		-32	mA
loL	Low-level output current	Except ERR	,O	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q*	10		10	ns/V
TA	Operating free-air temperature		-55	125	<del>-4</del> 0	85	°Ç

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T	A = 25°	С	SN54ABT	16853	SN74ABT16853		UNIT
PARAMETER	15	SI CONDITIO	NO.	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$		2.5	3		2.5				
V <sub>OH</sub>	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA	All outputs	3	3.4		3		3		v
VOH .	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> =	-24 mA	except ERR				2				\ \ \
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> =	-32 mA		2‡	2.7				2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,				0.25	0.55		0.55			v
VOL.	V <sub>CC</sub> = 4.5 V,				0.3	0.55‡				0.55	•
Іон	V <sub>CC</sub> = 4.5 V,	V <sub>OH</sub> = 5.5 V	ERR			20		20		20	μΑ
h	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$		Control inputs			±1		,≪£1		±1	μА
			A or B ports			±100		<i>⊈</i> 100		±100	μΛ
IιL	V <sub>CC</sub> = 0 V,	V <sub>I</sub> = GND	A or B ports			50		ર્યે −50		-50	μА
lozh <sup>§</sup>	$V_{CC} = 5.5 \text{ V}, \qquad V_0 = 2.7 \text{ V}$					50	Ç,	50		50	μΑ
l <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V},$	$V_0 = 0.5 V$				-50	Ş	-50		-50	μA
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100	Color			±100	μΑ
I <sub>CEX</sub>		V <sub>O</sub> = 5.5 V	Outputs high			50	*	50		50	μА
10 <sup>¶</sup>	$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		1.5	2		2		2	
Icc	$l_0 = 0$ ,	A or B ports	Outputs low		32	40		40		40	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		1	2		2		2	
Alas#	ΔI <sub>CC</sub> ** V <sub>CC</sub> = 5.5 V, One input at 3.4 Other inputs at V <sub>CC</sub> or GND		.4 V,					50		<b>50</b>	
AICC"				50		50		50		μΑ	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs				3						рF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	/	A or B ports		9						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

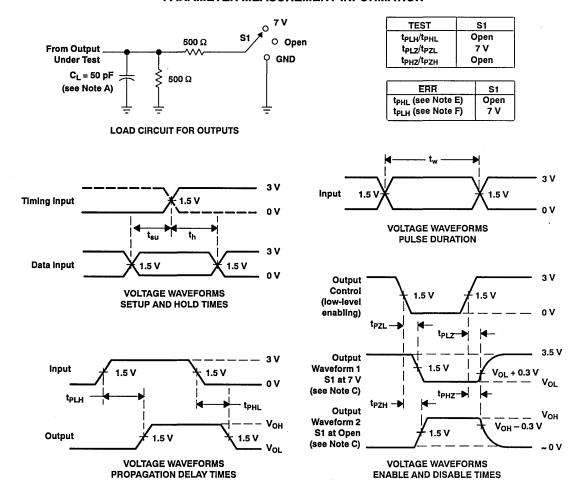
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54AB1	16853	SN74ABT16853		UNIT	
			MIN	MAX	MIN MAX		MIN	MAX		
	Dulas duration	LE high or low	8.5		8.5		8.5		ns	
lw	t <sub>w</sub> Pulse duration	CLR low	4		4.6	7.	4			
	Cotus time	. A, B, and PARITY before LE			187 🕸		10		20	
t <sub>su</sub> Setup time		CLR before LE↓	0		200	69 W			ns	
t <sub>h</sub> Hold time		A, B, and PARITY after LE	0		€ 6€		0		ns	
		CLR after LE	0		0		0		118	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	T16853	SN74AB	Г16853	UNIT
	( 5.)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t <sub>PHL</sub>	7018	6	2	3.1	3.9	2	4.5	2	4.3	113
t <sub>PLH</sub>	A or OE	PARITY	2	4.6	5.9	2	7.3	2	7.1	ns
t <sub>PHL</sub>	A OI OE	PARILI	2	4.8	6.2	2	7.6	2	7.2	115
t <sub>PLH</sub>	CLR	ERR	2	3.7	5.1	2	.5,9	2	5.7	ns
t <sub>PZH</sub>	OE .	A or B	2	3.9	4.9	2	₹5.8	2	5.6	ns
t <sub>PZL</sub>			2.5	4.3	5.1	2.5	<b>≪</b> 6.2	2.5	6	113
t <sub>PHZ</sub>	ŌĒ	A or B	2	3.6	4.5	2,	5.5	2	5.4	ns
t <sub>PLZ</sub>		A or B	1.5	3	3.8	1,57	4.7	1.5	4.3	115
t <sub>PZH</sub>	Œ	PARITY	2	3.6	5	<u>Ş</u> 2	5.8	2	5.7	ns
t <sub>PZL</sub>		PARILI	2.5	4.4	5.8	<b>₹</b> 2.5	6.7	2.5	6.5	115
t <sub>PHZ</sub>	OE .	PARITY	1.5	3.2	4	<b>` 1.5</b>	4.8	1.5	4.7	ns
t <sub>PLZ</sub>	ا ا	FARILL	1.5	2.9	3.7	1.5	4.2	1.5	4.1	113
t <sub>PLH</sub>	Œ	ERR	2	3.5	4.2	2	5	2	4.8	ns
t <sub>PHL</sub>		ENN	2	3.4	4.4	2	5.2	2	4.9	115
t <sub>PLH</sub>	A D DADITY	ERR	2	4.5	6.3	2	7.5	2	7.2	20
t <sub>PHL</sub>	A, B, or PARITY	EAR	2	4.8	6.3	2	7.7	2	7.4	ns

OCTOBER 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpHL is measured at 1.5 V.
- F.  $t_{PLH}$  is measured at  $V_{OL}$  + 0.3 V.

Figure 1. Load Circuit and Voltage Waveforms



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# SN54ABT16862, SN74ABT16862 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1992

•	Members of the Texas Instruments
	Widebus ™ Family

- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT18862 is a 20-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

The 'ABT16862 can be used as two 10-bit transceivers or one 20-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

SN54ABT16862...WD PACKAGE SN74ABT16862...DL PACKAGE (TOP VIEW)

		ı,		
10EAB	1	0	56	] 10EBA
1B1 [	2		55	] 1A1
1B2 [	3			] 1A2
GND [			53	GND
1B3 [				] 1A3
1B4 [				] 1A4
V <sub>CC</sub>				] v <sub>cc</sub>
1B5 [			49	] 1A5
1B6 [				] 1A6
1B7 [				] 1A7
GND [	11		46	] GND
1B8 [				] 1A8
1B9 [	13			] 1A9
1B10 [				] 1A10
2B1 [	15			] 2A1
2B2 [	16			] 2A2
2B3 [	17			] 2A3
GND [	18			] GND
2B4 [	19			] 2A4
2B5 [	20		37	] 2A5
2B6 [	21		36	] 2A6
V <sub>CC</sub> [	22		35	] v <sub>cc</sub>
2B7 [	23		34	] 2A7
2B8 [	24		33	] 2A8
GND [	25		32	] GND ·
2B9 [			31	2A9
2B10 [	27		30	2A10
20EAB [	28		29	20EBA
,				1

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16862 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16862 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16862 is characterized for operation from  $-40^{\circ}$ C to 85°C.

# FUNCTION TABLE (each 10-bit section)

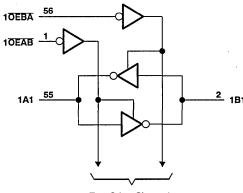
INP	UTS	OPERATION
OEAB	OEBA	OPERATION
L	Н	Ā data to B bus
н	L	B data to A bus
н	Н	Isolation
L	L	Latch A and B $(A = \overline{B})$

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

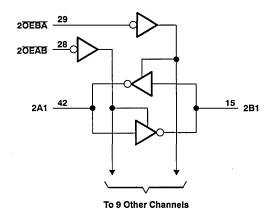


### SN54ABT16862, SN74ABT16862 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS OCTOBER 1992

#### logic diagram (positive logic)



To 9 Other Channels



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16862	96 mA
SN74ABT16862	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	−50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# SN54ABT16862, SN74ABT16862 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16862	SN74AB	UNIT	
			MIN	MAX	MIN	MAX	וואט
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature	<u> </u>	-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT16862		SN74ABT16862		UNIT
PARAMETER	15	SI CONDINO	NO	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>i</sub> = -18 mA	i <sub>i</sub> = -18 mA			-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
VoH	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA	OH = -3 mA				3		3		l v
VOH	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m.	A	2			2				1
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = 32 m.	A	2‡					2		
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55		0.55			v	
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
L.	V <sub>CC</sub> = 5.5 V,		Control inputs ±1 ±1					±1			
l <sub>i</sub>	$V_i = V_{CC}$ or GND		A or B ports			±100		±100		±100	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_I$ or $V_O \le 4.5$	5 V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
lcc	$I_0 = 0$ ,	A or B ports	Outputs low			32		32		32	mA
	$V_1 = V_{CC}$ or GND		Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data inputs	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	Control inputs									pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,	A or B ports								pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 5 V.



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>^{\</sup>S}$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

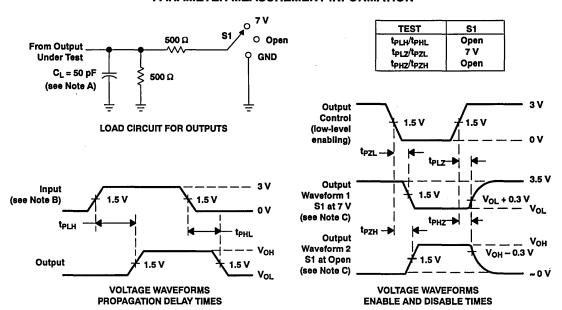
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT16862, SN74ABT16862 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns.}$   $t_r \leq 2.5 \text{ ns.}$
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT16863, SN74ABT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16863 is an 18-bit noninverting transceiver designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

The 'ABT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable (OEAB or OEBA) inputs.

SN54ABT16863...WD PACKAGE SN74ABT16863...DL PACKAGE (TOP VIEW)

1	_	т т			
10EAB[	1	O	56	þ	10EBA
1B1 [	2		55	þ	1A1
1B2 [			54	þ	1A2
GND [	4		53	1	GND
1B3 [					1A3
1B4 [	6		51	0	1A4
Vcc[	7		50	þ	Vcc
1B5 [	8				1A5
1B6 🛚					1A6
1B7 🛚	10				1A7
GND [					GND
1B8 [					1A8
1B9 [					1A9
GND [					GND
GND [			42	ם	GND
2B1 [					2A1
2B2 🛚	17				2A2
GND [					GND
2B3 [	19		38	0	2A3
2B4 [					2A4
2B5 [			36		2A5
Vcc [	22		35	0	$V_{CC}$
2B6 🛚					2A6
2B7 [			33		2A7
GND [			32	0	GND
2B8 [					2A8
2B9 [				_	2A9
20EAB [	28		29		20EBA

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16863 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16863 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16863 is characterized for operation from -40°C to 85°C.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated

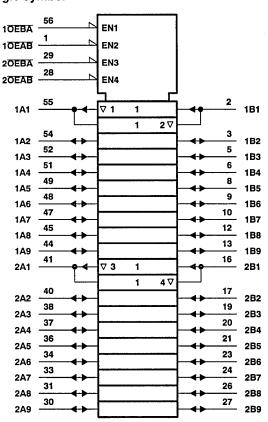
# SN54ABT16863, SN74ABT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

# FUNCTION TABLE (each 9-bit section)

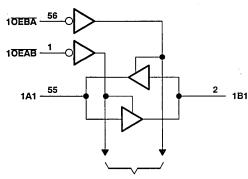
	•	<u> </u>		
INPUTS		OPERATION		
OEAB	OEBA	OPERATION		
Н	L	B data to A bus		
L	Н	A data to B bus		
н	Н	Isolation		

# logic symbol<sup>†</sup>

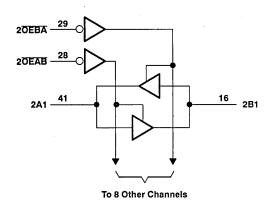


# <sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



To 8 Other Channels



# SN54ABT16863, SN74ABT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†						
Supply voltage range, V <sub>CC</sub> 0.5 V to 7 V						
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)						
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub>						
Current into any output in the low state, Io: SN54ABT16863						
SN74ABT16863						
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)						
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)						
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)						
Storage temperature range						

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54ABT16863		SN74ABT16863		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage			5.5	4.5	5.5	٧
VIH	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	V <sub>CC</sub>	٧
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



# SN54ABT16863, SN74ABT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T	A = 25°0	•	SN54AB	T16863	SN74ABT16863		UNIT
PARAMETER	'E	TEST CONDITIONS				MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	/, I <sub>i</sub> = –18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$					2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m	A	2			2				Πľ
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = - 32 mA		A	2‡					2		1
V.	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	ľ
	V <sub>CC</sub> = 5.5 V,	Control inputs			±1		±1		±1		
lj	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
lozh <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
lozL§	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V					-50		-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100		1		±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
-	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			32		32		32	mA
	$V_I = V_{CC}$ or GND		Outputs disabled			2		2		2	]
	V <sub>CC</sub> = 5.5 V, One	Data innuts	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control input	s			1.5		1.5		1.5	1
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs								pF
Cio	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,	A or B ports								pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		cc = 5 V \ = 25°C		SN54AB	Г16863	SN74AB1	Г16863	UNIT	
	( 0.)	(551.51,	MIN	TYP	MAX	MIN	MAX	MIN	MAX	. [	
t <sub>PLH</sub>	A or B	B or A						1	3.5	ns	
t <sub>PHL</sub>	] ^0'5	5017						1.2	4.3	113	
t <sub>PZH</sub>	OEBA or OEAB	A or B						1.3	4.9	ns	
t <sub>PZL</sub>	OLDA OF OLAB	7010						1.7	5.4	] "5	
t <sub>PHZ</sub>	OEBA or OEAB	A or B						1.9	5.1	ns	
t <sub>PLZ</sub>	OLDA OF OEAB	7018						1.4	5.4	, 115	

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

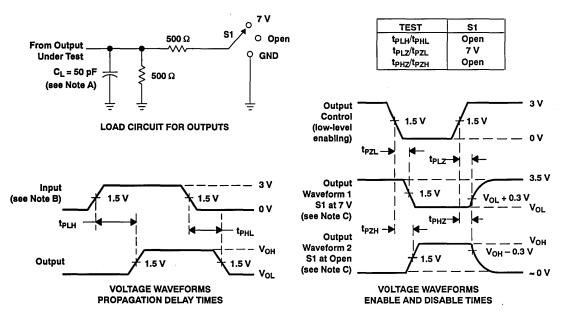
<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54ABT16863, SN74ABT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS082A-D3801, FEBRUARY 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT16952 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16952 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

SN54ABT16952...WD PACKAGE SN74ABT16952...DL PACKAGE (TOP VIEW)

\_\_\_\_

1OEAB[	1	56	1OEBA
1CLKAB[	2	55	] 1CLKBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A1[	5		] 1B1
1A2[	6	51	] 1B2
V <sub>cc</sub> [			] v <sub>cc</sub>
1A3[]			] 1B3
1A4[			] 1B4
1A5[]	10	47	] 1B5
GND	11	46	GND
1A6	12		1B6
1A7	13		] 1B7
1A8	14		] 1B8
2A1 🛚	15		] 2B1
2A2	16		] 2B2
2A3	17		] 2B3
GND	18		] GND
2A4	19		] 2B4
2A5[]	20		] 2B5
2A6	21		] 2B6
Vcc	22		] v <sub>cc</sub>
2A7	23		2B7
2A8			] 2B8
GND	25		GND
2CEAB	26		2CEBA
2CLKAB	27	30	
2OEAB	28	29	20EBA

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16952 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16952 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT16952 is characterized for operation from  $-40^{\circ}$ C to 85°C.

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# SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS082A-D3801, FEBRUARY 1991-REVISED OCTOBER 1992

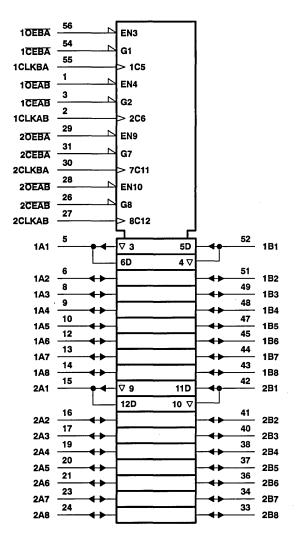
#### **FUNCTION TABLE<sup>†</sup>**

	INPUTS							
CEAB	CLKAB	OEAB	Α	В				
Н	Х	L	X	B₀‡				
×	L	L	×	В <sub>0</sub> ‡ В <sub>0</sub> ‡				
L	t	L	L	L				
L	<b>†</b>	L	Н	Н				
X	X	Н	X	z				

<sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses  $\overline{\text{CEBA}}$ , CLKBA, and  $\overline{\text{OEBA}}$ .

<sup>‡</sup> Level of B before the indicated steady-state input conditions were established.

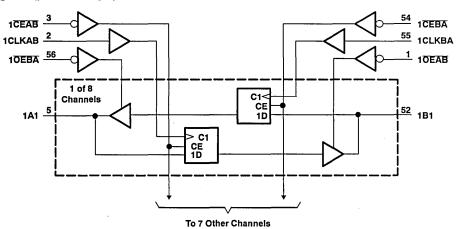
# logic symbol†

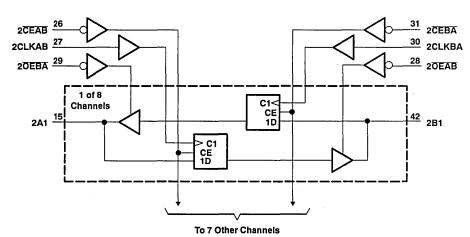


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS082A-D3801, FEBRUARY 1991-REVISED OCTOBER 1992

### logic diagram (positive logic)





#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	–0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16952	96 mA
SN74ABT16952	128 mA
Input clamp current, $I_{iK}$ ( $V_i < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



SCBS082A-D3801, FEBRUARY 1991-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54AB	T16952	SN74AB		
		•	MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2	39	2		V
VIL	Low-level input voltage		1	<b>∜</b> 0.8		0.8	V
VI	Input voltage		0,4	V <sub>CC</sub>	0	Vcc	V
loh	High-level output current		Ş	-24		-32	mA
loL	Low-level output current		N.	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	85	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAUETED	IETER TEST CONDITIONS			Т	A = 25°C	;	SN54ABT16952		SN74ABT16952		UNIT	
PARAMETER	153	ONDITIC	INS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>l</sub> = -18 mA				-1.2		-1.2		-1.2	V	
	V <sub>CC</sub> = 4.5 V,	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$					2.5		2.5			
.,	V <sub>CC</sub> = 5 V,	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3		v	
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = - 24 r	пA	2			2				V	
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2			
.,	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA	\			0.55		0.55	· · · · · · · · · · · · · · · · · · ·			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA		\			0.55‡		67		0.55	V	
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		, ±1		±1		
$V_1 = V_{CC}$ or GND			A or B ports			±100	,	€±100		±100	μA	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	<i>A</i> -	50		50	μА	
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	,3"	-50		-50	μΑ	
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$	.5 V			±100	,O'			±100	μΑ	
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Q.	50		.50	μΑ	
lo <sup>¶</sup>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V		-50	-100	-200	-50	-200	-50	-200	mA	
	V <sub>CC</sub> = 5.5 V,		Outputs high			2		2		2		
Icc	$I_0 = 0$ ,	A or B ports	Outputs low			35		35		35	mA	
	$V_I = V_{CC}$ or GND	Ports	Outputs disabled			2		2		2		
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				0.5		0.5		0.5	mA		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs			3						pF		
Cio	V <sub>O</sub> = 2.5 V or 0.5 V	,	A or B ports		8.5						pF	

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>\</sup>S$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT16952, SN74ABT16952 **16-BIT REGISTÉRED TRANSCEIVERS** WITH 3-STATE OUTPUTS SCBS082A-D3801, FEBRUARY 1991-REVISED OCTOBER 1992

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

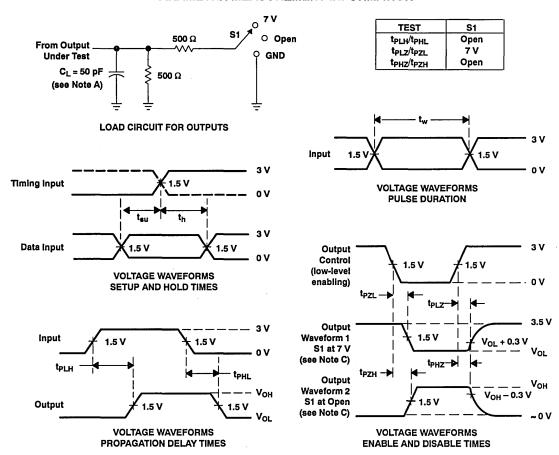
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16952		SN74ABT16952		UNIT	
			MIN	MAX	MIN MAX		MIN	MAX		
f <sub>clock</sub>	olock Clock frequency			150	0 ,	150	0	150	MHz	
tw <sup>†</sup>	Pulse duration, CLKAB or CLKBA high or low		3.3		3.3(2)		3.3		ns	
	Cohun time hafara CLIVARA as CLIVARA	A or B	3.5		3(5°,	(y	3.5			
t <sub>su</sub>	Setup time, before CLKAB† or CLKBA†	CEAB or CEBA	3		Q 3(V)	•	3		ns	
	Hold time ofter CLIVARA or CLIVARA	A or B	1		* 9		1			
th	Hold time, after CLKAB† or CLKBA†	CEAB or CEBA	1		1		1		ns	

<sup>†</sup> This parameter is specified by design but not tested.

#### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_1 = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16952		SN74ABT16952		UNIT
	( 01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150			150		150		MHz
t <sub>PLH</sub>	CLK	A or B	1	2.6	3.9	16	4.4	1	4.3	ns
t <sub>PHL</sub>	OLK	_ ^ OF B	1	2.6	4.2	83.6	7 4.6	1	4.5	113
t <sub>PZH</sub>	Œ	A or B	1	2.5	3.8	\Q\(\rho\)	4.7	1	4.6	ns
t <sub>PZL</sub>	Ų.	A or B	1	2.8	5.1	6. 9c	6.1	1	6	113
t <sub>PHZ</sub>	ŌĒ	A or B	1.7	3.4	4.7	1.7	6.1	1.7	5.5	ns
t <sub>PLZ</sub>	OE .		1.3	3	3.9	1.3	4.8	1.3	4.2	115

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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#### ABT Widebus+™

#### **Features**

- 32- and 36-bit bus interface
- EIAJ standard 80-, 100-, and 120-pin shrink quad flat packs (SQFPs)
- Enhanced UBT™ architectures that include global controls and parity generate and check
- Multiport universal bus exchanger (UBE™) architectures
- Symmetrical flowthrough pinouts with controls at the poles
- Bit partitioning
- Distributed pinout with 12 GND pins and 4 V<sub>CC</sub> pins
- Bus-hold circuitry
- Power-on-demand active feedback circuit
- TI has established an alternate source

#### Benefits

- Single-chip implementation for highest level of logic integration
- 35% less board space than equivalent PQFPs; over 50% less board space than 4 octal SOIC equivalents
- Special features for use in high-performance RISC/CISC/X86 microprocessor systems
- Multiplexing and memory interleaving capability for interbus communication
- Ease of board layout; provides compatible top-side or bottom-side mount
- Global, x 18-, or x 9-bit capability for flexible partitioning
- 3:1 signal-to-GND ratio minimizes simultaneous switching noise and mutual coupling effects
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces enabled static power consumption (I<sub>CCL</sub>) by over 50%
- Standardization that comes from a common product approach

The following table lists ABT Widebus+™ devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the General Purpose Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT32319	80	18-Bit Tri-Port Registered Bus Exchanger With Clock Enable
'ABT32600	100	36-Bit Universal Bus Transceiver With Clock Enable
'ABT32601	100	36-Bit Universal Bus Transceiver With Clock Enable
'ABT32700	120	36-Bit Universal Bus Transceiver With Byte Enable
'ABT32701	120	36-Bit Universal Bus Transceiver With Byte Enable
'ABT32900	120	36-Bit Universal Bus Transceiver With Parity Generate and Check
'ABT32901	120	36-Bit Universal Bus Transceiver With Parity Generate and Check

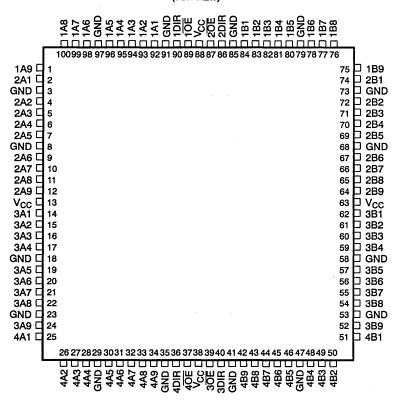
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- Members of the Texas Instruments
   Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA l<sub>OH</sub>, 64-mA l<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 × 14-mm Package Body Using 0.5-mm Lead Pitch

SN74ABT32245...PZ PACKAGE (TOP VIEW)



## description

The 'ABT32245 is a 36-bit (quad 9-bit) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

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#### description (continued)

This device can be used as four 9-bit transceivers, two18-bit transceivers, or one 36-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) inputs. The output-enable (OE) inputs can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT32245 is characterized for operation from  $-40^{\circ}$ C to 85°C.

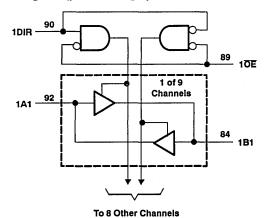
# FUNCTION TABLE (each 9-bit section)

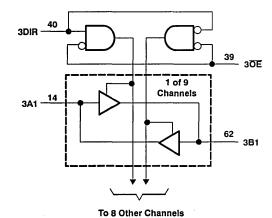
INP	UTS	OPERATION
ŌΕ	DIR	OPERATION
Ĺ	L	B data to A bus
L	Н	A data to B bus
Η	X	Isolation

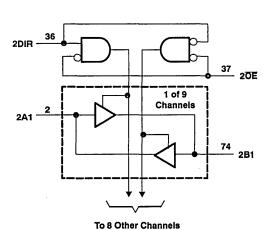


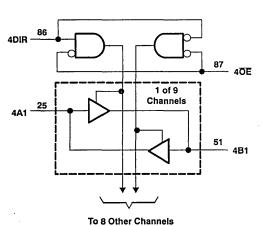
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### logic diagram (positive logic)









Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32245	96 mA
SN74ABT32245	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Storage temperature range	-40°C to 150°C

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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#### recommended operating conditions

		•	SN54ABT32245		SN74AB	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage				2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	٧
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEST CONDITIONS			SN5	4ABT32	245	SN74ABT32245					
PARAMETER		TEST CONDITIONS			MIN	TYP <sup>†</sup>	MAX	MIN	TYP	MAX	UNIT		
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	l <sub>i</sub> = –18 mA				-1.2			-1.2	٧		
		V <sub>CC</sub> = 4.5 V, 1	l <sub>OH</sub> = -3 mA		2.5			2.5					
		V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3			l v		
V <sub>ОН</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						<b>'</b>		
ł		V <sub>CC</sub> = 4.5 V,	l <sub>OH</sub> = -32 mA					2					
VoL		V <sub>CC</sub> = 4.5 V,	OL = 48 mA				0.55			0.55	V		
▼OL		V <sub>CC</sub> = 4.5 V,	OL = 64 mA							0.55	\ \ \		
1.	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND								±1			
lı	A or B ports									±100	μΑ		
ī	A or B ports	$V_{CC} = 4.5 \text{ V}, \qquad V_{I} = 0.8 \text{ V}$						100			μА		
hold	A OI B POILS	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V						-100			1 "		
lozh‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V							50	μΑ		
l <sub>OZL</sub> ‡		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V							-50	μΑ		
loff		V <sub>CC</sub> = 0,	$V_1 \text{ or } V_0 \le 4.5 \text{ V}$							±100	μΑ		
I <sub>CEX</sub>	-	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ		
lo <sup>§</sup>		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V					50	-100	-180	mA		
		V 55V		Outputs high						2			
Icc		$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	10 = 0,	Outputs low						5	mA		
		AI = ACC OL CLAD		Outputs disabled						0.5			
Δlcc¶		$V_{CC} = 5.5 \text{ V},$ Other inputs at $V_{C}$		1 V,						1	mA		
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V								pF			
Cio	A or B ports	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	V								pF		

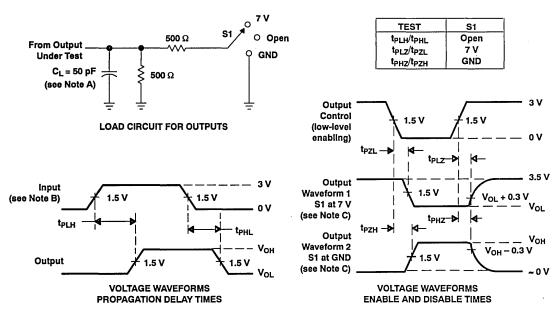
<sup>†</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C. ‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

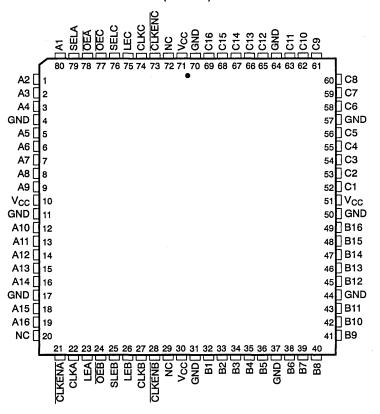
Figure 1. Load Circuit and Voltage Waveforms



- Members of the Texas Instruments Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- UBE™ (Universal Bus Exchanger)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 80-Pin Plastic Shrink Quad Flat Pack (SQFP) With 12 x 12-mm Package Body Using 0.5-mm Lead Pitch

SN74ABT32316...PN PACKAGE (TOP VIEW)



NC - No internal connection

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#### description

The 'ABT32316 consists of three 16-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable (OEA, OEB, and OEC), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A-data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA and clock enable A (CLKENA) are low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32316 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT32316 is characterized for operation from -40°C to 85°C.

#### STORAGE FUNCTION TABLE<sup>†</sup>

	INPUTS						
CLKENA	CLKA	LEA	Α	OUTPUT			
Н	Х	L	X	Q <sub>0</sub> ‡			
L	†	L.	L	L			
L	<b>†</b>	L	Н	н			
x	н	L	X	Q₀‡ Q₀‡			
x	L	L.	X	Q <sub>0</sub> ‡			
×	X	н	L	L			
X	X	Н	Н	Н			

<sup>†</sup> A-port register shown. B and C ports are similar but use CLKENB, CLKENC, CLKB, CLKC, LEB, and LEC.

Output level before the indicated steady-state input conditions were established.

#### A-PORT OUTPUT FUNCTION TABLE

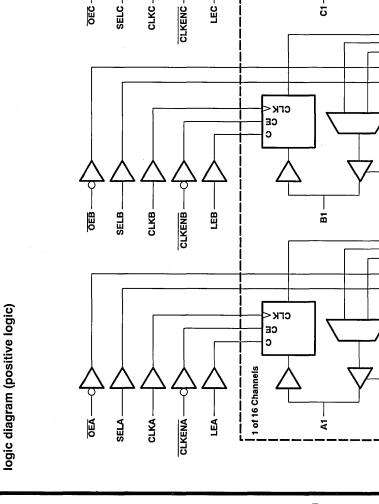
INP	UTS	OUTPUT
OEA	SELA	Α
Н	×	Z
L	Н	Output of C register
L	L	Output of B register

#### **B-PORT OUTPUT FUNCTION TABLE**

INP	UTS	OUTPUT
OEB	SELB	В
Н	Х	Z
L	н	Output of A register
L	L	Output of C register

#### **C-PORT OUTPUT FUNCTION TABLE**

0-1-011	O-F CHI COTT OTT CHOTICH TABLE							
INP	UTS	OUTPUT						
OEC	SELC	С						
Н	Х	Z						
L	• Н	Output of B register						
L	i.	Output of A register						





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absolute maximum ratings over operating free-air temperature range (unless other	wise noted)†
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>1</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, $V_0$	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32316	96 mA
SN74ABT32316	128 mA
Input clamp current, $I_{ K }(V_{ } < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Storage temperature range	-40°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

			SN54AB	Г32316	SN74AB		
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ဝ့

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ADAMETED		TEST CONDITIONS			SN54ABT32316			SN74ABT32316				
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	MIN	TYP	MAX	UNIT		
VIK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧		
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5					
		V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3			v		
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						· •		
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA					2					
<u></u>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55			0.55	V		
VOL		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55			
	Control inputs	V 55V	V V Ch	ID						±1			
4	A, B, or C ports	$V_{CC} = 5.5 \text{ V},  V_{I} = V_{CC} \text{ or GND}$				-				±100	μА		
	A, B, or C ports	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V						100					
hold	A, B, or C ports	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V						-100			μΑ		
I <sub>OZH</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V							50	μА		
lozL <sup>‡</sup>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V							-50	μА		
I <sub>OFF</sub>		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 \	7						±100	μА		
I <sub>CEX</sub>		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high		,				50	μА		
l <sub>O</sub> §		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA		
				Outputs high	_					2			
Icc		$V_{CC} = 5.5 \text{ V},$		Outputs low						5	mA		
		1 41 = ACC 01 CIV	V <sub>I</sub> = V <sub>CC</sub> or GND							0.5			
Δlcc			V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND							0.5	mA		
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V									pF		
Cio	A, B, or C ports	V <sub>O</sub> = 2.5 V or 0	.5 V								pF		

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

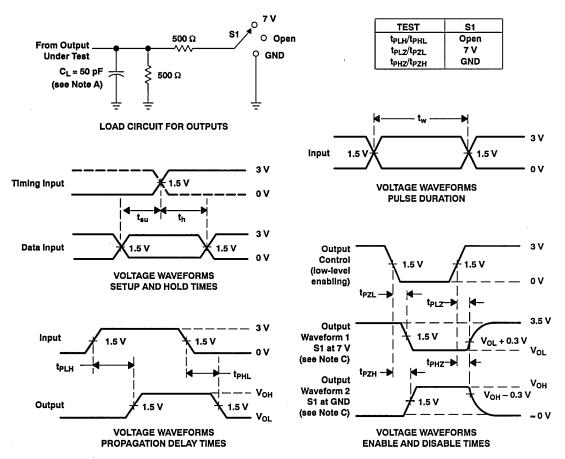
† The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# Members of the Texas Instruments Widebus+™ Family

- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBE ™ (Universal Bus Exchanger)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

 Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

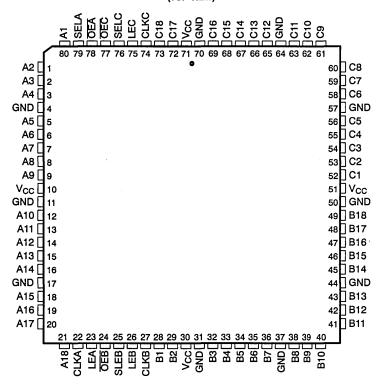
SN54ABT32318, SN74ABT32318

Typical V<sub>OLP</sub> (Output Ground Bounce)
 < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

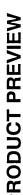
18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 80-Pin Plastic Shrink Quad Flat Pack (SQFP) With 12 × 12-mm Package Body Using 0.5-mm Lead Pitch

# SN74ABT32318...PN PACKAGE (TOP VIEW)



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#### description

The 'ABT32318 consists of three 18-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable (OEA, OEB, and OEC), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A-data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA is low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32318 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32318 is characterized for operation from –40°C to 85°C.

#### STORAGE FUNCTION TABLET

	NPUTS	ОИТРИТ	
CLKA	LEA	Α	001701
1	L	L	L
1	L	Н	н
н	L	X	Q <sub>0</sub> ‡
L	L	Х	Q₀ <sup>‡</sup> Q₀ <sup>‡</sup>
x	н	L	L
x	н	н	н .

<sup>&</sup>lt;sup>†</sup> A-port register shown. B and C ports are similar but use CLKB, CLKC, LEB, and 'LEC.

Output level before the indicated steady-state input conditions were established.

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#### A-PORT OUTPUT FUNCTION TABLE

	INP	UTS	OUTPUT				
	OEA	SELA	A				
	Н	Х	Z				
	L	н	Output of C register				
į	L	L	Output of B register				

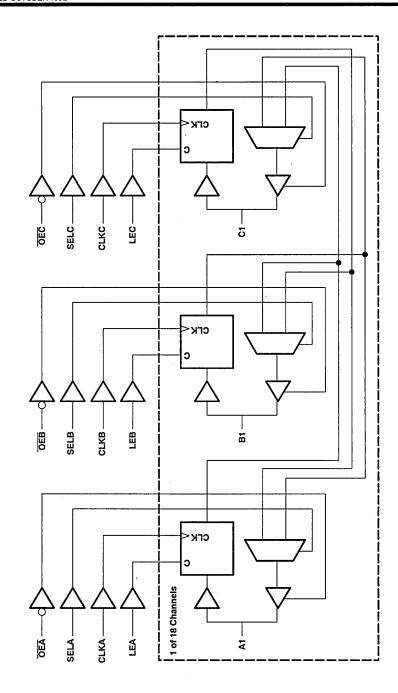
#### **B-PORT OUTPUT FUNCTION TABLE**

I	INPUTS		OUTPUT				
I	OEB	SELB	В				
ſ	Н	Х	Z				
ı	L	н	Output of A register				
l	L	L	Output of C register				

#### **C-PORT OUTPUT FUNCTION TABLE**

INP	UTS	OUTPUT				
OEC	SELC	С				
Н	Х	Z				
L	Н	Output of B register				
L	L	Output of A register				





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absolute maximum ratings over operating free-air temperature range (unless of	ierwise noted) i
Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32318	96 mA
SN74ABT32318	128 mA

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions

			SN54AB	T32318	SN74AB7	Г32318	UNIT
		MIN	MAX	MIN	MAX	UNII	
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>lH</sub>	High-level input voltage				2		٧.
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	٧
VI	Input voltage		0	Vcc	0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	1	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABT32318			SN74ABT32318					
					MIN	TYP	MAX	MIN	TYP	MAX	UNIT		
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		i		-1.2			-1.2	٧			
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2.5			2.5			v		
					3			3					
					2								
		V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$					2			1		
.,		V <sub>CC</sub> = 4.5 V,					0.55						
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55	V		
	Control inputs			·						±1			
lı	A, B, or C ports		V <sub>I</sub> ≈ V <sub>CC</sub> or GND							±100	μΑ		
	A D 0	$V_{CC} = 4.5 \text{ V},$	V <sub>I</sub> = 0.8 V					100					
hold	A, B, or C ports	$V_{CC} = 4.5 \text{ V},$	V <sub>i</sub> = 2 V					-100			μА		
l <sub>OZH</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V							50	μΑ		
l <sub>OZL</sub> ‡		$V_{CC} = 5.5 \text{ V},$	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V							-50	μΑ		
loff		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V					,		±100	μΑ		
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ		
10 <sup>\$</sup>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA		
			Outputs high						2				
lcc		$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low						5	mA			
		ALT ACC OF CIAD		Outputs disabled						0.5			
∆lcc¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND							0.5	mA			
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V								pF			
Cio	A, B, or C ports	V <sub>O</sub> = 2.5 V or 0.5 V								pF			

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

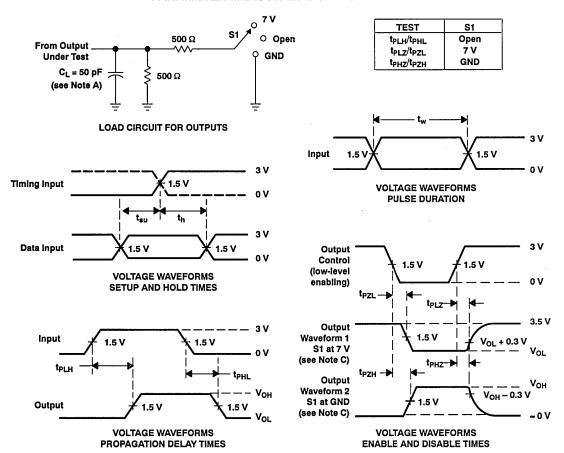
<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns.  $t_f \leq 2.5$  ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

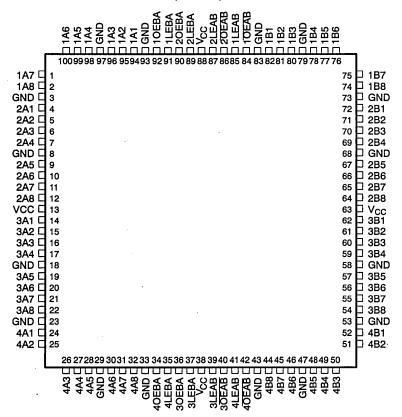
# SN54ABT32373, SN74ABT32373 32-BIT TRANSCEIVERS WITH D-TYPE LATCHES AND 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged In 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 x 14-mm Package Body Using 0.5-mm Lead Pitch

# SN74ABT32373 . . . PZ PACKAGE (TOP VIEW)



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#### description

The 'ABT32373 is a 32-bit (quad 8-bit) transceiver with D-type latches and 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable inputs.

The output-enable (OEAB or OEBA) inputs do not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (A to B). OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (B to A).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32373 is characterized for operation from –40°C to 85°C.

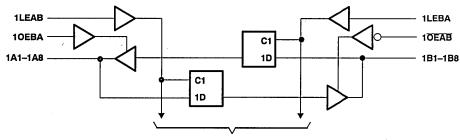
FUNCTION TABLE†
(each transceiver)

	INPUTS							
OEAB	LEAB	Α	В					
L	Н	Н	Н					
L	Н	L	L					
L	L	×	Q <sub>0</sub>					
Н	Х	Х	z					

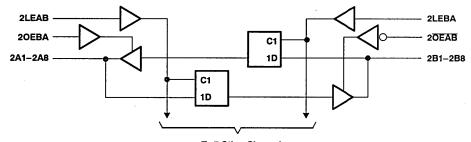
<sup>&</sup>lt;sup>†</sup> A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA and LEBA.

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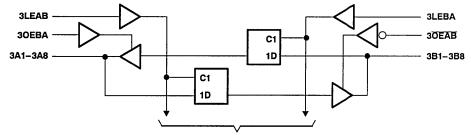
#### logic diagram (positive logic)



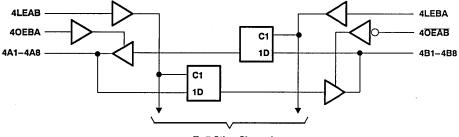
To 7 Other Channels



To 7 Other Channels



To 7 Other Channels



To 7 Other Channels

JUNE 1992-REVISED OCTOBER 1992

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> 0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, Vo0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32373
SN74ABT32373
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

					SN74ABT32373		UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	/IH High-level input voltage				2		V
V <sub>IL</sub>	Low-level input voltage			8.0		0.8	V
V <sub>I</sub>	Input voltage		0	Vcc	0	Vcc	V
loн	High-level output current			-24		-32	mA
IOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C



JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	D.4.11ETED		TEST CONDITIONS			SN54ABT32373			SN74ABT32373		
P#	RAMETER	,				TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
ViK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5			
l,		V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3			v
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						· •
		V <sub>CC</sub> = 4.5 V,	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$					2			
,,,,,		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55			0.55	\ \
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55	v
	Control inputs	V 5.5.V	$V_{CC} = 5.5 \text{ V}$ , $V_{I} = V_{CC} \text{ or GND}$							±1	μА
li li	A or B ports	$V_{CC} = 5.5 \text{ V},$	U						±100		
,	A or B north	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V						100			
I <sub>hold</sub>	A or B ports	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 2 V					-100			μА
lozh‡		$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$							50	μА	
loz <sub>L</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V							-50	μА
loff		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	<i>,</i>						±100	μA
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ
lo <sup>§</sup>		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA
		V 55V		Outputs high						2	
lcc		$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$		Outputs low						5	mA
		ALT ACC OF CITY		Outputs disabled						0.5	]
Δlcc¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND							1	mA	
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5	V <sub>I</sub> = 2.5 V or 0.5 V								pF
Cio	A or B ports	$V_0 = 2.5 \text{ V or } 0.5$	i V								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$ .

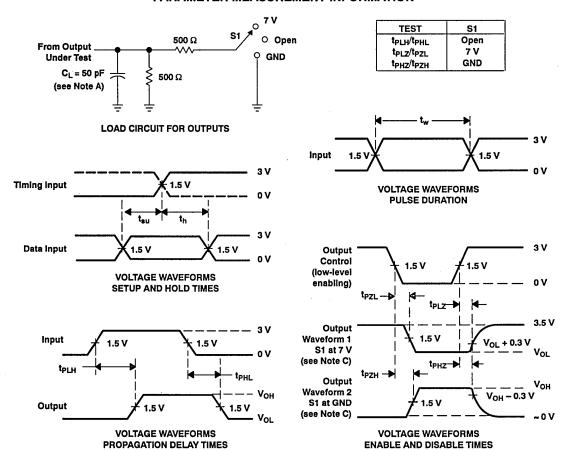
<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>5</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>1</sup> This is the Increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

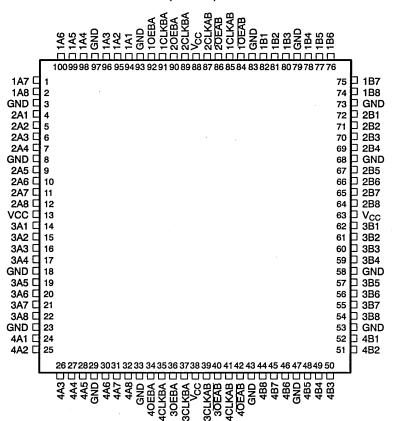


JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 x 14-mm Package Body Using 0.5-mm Lead Pitch

# SN74ABT32374...PZ PACKAGE (TOP VIEW)



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JUNE 1992-REVISED OCTOBER 1992

#### description

The 'ABT32374 is a 32-bit (quad 8-bit) transceiver with edge-triggered D-type flip-flops and 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT32374 can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLKAB or CLKBA) input, the B outputs of the flip-flop take on the logic levels set up at the A inputs. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable inputs.

A buffered output-enable (OEAB or OEBA) input can be used to place the 32 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (OEAB or OEBA) does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (A to B). OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (B to A).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32374 is characterized for operation from –40°C to 85°C.

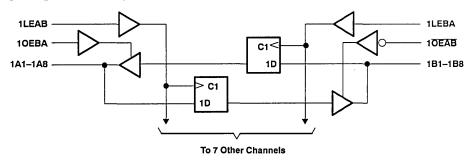
FUNCTION TABLE† (each flip-flop)

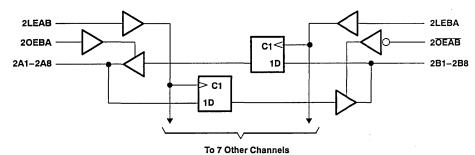
	INPUTS	OUTPUT	
OEAB	CLKAB	Α	В
L	†	Н	Н
L	<b>†</b>	L	L
L	L	X	Qo
н	X	х	z

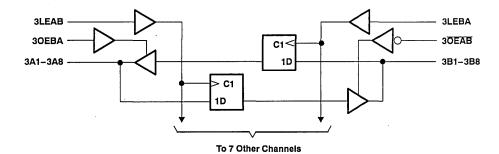
<sup>†</sup> A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA and CLKBA.

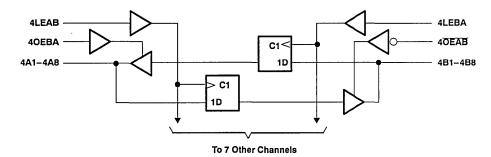
# SN54ABT32374, SN74ABT32374 32-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

logic diagram (positive logic)











JUNE 1992-REVISED OCTOBER 1992

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$-0.5\mathrm{V}$ to $7\mathrm{V}$
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32374	96 mA
SN74ABT32374	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Storage temperature range4	40°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

			SN54AB	T32374	SN74AB	UNIT		
			MIN	MAX	MIN	MIN MAX		
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V	
VIH	High-level Input voltage				2		V	
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V	
VI	Input voltage		0	Vcc	0	Vcc	٧	
I <sub>OH</sub>	High-level output current			-24		-32	mA	
loL	Low-level output current			48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	



JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED			TEST CONDITIONS			4ABT32	374	SN74ABT32374			UNIT
Ρ/	ARAMETER		TEST CONDITIONS			TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	= 4.5 V, I <sub>i</sub> = -18 mA				-1.2			-1.2	٧
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5			
.,		V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3			v
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						V
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA						2			
.,		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA		1		0.55			0.55	V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA								0.55	V
1	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND							±1		
lį	A or B ports			ND		*				±100	μΑ
1	A B	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V						100			
lhold	A or B ports							-100			μΑ
loz <sub>H</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V							50	μA
loz <sub>L</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V							-50	μΑ
loff		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	V						±100	μΑ
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ
lo§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA
		V 55V		Outputs high						2	
lcc		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GN	l <sub>O</sub> = 0,	Outputs low						5	·mA
		11-1660.00		Outputs disabled						0.5	
Δlcc		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND							1	mA	
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5	V <sub>I</sub> = 2.5 V or 0.5 V								pF
Cio	A or B ports	V <sub>O</sub> = 2.5 V or 0	.5 V							_	pF

 $<sup>\</sup>dagger$  All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C.

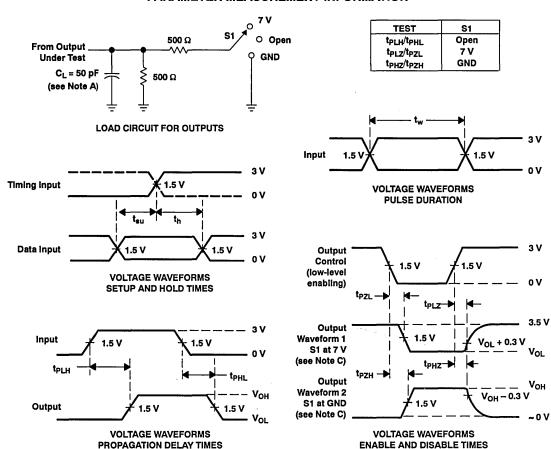
<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

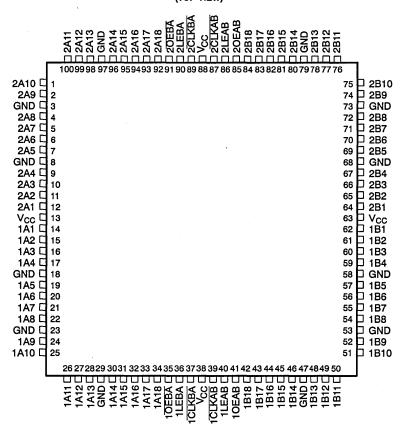
Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 x 14-mm Package Body Using 0.5-mm Lead Pitch

# SN74ABT32500 . . . PZ PACKAGE (TOP VIEW)



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JUNE 1992-REVISED OCTOBER 1992

#### description

These 36-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32500 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

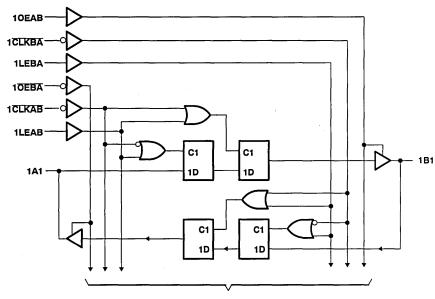
	INPUTS							
OEAB	OEAB LEAB CLKAB A							
L.	Х	Х	X	Z				
Н	Н	X	L	L				
Н	Н	X	Н	н				
Н	L	<b>↓</b>	L	L				
н	L	1	Н	н				
н	L	Н	X	В <sub>0</sub> ‡ В <sub>0</sub> §				
Н	L	L	Х	B <sub>0</sub> §				

<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

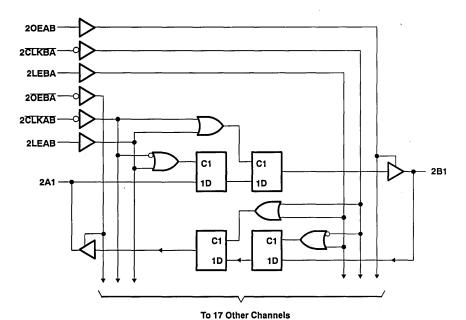
Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

# logic diagram (positive logic)



To 17 Other Channels



Instruments

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	T32500	SN74AB	UNIT	
1			MIN	MAX	MIN MAX		UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	္င

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

JUNE 1992-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER		TEST COMPLE	IONIC	SN5	4ABT32	500	SN74ABT32500			UNIT
"	ARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	MIN	TYP	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	l <sub>I</sub> = -18 mA				-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -3 mA		2.5			2.5			
l.,		V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3			V
V <sub>ОН</sub>	•	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						٧
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA					2		-	
· ·		$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 48 mA				0.55			0.55	V
VoL		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55	V
	Control inputs	V 55V								±1	
li I	A or B ports	$V_{CC} = 5.5 \text{ V},$	$V_i = V_{CC}$ or $GI$	טא						±100	μΑ
_	A or B norto	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V						100			
I <sub>hold</sub>	A or B ports										μΑ
lozH‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V							50	μΑ
lozL‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V						_	-50	μА
loff		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	V						±100	μА
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ
lo§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA
		V 55V		Outputs high						2	
lcc		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GNI		Outputs low						60	mA
		1 1 - 466 01 0141	•	Outputs disabled		_				0.5	
Δlcc¶		V <sub>CC</sub> = 5.5 V, Other inputs at		3.4 V,						1	mA
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5	5 V	······································	İ			-			pF
Cio	A or B ports	V <sub>O</sub> = 2.5 V or 0.	5 V								pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

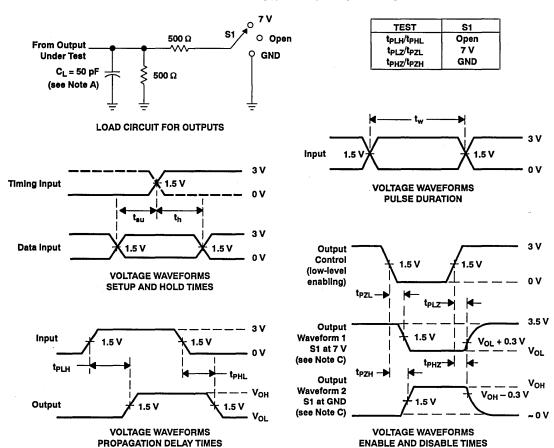
† The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

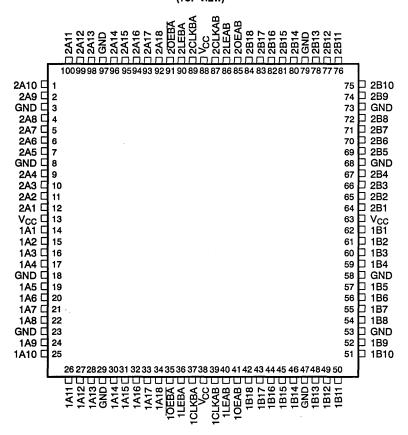
Figure 1. Load Circuit and Voltage Waveforms

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- **Members of the Texas Instruments** Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design **Significantly Reduces Power Dissipation**
- **UBT** ™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF,

- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 5 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (–32-mA l<sub>OH</sub>, 64-mA loL)
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 × 14-mm Package **Body Using 0.5-mm Lead Pitch**

#### SN74ABT32501 . . . PZ PACKAGE (TOP VIEW)



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JUNE 1992-REVISED OCTOBER 1992

#### description

These 36-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32501 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE<sup>†</sup>** 

	INPUTS							
OEAB	OEAB LEAB CLKAB A							
L	Х	Х	X	Z				
Н	Н	X	L	L				
н	Н	X	Н	н				
Н	L	<b>†</b>	L	L				
Н	L	<b>†</b>	Н	Н				
Н	L	н	X	B₀‡				
Н	L	L	Х	B₀ <sup>‡</sup> B₀ <sup>§</sup>				

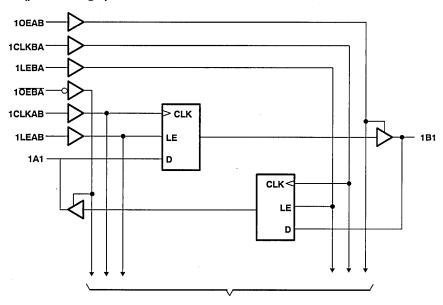
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established.

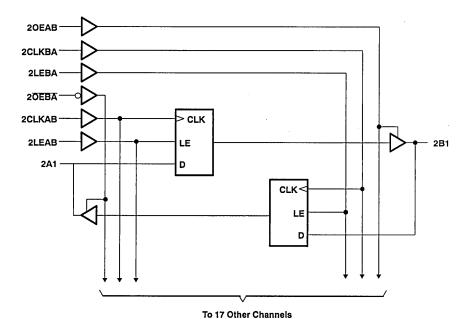
<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

JUNE 1992-REVISED OCTOBER 1992

# logic diagram (positive logic)



To 17 Other Channels



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JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings ove	r operating free-ai	r temperature range	(unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32501	96 mA
SN74ABT32501	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Storage temperature range	-40°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	SN54ABT32501		SN74ABT32501		
1			MIN	MAX	MIN MAX		UNIT	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	٧	
V <sub>IH</sub>	High-level input voltage		2		2		٧	
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V	
Vi	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	٧	
Іон	High-level output current			-24		-32	mA	
loL	Low-level output current			48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	ç	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER		TECT CONDITIO	oue.	SN5	4ABT32	501	SN74ABT32501			UNIT	
P/	RAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	TYP <sup>†</sup>	MAX	UNII	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	$V_{CC} = 4.5 \text{ V}, \qquad I_{\parallel} = -18 \text{ mA}$				-1.2			-1.2	V	
	-	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$		2.5	<del></del>		2.5				
١.,		V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3			. <b>v</b>	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						· V	
		V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ mA}$				$\neg \neg$	2				
.,		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55			0.55		
VoL		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55	v	
	Control inputs	V 55V	V V ~ C	ID.						±1		
li ·	A or B ports	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = V_{CC} \text{ or GN}$		י טו						±100	μА	
1	A or B ports	$V_{CC} = 4.5 \text{ V}, \qquad V_{I} = 0.8 \text{ V}$					100			μΑ		
hold	A of B poils	$V_{CC} = 4.5 \text{ V}, \qquad V_{i} = 2 \text{ V}$										
l <sub>OZH</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	· · · · · · · · · · · · · · · · · · ·						50	μA	
lozL‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V							-50	μА	
I <sub>OFF</sub>		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 \	/						±100	μΑ	
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ	
lo§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA	
	_	V 55V		Outputs high						6		
Icc		$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GNE}$		Outputs low						90	mA	
		11-100010101		Outputs disabled						6		
Δlcc¶		V <sub>CC</sub> = 5.5 V, Other inputs at \		.4 V,						1	mA	
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V							3.5		pF	
Cio	A or B ports	V <sub>O</sub> = 2.5 V or 0.5	5 V						11.5		pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT32501		SN74AB	UNIT			
		,	MIN	MIN MAX		MIN MAX			
f <sub>clock</sub>	Clock frequency				0	150	MHz		
t <sub>w</sub> I	Pulse duration	LE high or low			3.3				
	Pulse duration	CLK high or low			3.3		ns		
	Oat at the a	A or B before CLK†			3.5		ns		
t <sub>su</sub>	Setup time	A or B before LE			1.6				
		A or B after CLK†			0				
t <sub>h</sub>	Hold time	A or B after LE			1.6		ns		

<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>&</sup>lt;sup>1</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT32501, SN74ABT32501 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

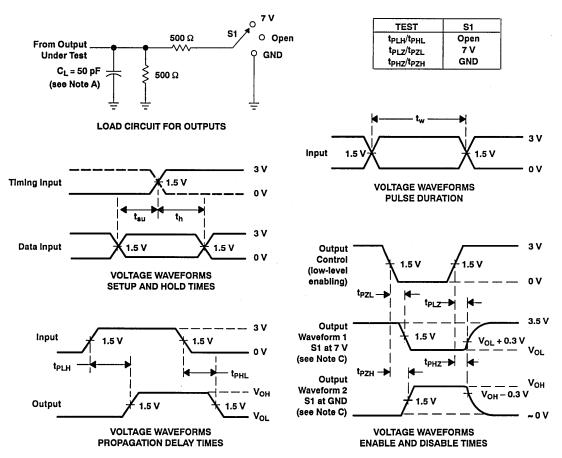
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	SN5	SN54ABT32501			4ABT32	501	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MiN	TYP	MAX	UNII
f <sub>max</sub>						150			MHz
t <sub>PLH</sub>	A or B	B or A				1.3	2.9	4.8	ns
t <sub>PHL</sub>	] ^0''	BOTA				1.4	2.7	5.3	ns
t <sub>PLH</sub>	LEAB or LEBA	B or A				1.6	3.4	5.1	ns
t <sub>PHL</sub>		BUIA				1.9	3.6	5.2	112
t <sub>PLH</sub>	CLKAB or CLKBA	B or A				1.5	3.2	4.9	ns
t <sub>PHL</sub>	CLIVAB OI CLIVBA	BOTA				1.7	3.3	4.9	115
t <sub>PZH</sub>	OEAB or OEBA	B or A				1.2	3.2	5.6	ns
t <sub>PZL</sub>	] OEAD OF OEBA	BULA				1.5	3.6	6	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A				1.8	3.6	5.9	ns
t <sub>PLZ</sub>	1 DEAD OF DEBA	D OF A				1.7	3.5	5.6	118



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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\leq}$  10 MHz,  $Z_0 = 50~\Omega$ ,  $t_f \leq 2.5~ns$ ,  $t_f \leq 2.5~ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

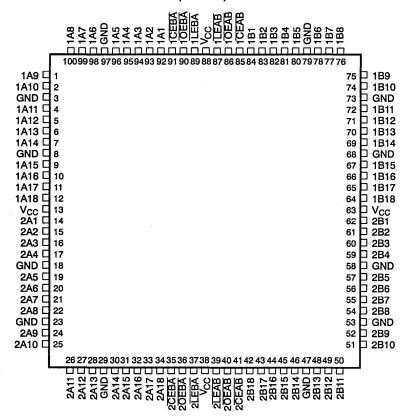
4-50

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 x 14-mm Package Body Using 0.5-mm Lead Pitch

# SN74ABT32543...PZ PACKAGE (TOP VIEW)



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#### description

The 'ABT32543 is a 36-bit registered transceiver that contains two sets of D-type latches for temporary storage of data flowing in either direction. The device can be used as two 18-bit transceivers or one 36-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT32543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE† (each 18-bit section)

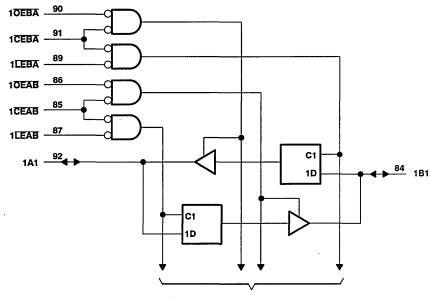
	INPL	OUTPUT		
CEAB	LEAB	OEAB	Α	В
Н	Х	Х	X	Z
×	X	Н	X	z
L	Н	L	X	B₀‡
L	L	L	L	L
L	L	L	Н	н

<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

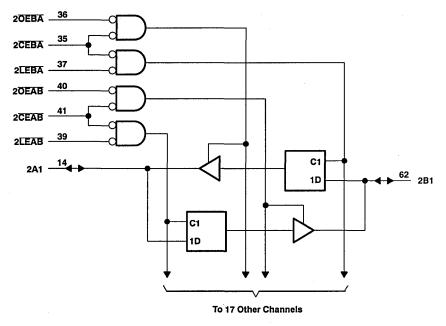
Output level before the indicated steady-state input conditions were established.

### SN54ABT32543, SN74ABT32543 36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

### logic diagram (positive logic)



To 17 Other Channels





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	
Current into any output in the low state, Io: SN54ABT32543	96 mA
SN74ABT32543	128 mA
Input clamp current, $I_{IK}(V_I < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Storage temperature range	-40°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

			SN54ABT32543		SN74AB	T32543	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	٧
Vi	Input voltage		0	Vcc	0	Vcc	٧
Гон	High-level output current			-24		-32	mA
I <sub>OL</sub>	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER		TECT CONDITI	ONO	SN5	4ABT32	543	SN74ABT32543			UNIT	
12/	ARAMETER		TEST CONDITIONS			TYP†	MAX	MIN	TYP†	MAX	UNII	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA				-1.2			-1.2	V	
		V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5				
.,		V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3			v	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA		2						\ \ \	
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA			· · · · · · · · · · · · · · · · · · ·		2				
.,		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55			0.55	V	
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55	\ \ \	
	Control inputs	V 55V		15						±1		
lj	A or B ports	V <sub>CC</sub> = 5.5 V,	$V_{CC} = 5.5 \text{ V}, \qquad V_I = V_{CC} \text{ or GND}$							±100	μΑ	
	A D	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V					100			^		
lhoid	A or B ports	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V						-100			μА	
lozh‡	-	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.7 V							50	μΑ	
lozL‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V							-50	μΑ	
loff		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5	V						±100	μΑ	
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ	
lo§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V					-50	-100	-180	mA	
		V 55V		Outputs high						2		
¹cc		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GN	l <sub>O</sub> = 0,	Outputs low						5	mA	
		AI = ACC OL CLAD		Outputs disabled						0.5		
Δlcc¶		$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND							1	mA		
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5	V <sub>I</sub> = 2.5 V or 0.5 V								pF	
Cio	A or B ports	V <sub>O</sub> = 2.5 V or 0.	5 V								pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

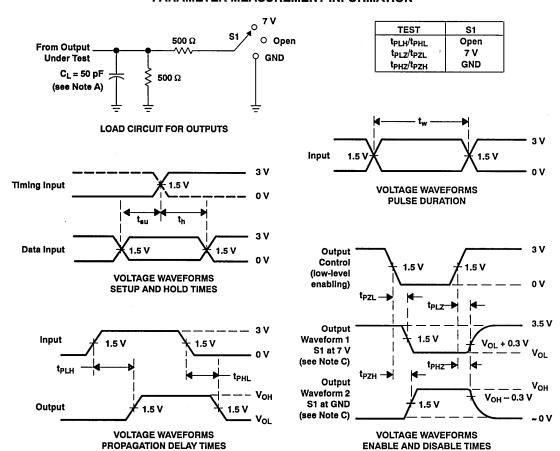
<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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#### PARAMETER MEASUREMENT INFORMATION



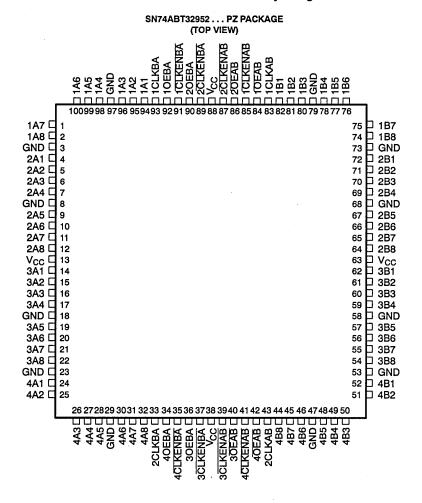
- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_f \leq 2.5 \ ns$ ,  $t_f \leq 2.5 \ ns$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   Widebus+™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Packaged in 100-Pin Plastic Shrink Quad Flat Pack (SQFP) With 14 x 14-mm Package Body Using 0.5-mm Lead Pitch



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#### description

The 'ABT32952 is a 32-bit (quad 8-bit) transceiver with edge-triggered D-type flip-flops and 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The 'ABT32952 can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. Provided that the clock-enable (CLKENAB or CLKENBA) input is low on the positive transition of the clock (CLKAB or CLKBA) input, the output (B or A) of the flip-flop takes on the logic level set up at the input (A or B). The 'ABT32952 allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable inputs.

A buffered output-enable (OEAB or OEBA) input can be used to place the 32 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (OEAB or OEBA) does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (A to B). OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (B to A).

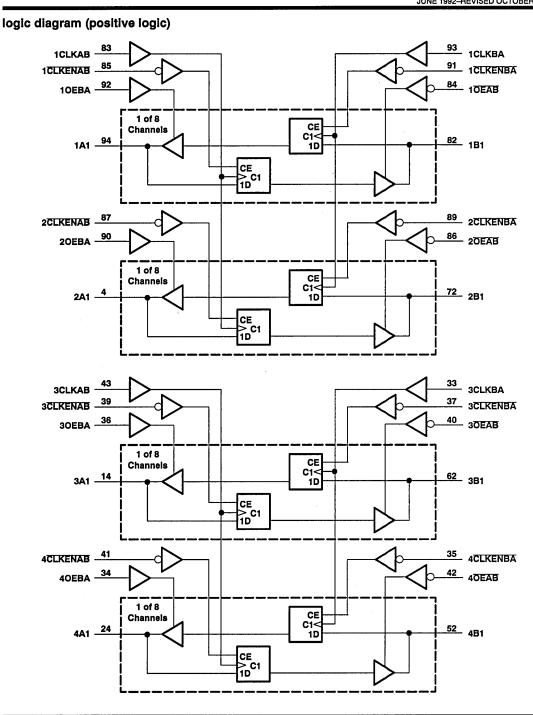
Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN54ABT32952 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT32952 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE† (each flip-flop)

	OUTPUT			
CLKENAB	OEAB	CLKAB	Α	В
L	L	1	Н	Н
L	L	<b>†</b>	L	L
н	L	X	Х	Qo
X	L	L	Х	$Q_0$
Ιx	Н	Х	Х	z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, OEBA, and CLKBA.





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT32952	96 mA
SN74ABT32952	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Storage temperature range –	40°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

			SN54AB	T32952	SN74ABT32952			
1			MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage			5.5	4.5	5.5	٧	
V <sub>IH</sub>	High-level input voltage				2		V	
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V	
V <sub>I</sub>	Input voltage			Vcc	0	Vcc	٧	
Іон	High-level output current			-24		-32	mA	
lol	Low-level output current			48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	ç	



JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABT32952			SN74ABT32952				
		TEST CONDITIONS			MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},  I_1 = -18 \text{ mA}$					-1.2			-1.2	V	
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2.5			2.5			٧
					3			3			
					2						
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA						2			
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA				0.55			0.55	V	
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA									0.55
l <sub>i</sub>	Control inputs	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = V_{CC} \text{ or GI}$								±1	<del>1</del>
	A or B ports			J						±100	μΑ
I <sub>hold</sub>	A D	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 0.8 V					100			
	A or B ports	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V						-100			μΑ
l <sub>ozh</sub> ‡		$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$						-	50	μA	
l <sub>OZL</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-			-50	μΑ	
l <sub>OFF</sub>		$V_{CC} = 0$ , $V_I \text{ or } V_O \le 4.5 \text{ V}$							±100	μΑ	
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high						50	μΑ
10 <sup>§</sup>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V					-50	-100	-180	mA	
		V 55V		Outputs high						2	
lcc		$V_{CC} = 5.5 \text{ V},  I_{O} = 0, \\ V_{L} = V_{CC} \text{ or GND}$	Outputs low						5	mA	
		VI = VCC OF GIVE		Outputs disabled						0.5	
Δlcc	CLK pins	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		4 V,						1.5	mA
	Others									0.5	mA
Ci	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V									pF
Cio	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V									pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$ .

<sup>&</sup>lt;sup>‡</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

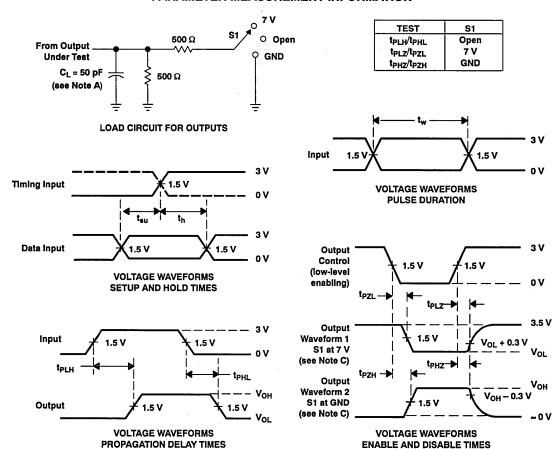
<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54ABT32952, SN74ABT32952 32-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_1 \leq 2.5 \text{ ns}$ ,  $t_1 \leq 2.5 \text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

	General Information	1
	ABT Octals	2
	ABT Widebus™	3
	ADI MUGDUS	
	ABT Widebus+™	4
	ABT Memory Drivers	 <b>5</b> ″
	ABT 25-Ω Incident-Wave Switching Drivers	6
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#### **ABT MEMORY DRIVERS**

#### **Features**

- Output ports have 25-Ω series resistors included on chip
- Octal, Widebus™, and Widebus+™ functional equivalents with complete pinout and package compatibility
- 8-, 9-, 10-, 11-, and 12-bit options
- 16-, 18-, 20-, 32-, and 36-bit options
- Typical V<sub>OLV</sub> (voltage output low-level valley)
   < 0.5 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Symmetrical, balanced output-drive capability of 12 mA

#### Benefits

- Reduce component count and save valuable board space
- Drop-in replaceable series resistor options with characteristic ABT advanced system performance and minimal system power
- Reliably drive address lines of 64K, 256K, 1M, 4M, and 16M MOS dynamic random access memories (DRAMs)
- Highly integrated, undershoot-dampened line drivers for advanced lump load transmission conditions
- Reduced output undershoot experienced at the receiver input for increased system reliability
- Equivalent output high and low current levels optimally drive highly capacitive inputs

The following table lists ABT memory driver devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the General Purpose Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT2540	20	Octal Memory Driver
'ABT2541	20	Octal Memory Driver
'ABT2620	20	Octal Memory Driver
'ABT2623	20	Octal Memory Driver
'ABT2640	20	Octal Memory Driver
'ABT2827	24	10-Bit Inverting Memory Driver
'ABT2828	24	10-Bit Noninverting Memory Driver
'ABT2863	24	9-Bit Memory Driver
'ABT5410	24	12-Bit Memory Driver
'ABT5411	24	12-Bit Memory Driver
'ABT5412	24	12-Bit Memory Driver
'ABT5413	24	12-Bit Memory Driver
'ABT162241	48	Noninverting 16-Bit Buffer/Driver With Series Output Resistors
'ABT162540	48	Inverting 16-Bit Buffer/Driver With Series Output Resistors
'ABT162541	48	Noninverting 16-Bit Buffer/Driver With Series Output Resistors
'ABT162825	56	Noninverting 18-Bit Buffer/Driver With Series Output Resistors
'ABT162826	56	Inverting 18-Bit Buffer/Driver With Series Output Resistors
'ABT162827	56	Noninverting 20-Bit Buffer/Driver With Series Output Resistors
'ABT162828	56	Inverting 20-Bit Buffer/Driver With Series Output Resistors
'ABT162861	56	Noninverting 20-Bit Transceiver With Series Output Resistors
'ABT162862	56	Inverting 20-Bit Transceiver With Series Output Resistors
'ABT162863	56	Noninverting 18-Bit Transceiver With Series Output Resistors
'ABT162864	56	Inverting 18-Bit Transceiver With Series Output Resistors
'ABT322245	100	36-Bit Bus Transceiver With Series Output Resistors
'ABT322316	80	16-Bit Tri-Port Universal Bus Exchanger With Series Output Resistors
'ABT322318	80	18-Bit Tri-Port Universal Bus Exchanger With Series Output Resistors
'ABT322319	80	18-Bit Tri-Port Universal Bus Exchanger With Clock Enable and Series Output Resistors
'ABT322373	100	32-Bit Transceiver With D-Type Latches and Series Output Resistors
'ABT322374	100	32-Bit Registered Transceiver With Series Output Resistors
'ABT322500	100	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322501	100	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322543	100	36-Bit Registered Bus Transceiver With Series Output Resistors
'ABT322600	100	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322601	100	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322700	120	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322701	120	36-Bit Universal Bus Transceiver With Series Output Resistors
'ABT322900	120	36-Bit Transceiver With Parity Generate/Check and Series Output Resistors
'ABT322901	120	36-Bit Registered Bus Transceiver With Parity Generate/Check and Series Output Resistors
'ABT322952	120	32-Bit Registered Transceiver With Clock Enable and Series Output Resistors

. 5<del>-4</del> .

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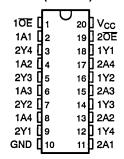
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art *EPIC-IIB* ™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

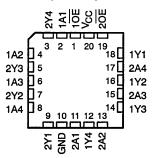
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2241 and 'ABT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary  $\overline{OE}$  and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

The 'ABT2240 is organized as two 4-bit line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

SN54ABT2240...J PACKAGE SN74ABT2240...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT2240 ... FK PACKAGE (TOP VIEW)



The outputs, which are designed to source or sink up to 12 mA, include  $25 - \Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor: the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2240 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2240 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT2240 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

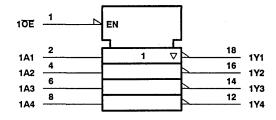
EPIC-IIB is a trademark of Texas Instruments Incorporated.

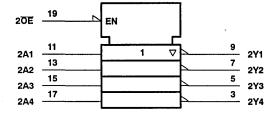
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## FUNCTION TABLE (each buffer)

INP	UTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	Н
н	X	Z

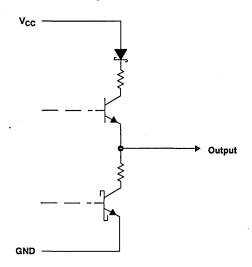
## logic symbol†



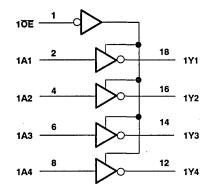


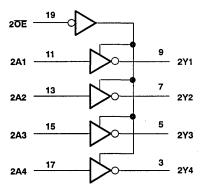
<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematic of Y outputs



## logic diagram (positive logic)





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>1</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT2240	96 mA
SN74ABT2240	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	0.85 W
N package	1.3 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

			SN54AB	T2240	SN74ABT2240		UNIT
			MIN	MAX	MIN	MAX	ONII
Vcc	Supply voltage		4.5	5,5	4.5	5.5	٧
ViH	High-level input voltage	2	¥,	2		٧	
VIL	Low-level input voltage			<i>€</i> 0.8		0.8	٧
VI	Input voltage		0,4		0	Vcc	٧
I <sub>OH</sub>	High-level output current		\$	-24		-32	mA
loL	Low-level output current		S	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	1,80	5		5	ns/V
T <sub>A</sub>	Operating free-air temperature		~-55	125	-40	85	ပံ့

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T	A = 25°C	:	SN54AB	T2240	SN74ABT2240		UNIT
PAHAMETER				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> =18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	Α	2			2				·
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 m/	4	2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA				0.8		0.8		0.8	٧
l <sub>i</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or C	V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	V <sub>O</sub> = 2.7 V			50		₹50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	V <sub>O</sub> = 0.5 V			-50	50			-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.9$	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100	Si		±100		μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	A.	50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 \text{ V}$		-50	-100	-180	-60	-180	-50	-180	mA
	V 55V		Outputs high		1	250	ري _	250	l	250	μА
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0,$	Outputs low		24	30	Q"	30		30	mA
	11-10001010		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data	Outputs enabled		-	1.5		1.5		1.5	
ΔI <sub>CC</sub> #	One input at 3.4 V, Other inputs at	· Imputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control input	s			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,			8.5						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			T2240	SN74ABT2240		UNIT
	(	(00.1.0.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	l i
t <sub>PLH</sub>	Α			3	4	1 🔏	5	1	4.9	ns
t <sub>PHL</sub>		'	3	4.8	5.8	3.0	6.1	3	6	115
t <sub>PZH</sub>	ŌĒ		1.5	3.7	4.7	1.5	∜ 6.1	1.5	5.8	ns
t <sub>PZL</sub>	OE		4.2	6.5	7.6	4:2	8.6	4.2	8.4	115
t <sub>PHZ</sub>	ŌE		1.9	3.8	5	1.9	5.7	1.9	5.6	ns
t <sub>PLZ</sub>		<u>L</u>	2.5	4.7	5.8	2.5	6.9	2.5	6.4	113

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

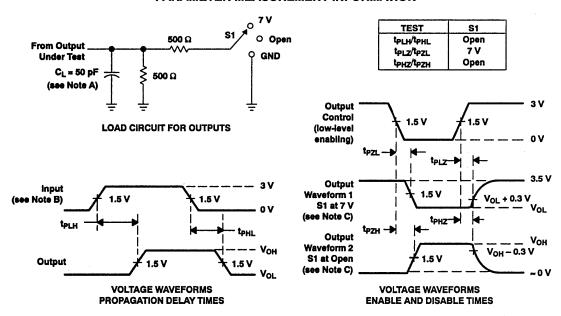
 $<sup>\</sup>S$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

D3697, JANUARY 1991-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

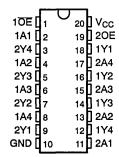
JANUARY 1991-REVISED OCTOBER 1992

- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

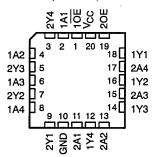
#### description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2240 and 'ABT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary  $\overline{OE}$  and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

SN54ABT2241 . . . J PACKAGE SN74ABT2241 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT2241 ... FK PACKAGE (TOP VIEW)



The outputs, which are designed to source or sink up to  $12 \, \text{mA}$ , include  $25 - \Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.  $\overline{OE}$  should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT2241 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2241 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT2241 is characterized for operation from -40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



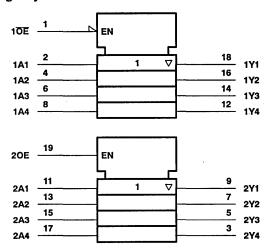
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#### **FUNCTION TABLES**

INP	JTS	OUTPUT
10E	1A	1Y
L	Н	Н
L	L	L
н	X	z

INP	UTS	OUTPUT
20E	2A	2Y
Н	Н	Н
н	L	L
L	X	z

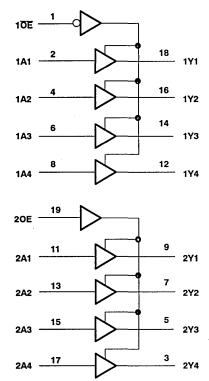
## logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

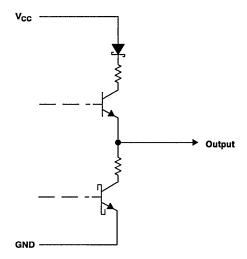
Pin numbers shown are for DW, J, and N packages.

## logic diagram (positive logic)



JANUARY 1991-REVISED OCTOBER 1992

## schematic of Y outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub>	. −0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT2241	96 mA
SN74ABT2241	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	0.85 W
N package	1,3 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AE	T2241	SN74AB	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current		1	12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



JANUARY 1991-REVISED OCTOBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54AE	T2241	SN74ABT2241		
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> =3 mA		2.5			2.5	_	2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	4	2			2				V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 m/	4	2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA				0.8		0.8		0.8	٧
l l <sub>i</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or C			±1		±1		±1	μΑ	
l <sub>ozh</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	V <sub>O</sub> = 2.7 V			50		50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50		-50		-50	μΑ	
loff	V <sub>CC</sub> = 0 V,	$V_I$ or $V_O \le 4.5$	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V		Outputs high		1	250		250		250	μΑ
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0,$	Outputs low		24	30		30		30	mA
	11-10001010		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data	Outputs enabled			1.5		1.5	Ĭ	1.5	
Δl <sub>CC</sub> #	One input at 3.4 V, Other inputs at		Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND Control inp		S			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,			8						рF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

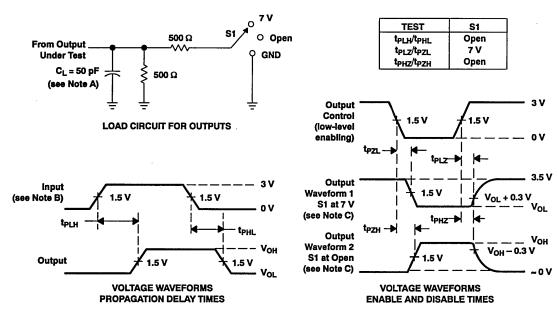
<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_t \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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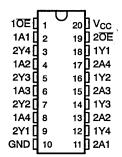
- **Space-Saving Package Option:** Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- **Package Options Include Plastic** Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

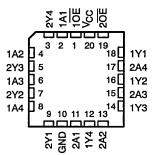
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2240 and 'ABT2241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical OE (active-low output-enable) inputs, and complementary OE and OE inputs. These devices feature high fan-out and improved fan-in.

The outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

SN54ABT2244 . . . J PACKAGE SN74ABT2244...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT2244 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT2244 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE** (each buffer)

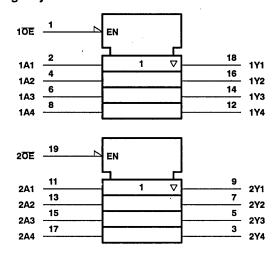
INPL	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X	z

EPIC-IIB is a trademark of Texas Instruments Incorporated.



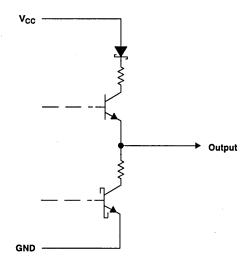
## SN54ABT2244, SN74ABT2244 OCTAL BUFFÉRS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS SCBS106A-D3710, JANUARY 1991-REVISED OCTOBER 1992

## logic symbol†

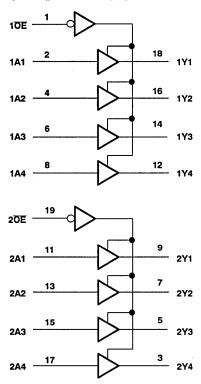


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### schematic of Y outputs



## logic diagram (positive logic)





## SN54ABT2244, SN74ABT2244 **OCTAL BUFFERS AND LINE/MOS DRIVERS** WITH 3-STATE OUTPUTS SCBS106A-D3710, JANUARY 1991-REVISED OCTOBER 1992

bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>
Current into any output in the low state, Io: SN54ABT2244
SN74ABT2244
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, $I_{OK}(V_O < 0)$
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package
DW package 0.85 W
N package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 2)

			SN54ABT2244		SN74ABT2244		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5,5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2	,35	2		V
VIL	Low-level input voltage		Τ,	<i>&amp;</i> ₹ 0.8		0.8	V
VI	Input voltage		0,	Vcc	0	Vcc	V
Іон	High-level output current		3	-24		-32	mA
loL	Low-level output current		े	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	85	5		5	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			A = 25°C	;	SN54AB	T2244	SN74ABT2244		UNIT	
PARAMETER	l le:				TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	וואט	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V	
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5				
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		l v l	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m/	A	2			2				V	
	V <sub>CC</sub> = 4.5 V,	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA							2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA				0.8		0.8		0.8	٧	
11	V <sub>CC</sub> = 5.5 V,	5 V, $V_I = V_{CC}$ or GND				±1		±1		±1	μΑ	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	•	∂50		50	μА	
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		<i>5</i> 0 €	i	-50	μΑ	
loff	V <sub>CC</sub> = 0 V,	$V_{\rm I}$ or $V_{\rm O} \le 4.5$	5 V			±100	S.F.		±100		μΑ	
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	. A	50		50	μΑ	
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-60	-180	50	-180	mA	
	V 55V		Outputs high		1	250	,Ö'	250		250	μΑ	
lcc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$ ,	Outputs low		24	30	4"	30		30	mA	
	11 - 100 01 GILD		Outputs disabled		0.5	250		250		250	μА	
	V <sub>CC</sub> = 5.5 V,	Data	Outputs enabled			1.5		1.5		1.5		
Δl <sub>CC</sub> #	V, Other inputs at	One input at 3.4 inputs	inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control input	S			1.5		1.5		1.5		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			3						pF		
Co	V <sub>O</sub> = 2.5 V or 0.5 V				8.5						pF	

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>4</sub> = 25°C		SN54ABT22	14	SN74AB	T2244	UNIT
	( 0.)	(55.1.5.)	MIN	TYP	MAX	MIN MA	١X	MIN	MAX	
t <sub>PLH</sub>	^		1	3.4	4.3	1 4	8.4	1	4.7	ns
t <sub>PHL</sub>	Α	'	1	4.5	5.3	1,\$2 ,\2\1	5.7	1	5.6	115
<sup>t</sup> PZH	ŌĒ		1.1	3.8	4.8	4.3 63.	5.7	1.1	5.5	ns
t <sub>PZL</sub>	OE .	1	2.1	6.3	7.3	2.1% 8	3.4	2.1	8.3	115
t <sub>PHZ</sub>	ŌĒ	~	2.1	4.5	5.6		3.7	2.1	6.6	ns
t <sub>PLZ</sub>	06	,	1.7	4.3	5.3	1.7	3.1	1.7	5.8	113

 $<sup>^\</sup>dagger$  All typical values are at V<sub>CC</sub> = 5 V.  $^\ddagger$  On products compliant to MIL-STD-883, Class B, this parameter does not apply.

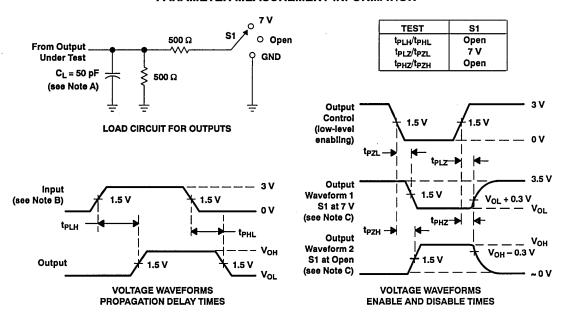
<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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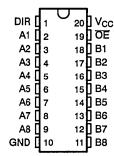
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

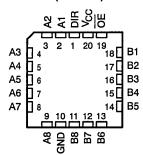
These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

The outputs, which are designed to source or sink up to 12 mA, include  $25-\Omega$  series resistors to reduce overshoot and undershoot.

SN54ABT2245...J PACKAGE SN74ABT2245...DB, DW, OR N PACKAGE (TOP VIEW)



SN54ABT2245 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2245 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2245 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

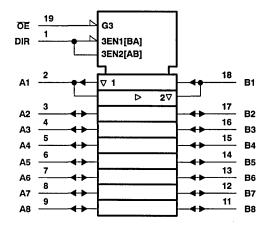
INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	н	A data to B bus				
н	Х	Isolation				

EPIC-IIB is a trademark of Texas Instruments Incorporated.

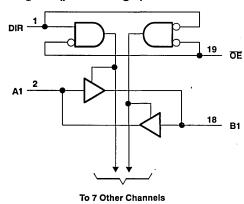


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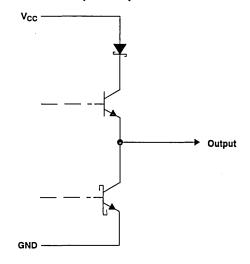
## logic symbol†



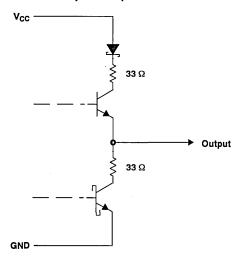
## logic diagram (positive logic)



#### schematic of A-port outputs



### schematic of B-port outputs



All resistor values shown are nominal.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage range, V <sub>CC</sub> –0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub> –0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT2245
<b>SN74ABT2245</b>
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)

#### NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AE	3T2245	SN74AE	UNIT	
İ			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage				2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate Outputs enabled			5		5	ns/V
T <sub>A</sub>	Operating free-air temperature	perating free-air temperature		125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS SEPTEMBER 1992-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		OT COMPLETO	NO	T	A = 25°0	2	SN54AE	T2245	SN74ABT2245		
PARAMETER	""	TEST CONDITIONS				MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	1 <sub>OH</sub> = -24 m/	4	2			2				V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 m/	4	2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA				8.0		0.8		0.8	٧
ı	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
l <sub>l</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V					50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V					-50		-50		-50	μА
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		- 50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
-	V <sub>CC</sub> = 5.5 V,		Outputs high		1	250		250		250	μА
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		24	30		30		30	mA
	$V_i = V_{CC}$ or GND		Outputs disabled		0.5	250		250		250	μΑ
	V <sub>CC</sub> = 5.5 V,	Data	Outputs enabled			1.5		1.5		1.5	
ΔI <sub>CC</sub> #	One input at 3.4 V, Other inputs at	Outputs disabled			0.05		0.05		0.05	mA	
	V <sub>CC</sub> or GND	Control input	Control inputs			1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V										pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	/									pF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

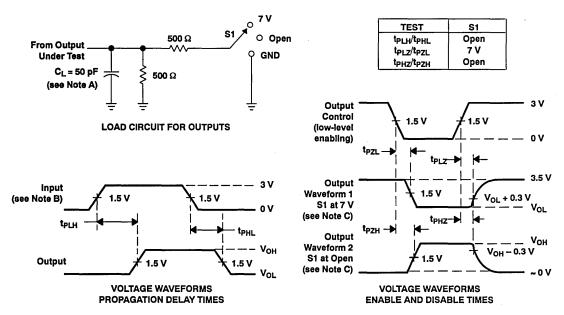
<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SEPTEMBER 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{<}$  10 MHz,  $Z_{o}$  = 50  $\Omega$ ,  $t_{f}$   $_{<}$  2.5 ns,  $t_{f}$   $_{<}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT5400, SN74ABT5400 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS094A-D3962, DECEMBER 1991-REVISED OCTOBER 1992

- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Typical V<sub>OLV</sub> (Output Undershoot)
   < 0.5 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs

#### description

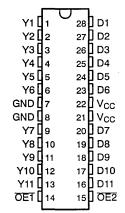
These 11-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all 11 outputs are in the high-impedance state.

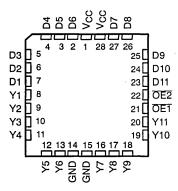
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5400 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT5400 is characterized for operation from –40°C to 85°C.

SN54ABT5400 ... JT PACKAGE SN74ABT5400 ... DW PACKAGE (TOP VIEW)



SN54ABT5400 . . . FK PACKAGE (TOP VIEW)



#### **FUNCTION TABLE**

	INPUTS	OUTPUT	
OE1	OE2	D	Υ
L	L	L	L
L	L	Н	Н
н	X	Х	z
X	Н	Х	Z

EPIC-IIB is a trademark of Texas Instruments Incorporated.

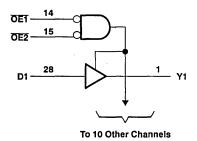
## SN54ABT5400, SN74ABT5400 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS094A-D3962 DECEMBER 1991-REVISED OCTOBER 1992

## logic symbol†

#### & 14 EΝ 15 OE2 28 D1 **Y**1 2 27 Y2 D2 3 26 D3 **Y3** 25 4 **Y4** D4 24 5 D5 **Y**5 6 23 D6 **Y6** 20 9 D7 **Y7** 19 10 D8 **Y8** 18 11 D9 **Y9** 17 12 D10 Y10 16 13 D11 Y11

### logic diagram (positive logic)



Pin numbers shown are for DW and JT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	. $-0.5 \text{ V}$ to $5.5 \text{ V}$
Current into any output in the low state, Io	60 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1.2 W
Storage temperature range	65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### recommended operating conditions (see Note 2)

			SN54AE	3T5400	SN74AB	UNIT	
			MIN	MAX	MIN	MAX	וואט
Vcc	Supply voltage		4.5	5,5	4.5	5.5	V
VIH	High-level input voltage		2	Ų,	2		V
VIL	Low-level input voltage			<i>€</i> 0.8		0.8	V
V <sub>I</sub>	Input voltage		0.4	₹ V <sub>CC</sub>	0	Vcc	V
ЮН	High-level output current		ن.	-12		-12	mA
loL	Low-level output current		್ರ	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	18	10	1	10	ns/V
TA	Operating free-air temperature		₹-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T	A = 25°C	<u> </u>	SN54ABT5400		SN74ABT5400		UNIT
PARAMEIER	! "°	SI CONDITIO	13	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2	-	-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA			3.35	3.7		3.3		3.35		
V <sub>OH</sub>	V <sub>CC</sub> = 5 V,	/ <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA			4.2		3.8		3.85		l v
▼он	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$					3		3.1		]
	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -12 mÅ							2.6		
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 8 \text{ mA}$							0.8		0.65	٧
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA								0.8	
l <sub>1</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or G	ND			±1		<b>(4</b> ,		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		\$50		50	μA
lozL	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50		<b>€</b> 4–50		-50	μA
loff	V <sub>CC</sub> = 0 V,	$V_I \text{ or } V_O \le 4.5$	٧			±100	, A			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Š	50		50	μΑ
lo	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-25	-45	-100	<b>-3</b> 5	-100	-25	-100	mA
los‡	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0		-50	_	-200	<i>&amp;</i> ⊆50	-200	-50	-200	mA
	V 55V		Outputs high		5	50		50		50	μA
Icc	$V_{CC} = 5.5 \text{ V},$ $V_i = V_{CC} \text{ or GND}$	l <sub>O</sub> = 0,	Outputs low		36	45	I	45		45	mA
	1 - 4CC of CIAB		Outputs disabled		1	50		50		50	μА
	V <sub>CC</sub> = 5.5 V,	Data inputa	Outputs enabled			1.5		1.5		1.5	
ΔI <sub>CC</sub> §	One input at 3.4 V. Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND Control inputs					1.5		1.5		1.5	
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$				8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>\*</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

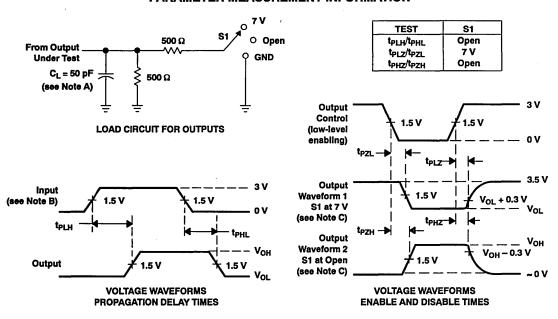
<sup>&</sup>lt;sup>5</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS094A-D3962, DECEMBER 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54ABT5400		SN74ABT5400		UNIT
	(1111 01)	(0011-01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	2	4.5	5.7	2	× 6.7	2	6.5	ns
t <sub>PHL</sub>			1.5	3.7	4.5	1.5	\$5.5	1.5	5.2	
t <sub>PZH</sub>	QE	Y	2.5	5.7	6.6	£35%	8.6	2.5	8.5	ns
t <sub>PZL</sub>			2	4.4	5.5	495	6.9	2	6.8	
t <sub>PHZ</sub>	ŌĒ	Υ	1.5	3.6	4.4	1.5	5.5	1.5	5.2	
t <sub>PLZ</sub>	OE		1.5	4.2	5.4	1.5	7.4	1.5	6.9	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT5401, SN74ABT5401 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical Volp (Output Ground Bounce) < 1 V at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical V<sub>OLV</sub> (Output Undershoot) < 0.5 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- **Package Options Include Plastic** Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil **DIPs**

#### description

These 11-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all 11 outputs are in the high-impedance state. These devices provide inverted data.

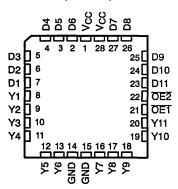
To ensure the high-impedance state during power up or power down, OE should be tied to Vcc. through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5401 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT5401 is characterized for operation from -40°C to 85°C.

SN54ABT5401 ... JT PACKAGE SN74ABT5401 . . . DW PACKAGE (TOP VIEW)

Y1 [	1	28	D1
Y2		27	D2
Y3 [		26	D3
Y4 [			D4
Y5 [		24	D5
Y6 [			D6
GND [		22	] v <sub>cc</sub>
GND [		21	$1_{\rm V_{CC}}$
Y7 [		20	D7
Y8 [		19	BG [
Y9 [		18	D9
Y10		17	D10
Y11 [	13	16	D11
OE1	14	15	OE2

SN54ABT5401 ... FK PACKAGE (TOP VIEW)



#### **FUNCTION TABLE**

	INPUTS		OUTPUT
OE1	OE2	D	] Y
L	L	L	Н
L	L	Н	L
н	X	X	z
×	н	_x	Z

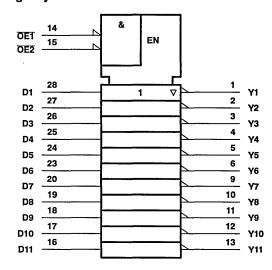
EPIC-IIB is a trademark of Texas Instruments Incorporated.

nation current as of publication date. Products conform to ne per the terms of Taxas Instruments standard warranty, processing does not necessarily include testing of all

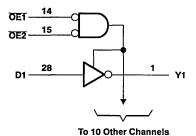
## SN54ABT5401, SN74ABT5401 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### logic symbol†



### logic diagram (positive logic)



Pin numbers shown are for DW and JT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub>	60 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1.2 W
Storage temperature range	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AE	T5401	SN74AE	UNIT	
			MIN	MAX	4.5 5 2 0 0 V <sub>C</sub>	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5,5	4.5	5.5	V
VIH	High-level input voltage		2	Ų,	2		V
V <sub>IL</sub>	Low-level input voltage			<i>€</i> 0.8		0.8	V
V <sub>I</sub>	Input voltage		0 4	₹ V <sub>CC</sub>	0	Vcc	V
Гон	High-level output current		1 6	-12	i	-12	mA
loL	Low-level output current		3	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TA	Operating free-air temperature		<sup>3</sup> -55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## SN54ABT5401, SN74ABT5401 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T	A = 25°C	;	SN54AE	3T5401	SN74ABT5401		Ī	
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V <sub>1</sub>	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA			3.35	3.7		3.3		3.35		V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA			3.85	4.2		3.8		3.85			
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$						3		3.1			
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -12 mA		2.6					2.6			
Var	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 8 mA						0.8		0.65	v	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA								0.8	١ ٧	
h	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or G	I = V <sub>CC</sub> or GND			±1		(A)		±1	μΑ	
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		- SEA		50	μΑ	
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	V <sub>O</sub> = 0.5 V			-50		2-50 2-50		-50	μΑ	
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_I$ or $V_O \le 4.5$	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100	_ ^			±100	μА	
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Š	50		50	μA	
lo	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-25	-45	-100	-₹35	-100	-25	-100	mA	
los‡	V <sub>CC</sub> ≈ 5.5 V,	V <sub>O</sub> = 0		-50		-200	& <sup>©</sup> 50	-200	-50	-200	mA	
	V <sub>CC</sub> = 5.5 V,		Outputs high		5	50		50		50	μΑ	
Icc	$V_{i} = V_{CC}$ or GND	$I_{O}=0,$	Outputs low		36	45		45		45	mA	
	ALE ACC OF GIAD		Outputs disabled		1	50		50		50	μА	
	V <sub>CC</sub> = 5.5 V,	B	Outputs enabled			1.5		1.5		1.5		
ΔI <sub>CC</sub> §	One input at 3.4 Data in	Data inputs	Outputs disabled			0.05		0.05		0.05	mA	
	V <sub>CC</sub> or GND Control inputs					1.5		1.5		1.5		
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						рF	
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	1			8						pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

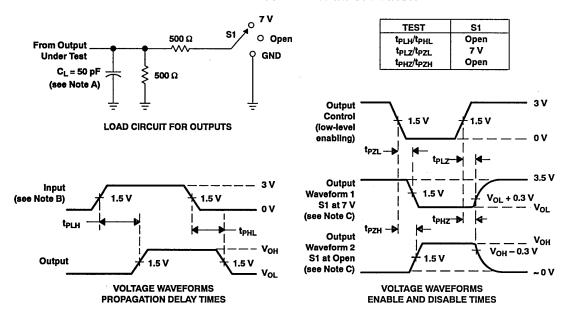
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			T5401	SN74ABT5401		UNIT
	(att O1)	(001101)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	2	4.5	6.1	2	7	2	6.9	ns
t <sub>PHL</sub>			1.5	4.4	5.2	1.5	<b>5.9</b>	1.5	5.7	
tpzH	OE	Y	2.5	5.7	6.6	2,5	8.6	2.5	8.5	- ns l
t <sub>PZL</sub>			2	4.4	5.5	V 22.	6.9	2	6.8	
t <sub>PHZ</sub>	OE .	ŌE Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	
tplZ	<u> </u>		1.5	4.2	5.4	1.5	7.4	1.5	6.9	ns

<sup>\*</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT5402, SN74ABT5402 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS100A-D3978, JANUARY 1992-REVISED OCTOBER 1992

- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Typical V<sub>OLV</sub> (Output Undershoot)
   < 0.5 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- $^{ullet}$  Output Ports Have 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs

#### description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all 12 outputs are in the high-impedance state.

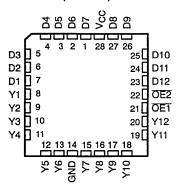
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5402 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT5402 is characterized for operation from –40°C to 85°C.

SN54ABT5402...JT PACKAGE SN74ABT5402...DW PACKAGE (TOP VIEW)

ا		
Y1 [		28 D1
Y2 [		27 D2
Y3 [		26 D3
Y4 [		25 D4
Y5 [		24 D5
Y6 [	6	23 🕽 D6
GND [	7	22 D7
Y7 [		21 VCC
Y8 [	9	20 D8
Y9 [	10	19 D9
Y10[	11	18 D10
Y11 [	12	17 D11
Y12 [	13	16 D12
OE1 [	14	15 OE2

SN54ABT5402 . . . FK PACKAGE (TOP VIEW)



#### **FUNCTION TABLE**

	INPUTS	OUTPUT	
OE1	OE2	D	Υ
L	L		L
L	L	Н	Н
н	Х	Χ	z
x	Н	X	z

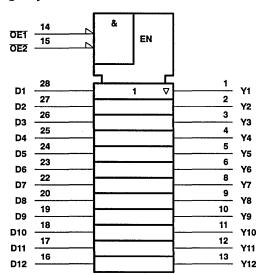
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Texas VI

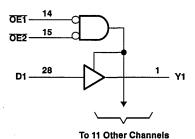
## SN54ABT5402, SN74ABT5402 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS100A-D3978, JANUARY 1992-REVISED OCTOBER 1992

#### logic symbol†



#### logic diagram (positive logic)



Pin numbers shown are for DW and JT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub>	60 mA
Input clamp current, I <sub>IK</sub> (V <sub>1</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1.2 W
Storage temperature range	65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### recommended operating conditions (see Note 2)

			SN54AE	T5402	SN74AB	UNIT	
l			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5,5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2	W	2		
VIL	Low-level input voltage			0.8 °Ç		0.8	٧
V <sub>I</sub>	Input voltage		0,4		0	Vcc	V
Гон	High-level output current		رن.	-12		-12	mA
loL	Low-level output current		S	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	3	10		10	ns/V
TA	Operating free-air temperature		~-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	75	TEST CONDITIONS			<sub>A</sub> = 25°C	;	SN54ABT5402		SN74ABT5402		TINU
PANAMEIEN	16	SI CONDITIO	No	MIN	TYP	MAX	MIN	MAX	MIN	MAX	וואט
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	<sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -1 mA		3.35	3.7		3.3		3.35		
V <sub>OH</sub>	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -1 mA		3.85	4.2		3.8		3.85		l <sub>v</sub>
V oH	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$					3		3.1		ľ
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$		2.6					2.6		
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 8 mA						0.8		0.65	v
VOL	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA								0.8	
!l	$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$ or G	ND			±1		,±3		±1	μΑ
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		₹50		50	μA
lozL	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V				-50		<b>⊘</b> ¥–50		-50	μΑ
OFF	V <sub>CC</sub> = 0 V,	$V_I$ or $V_O \le 4.5$	V .			±100	1 7	W.,		±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50	Š	50		50	μΑ
lo	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$		-25	-45	-100	₹25	-100	-25	-100	mA
los <sup>‡</sup>	$V_{CC} = 5.5 V$ ,	V <sub>O</sub> = 0		-50		-200	્વ <sup>⊆</sup> 50	-200	50	-200	mA
	V	10	Outputs high		5	50		50		50	μΑ
l <sub>CC</sub>	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$i_0 = 0$ ,	Outputs low		36	45		45		45	mA
	11 - 100 0. 0.12		Outputs disabled		1	50		50		50	μΑ
	V <sub>CC</sub> = 5.5 V,	Data innuta	Outputs enabled			1.5		1.5		1.5	
Δlcc <sup>§</sup>	One input at 3.4 V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$				8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>\*</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS100A-D3978, JANUARY 1992-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			T5402	SN74AE	UNIT	
	(INFO1)	(000.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	2	4.5	5.7	2 /	6.7	2	6.5	ns
t <sub>PHL</sub>			1.5	3.7	4.5	1.50	5.5	1.5	5.2	
t <sub>PZH</sub>	ŌE		2.5	5.7	6.6	23/2	8.6	2.5	8.5	
tpzL	OE .	1	2	4.4	5.5	Q.25	6.9	2	6.8	ns
t <sub>PHZ</sub>	ŌE		1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
tPLZ	OE .	T	1.5	4.2	5.4	1.5	7.4	1.5	6.9	113

#### PARAMETER MEASUREMENT INFORMATION 7 V TEST S1 O Open 500 Ω Open t<sub>PLH</sub>/t<sub>PHL</sub> From Output t<sub>PLZ</sub>/t<sub>PZL</sub> 7 V **Under Test** GND Open t<sub>PHZ</sub>/t<sub>PZH</sub> C<sub>L</sub> = 50 pF 500 Ω (see Note A) 3 V Output Control LOAD CIRCUIT FOR OUTPUTS (low-level enabling) 3.5 V Output Input Waveform 1 V<sub>OL</sub> + 0.3 V (see Note B) S1 at 7 V (see Note C) t<sub>PHZ</sub>-> Output Waveform 2 V<sub>OH</sub> -- 0.3 V S1 at Open Output 1.5 V (see Note C) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES**

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 ns$ ,  $t_f \leq 2.5 ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT5403, SN74ABT5403 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Typical V<sub>OLV</sub> (Output Undershoot)
   < 0.5 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs

#### description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OET or OE2) input is high, all 12 outputs are in the high-impedance state. These devices provide inverted data.

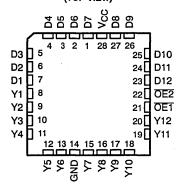
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5403 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT5403 is characterized for operation from -40°C to 85°C.

SN54ABT5403...JT PACKAGE SN74ABT5403...DW PACKAGE (TOP VIEW)

_	$\Box$	─L
Y1 [	1	28 D1
Y2[		27 D2
Y3[	3	26 D3
Y4[		25]] D4
Y5[	5	24 D5
Y6[		23 D6
GND[		22 D7
Y7[		21 V <sub>CC</sub>
Y8[		20 D8
Y9[		19 D9
Y10[		18 D10
Y11 [		17 D11
Y12[	13	16 D12
OE1 [	14	15 OE2

SN54ABT5403...FK PACKAGE (TOP VIEW)



#### **FUNCTION TABLE**

	INPUTS		OUTPUT
OET	OE2	D	Y
L	L	L	н
L	L	Н	L
н	X	X	z
X	н	X	z

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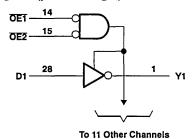
Texas VI

## SN54ABT5403, SN74ABT5403 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### logic symbol† 14 **OET** ΕN 15 OE2 28 1 D1 **Y1** 2 27 **Y2** D2 26 3 **Y3** 4 25 D4 **Y4** 24 5 **Y**5 D5 23 6 D6 **Y6** 22 8 D7 **Y7** 20 9 **D8** VR 19 10 D9 **Y9** 18 11 Y10 17 12 **D11** Y11 16 13 D12 Y12

### logic diagram (positive logic)



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW and JT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	−0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub>	60 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1.2 W
Storage temperature range	-65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54ABT540:		SN74AE	3T5403	11117
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5,5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage		2	49	2		٧
V <sub>IL</sub>	Low-level input voltage			<i>⊈</i> ; 0.8		0.8	V
Vı	Input voltage		0,4	V <sub>CC</sub>	0	Vcc	V
Гон	High-level output current		(ي.	-12		-12	mA
loL	Low-level output current		8	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	2	10		10	ns/V
TA	Operating free-air temperature		₹-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		CT OCNUTION	NO.	T	A = 25°C	;	SN54AE	3T5403	SN74ABT5403		UNIT
PARAMETER	"	ST CONDITIO	NS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>1</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -1 mA		3.35	3.7		3.3		3.35		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -1 mA		3.85	4.2		3.8		3.85		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$					3		3.1		ľ
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -12 mA		2.6					2.6		1
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 8 mA						0.8		0.65	V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA								0.8	\ \ \
l <sub>1</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or G	ND			±1		<b>(4</b> ,		±1	μА
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		<u>,</u> \$60		50	μА
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		<u>√</u> –50		-50	μΑ
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	V			±100				±100	μA
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Š	50		50	μA
lo	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$	-	-25	-45	-100	-25	-100	-25	-100	mA
los‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0		-50		-200	ర్డ≃50	-200	-50	-200	mA
	V 55V	1. 0	Outputs high		5	50		50		50	μΑ
Icc	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	l <sub>O</sub> = 0,	Outputs low		36	45		45		45	mΑ
	11-100 01 0115		Outputs disabled		1	50		50		50	μΑ
	V <sub>CC</sub> = 5.5 V,	Dota innuta	Outputs enabled			1.5		1.5		1.5	
ΔICC	One input at 3.4 Dat V, Other inputs at	Data inputs	Outputs disabled			0.05		0.05		0.05	mA
	V <sub>CC</sub> or GND	Control inputs				1.5		1.5		1.5	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V				3						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$				8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

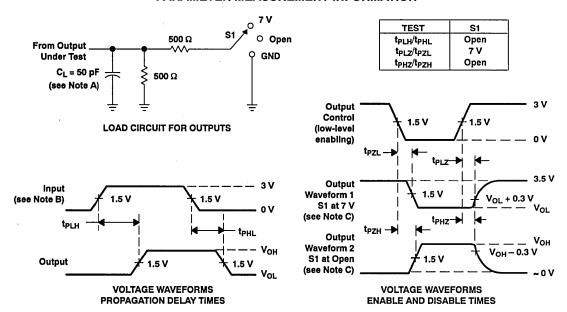
PARAMETER	FROM (INPUT)			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			3T5403	SN74AB	UNIT	
•	(11.1.01)	(65.1.6.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	D Y	2	4.5	6.1	2	7	2	6.9	ns
t <sub>PHL</sub>			1.5	4.4	5.2	1.5	5.9	1.5	5.7	
t <sub>PZH</sub>	ŌĒ	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	
t <sub>PZL</sub>	OE	1	2	4.4	5.5	₹ 2.	6.9	2	6.8	ns
t <sub>PHZ</sub>	ŌĒ		1.5	3.6	4.4	1.5	5.5	1.5	5.2	
tPLZ	)E	, T	1.5	4.2	5.4	1.5	7.4	1.5	6.9	ns

<sup>\*</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>\$</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT162240, SN74ABT162240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT162240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical  $\overline{OE}$  (active-low output-enable) inputs.

SN54ABT162240 ... WD PACKAGE SN74ABT162240 ... DL PACKAGE (TOP VIEW)

	_		_		
10E[	1	U	48	b	20E
1Y1[	2		47	1	1A1
1Y2[	3		46	1	1A2
GND[	4		45		GND
1Y3[	5		44		1A3
1Y4[	6		43		1A4
V <sub>CC</sub> [	7		42		$V_{CC}$
2Y1[	8		41	0	2A1
2Y2[	9		40	0	2A2
GND[	10		39	0	GND
2Y3[				_	2A3
2Y4[	12		37		2A4
3Y1[	13		36	0	3A1
3Y2[	14		35	0	3A2
GND[			34	1	GND
3Y3[	16		33	0	3A3
3Y4[	17			_	3A4
V <sub>CC</sub> [			31		$V_{CC}$
4Y1 [	19		30	0	4A1
4Y2	20		29	0	4A2
GND[				_	GND
4Y3[					4A3
4Y4[				_	4A4
40E[	24		25	1	30E
	_			ı	

The outputs, which are designed to sink up to 12 mA, include  $25-\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162240 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT162240 is characterized for operation from -40°C to 85°C.

# FUNCTION TABLE (each 4-bit buffer)

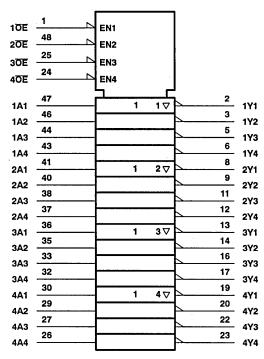
INP	UTS	OUTPUT
ŌĒ	Α	Y
L	Н	L
L	L	н
Н	X	Z

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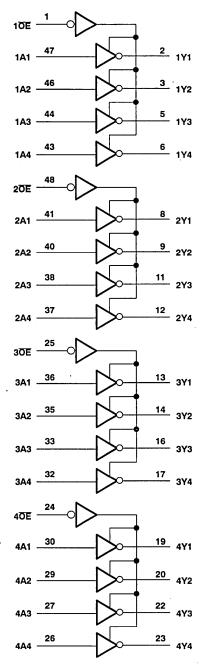
## SN54ABT162240, SN74ABT162240 **16-BIT BUFFERS/DRIVERS** WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

## logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)





## SN54ABT162240, SN74ABT162240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otnerwise note	ngs over operating free-air temperature range (unless otherwise noted)†
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Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	. $-0.5 V$ to $7 V$
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT162240	96 mA
SN74ABT162240	128 mA
Input clamp current, $I_{IK}(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air)	0.85 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

			SN54ABT	162240	SN74ABT162240		UNIT
	•		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10	-	10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# SN54ABT162240, SN74ABT162240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			NO.	T	<sub>A</sub> = 25°C	;	SN54ABT	162240	SN74ABT162240		UNIT
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
VIK	$V_{CC} = 4.5 \text{ V},$	/, I <sub>I</sub> = –18 mA				-1.2		-1.2		-1.2	٧
4	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 m.	A	2.5			2.5	_	2.5		
V <sub>OH</sub>	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = - 3 m.	A	3			3		3	1	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 mA		2			2				, v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 r	I <sub>OH</sub> = - 32 mA						2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA	l <sub>OL</sub> = 12 mA			8.0		0.8		8.0	٧
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1		±1	μА
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	V <sub>O</sub> = 0.5 V			-50		-50		-50	μА
I <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4$	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	I <sub>O</sub> = 0,	Outputs high			2		2		2	mA
Icc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	10 = 0,	Outputs low			32		32		32	
	11 - 100 01 0115	1 - 400 or GHD	Outputs disabled			2		2		2	
	V <sub>CC</sub> = 5.5 V, One	Data	Outputs enabled		-	1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at	inputs	Outputs disabled			0.05		1	İ	0.05	mA
	V <sub>CC</sub> or GND	•				1.5		1.5		1.5	1
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				7			_	ĺ		pF
Co	V <sub>O</sub> = 2.5 V or 0.5 \	/			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

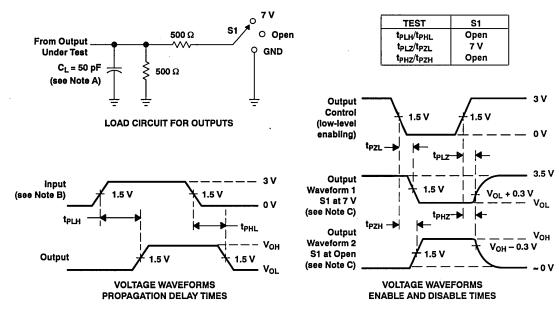
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54ABT162240, SN74ABT162240 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_f \leq 2.5 \ ns$ ,  $t_f \leq 2.5 \ ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The 'ABT162244 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides noninverting outputs and symmetrical OE (active-low output-enable) inputs.

SN54ABT162244... WD PACKAGE SN74ABT162244... DGG OR DL PACKAGE (TOP VIEW)

10E	1	U	48	2 <u>0E</u>
1Y1	2		47	1A1
1Y2	3			1A2
GND	4			GND
1Y3 🛚	5			1A3
1Y4 🛚	6		43	1A4
v <sub>cc</sub> [	7			Vcc
2Y1 [	8			5 2A1
2Y2 [	9		40	2A2
GND [			39	GND
2Y3 🛚			38	2A3
2Y4 [	12		37	2A4
3Y1 [			36	3A1
3Y2 [	14		35	3A2
GND [			34	GND
3Y3 🛚	16		33	3A3
3Y4 [	17		32	] 3A4
v <sub>cc</sub> [	18		31	Vcc
4Y1 [	19		30	4A1
4Y2 [	20		29	4A2
GND [	21		28	] GND
4Y3 [	22		27	] 4A3
4Y4 🛚	23		26	<b>4A4</b>
40E [	24		25	30E

The outputs, which are designed to sink up to 12 mA, include  $25-\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162244 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162244 is characterized for operation from –40°C to 85°C.

# FUNCTION TABLE (each 4-bit buffer)

INP	UTS	OUTPUT
ŌĔ	Α	Y
L	Н	Н
L	L	L
l H	Х	z

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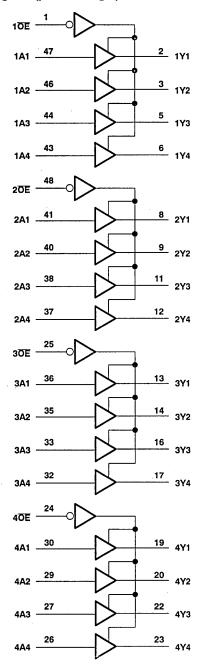
## SN54ABT162244, SN74ABT162244 **16-BIT BUFFERS/DRIVERS** WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

## logic symbol†

10E	1	EN1				
20E	48	EN2				
30E	25	EN3				
40E	24	EN4				
702		5		_ ,_	_	
1A1	47		1	1 ▽	2	1Y1
1A2	46				3	1Y2
1A3	44				5	1Y3
1A4	43				6	1Y4
2A1	41		1	2 ▽	8	2Y1
2A2	40				9	2Y2
2A3	38				11	2Y3
2A4	37	_			12	2Y4
3A1	36	<u> </u>	1	3 ▽	13	3Y1
3A2	35		•	Ť	14	3Y2
3A3	33	<u> </u>			16	3Y3
3A4	32				17	3Y4
4A1	30	<b>-</b>	1	4 ▽	19	4Y1
4A2	29	<b> </b>		-, v	.20	4Y2
4A2 4A3	27	<b>-</b>			22	412 4Y3
4A3 4A4	26	<b>—</b>			23	
444		L				4Y4

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)





## SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unl	ess otherwise noted)†
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· · · · · ·	<del>-</del> •
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or pow	rer-off state, V <sub>O</sub> 0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT1622	244 96 mA
SN74ABT1622	244 128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG	package 0.6 W
DL pa	ackage
Storage temperature range	

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

			SN54ABT	162244	SN74ABT	162244	LIMIT
1			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vi	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## SN54ABT162244, SN74ABT162244 **16-BIT BUFFERS/DRIVERS** WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT	162244	SN74ABT162244		
PARAMETER	'ES	I CONDITIO	ns ·	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 m.	A	2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	l <sub>OH</sub> = -3 m.	A	3			3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>OH</sub> = -24 r	nA	2			2		<u> </u>		
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 r	nA	2‡					2		l
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	$I_{OL} = 12 \text{ m/s}$	\			0.8		0.8		0.8	V
l;	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or	GND			±1		±1		±1	μА
lozH <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	<sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_{CC} = 0 \text{ V}, \qquad V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$				±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
10 <sup>¶</sup>	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V <sub>i</sub>	I <sub>O</sub> = 0,	Outputs high			2		2		2	
Icc	V <sub>I</sub> = V <sub>CC</sub> or GND	10 = 0,	Outputs low			32		32		32	mA
	11-1000 01 0115		Outputs disabled			2		2		2	1
	V <sub>CC</sub> = 5.5 V, One	Data	Outputs enabled			1		1.5		1	
Δl <sub>CC</sub> #	input at 3.4 V, Other inputs at		Outputs disabled			0.05		1		0.05	mA
	V <sub>CC</sub> or GND Control inputs				1.5		1.5		1.5	Ì	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V			7						pF	
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	,			7						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

The parameters IOZH and IOZL include the input leakage current.

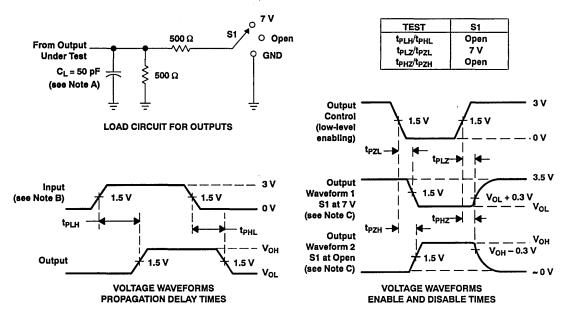
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## SN54ABT162260, SN74ABT162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

•	<b>Members of the Texas Instruments</b>	
	Widebus™ Family	

- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

The 'ABT162260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

SN54ABT162260 ... WD PACKAGE SN74ABT162260 ... DL PACKAGE (TOP VIEW)

			1
OEA [	1	$\bigcup_{56}$	OE2B
LE1B [	2	55	LEA2B
2B3 [		54	2B4
GND [	4		GND
2B2 [	5	52	2B5
2B1 [		51	] 2B6
Vcc [	7	50	]v <sub>cc</sub>
A1 [	8	49	] 2B7
A2 [	9	48	] 2B8
A3 [	10		] 2B9
GND [	11	46	] GND
A4 [	12	45	]2B10
A5 [	13		]2B11
A6 [	14		] 2B12
A7 [			] 1B12
A8 [			] 1B11
A9 [			] 1B10
GND [			] GND
A10 [			] 1B9
A11 [			] 1B8
A12 [	21	36	] 1B7
Vcc [	22	35	]v <sub>cc</sub>
	23	34	
1B2 [		33	] 1B5
GND [	25		] GND
1B3 [	26		] 1B4
LE2B [	27	30	
SEL [	28	29	DE1B

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. These control signals also allow byte control of the most significant byte and least significant byte for each bus.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B-port outputs, which are designed to sink up to 12 mA, include  $25-\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

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## SN54ABT162260, SN74ABT162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162260 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

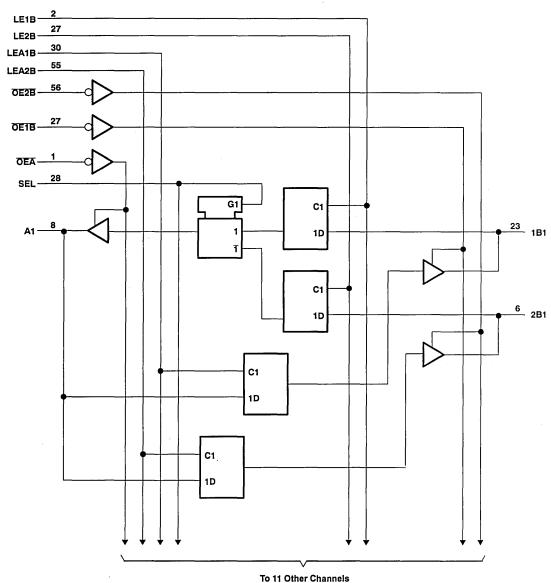
The SN54ABT162260 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT162260 is characterized for operation from  $-40^{\circ}$ C to 85°C.

#### **FUNCTION TABLES**

			OUTPUT				
	1B	2B	SEL	LE1B	LE2B	OEA	Α
Γ	Н	Х	Н	Н	X	L	Н
ı	L	X	Н	Н	X	L	L
ı	X	X	Н	L	X	L	A <sub>0</sub>
ı	Х	Н	L	X	н	L	н
1	X	L	L	X	Н	L	L
ı	X	X	L	X	L	L	A <sub>0</sub>
L	X	X	X	X	X	Н	z

		OUTI	PUTS			
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L	Н	н	L	L	L	L
н	Н	L	L	L	Н	2B <sub>0</sub>
L	Н	L	L	L	L	2B <sub>0</sub>
Н	L	н	L	L	1B <sub>0</sub>	Н.
L	L	н	L	L	1B <sub>0</sub>	L
×	L	L	L	L	1B <sub>0</sub>	2B <sub>0</sub>
×	Х	X	н	н	z	Z
x	X	X	L	н	Active	Z
×	х	X	н	L	z	Active
x	Х	Х	L	L	Active	Active

## logic diagram (positive logic)



## SN54ABT162260, SN74ABT162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

and and a series of the series	,
Supply voltage range, V <sub>CC</sub>	7 V
Input voltage range, V <sub>I</sub> (see Note 1)	7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	5.5 V
Current into any output in the low state, Io: SN54ABT162260	3 mA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

 Current into any output in the low state,  $I_O$ :
 SN54AB1162260
 96 mA

 SN74ABT162260
 128 mA

 Input clamp current,  $I_{IK}$  ( $V_I < 0$ )
 —18 mA

 Output clamp current,  $I_{OK}$  ( $V_O < 0$ )
 —50 mA

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

			SN54ABT	162260	SN74ABT	162260	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		· 2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
1	Low-level output current	A ports		48		64	mA
loL	Low-level output current	B ports		12		12	, '''^
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## SN54ABT162260, SN74ABT162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T	' <sub>A</sub> = 25°(	)	SN54ABT	162260	SN74ABT162260		UNIT
PARAMETER	lesi condini	ONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V},  I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	٧
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
\ <sub>V=</sub>	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -24 \text{ mA}$		2			2				ľ
	$V_{CC} = 4.5 \text{ V},  I_{OH} = -32 \text{ mA}$		2‡					2		l
	$V_{CC} = 4.5 \text{ V},  I_{OL} = 48 \text{ mA}$	A ports			0.55		0.55			
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V},  I_{OL} = 64 \text{ mA}$	Aports			0.55‡				0.55	٧
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 12 \text{ mA}$	B ports			0.8		0.8		8.0	
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	Control inputs			±1		±1		±1	μА
	V <sub>I</sub> = V <sub>CC</sub> or GND	A or B ports			±100		±100		±100	μ.
<b>.</b>	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.8 V	A or B ports						100		μА
hold	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2 V	A OI D POILS						-100		μΑ.
lozn§	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.7 \text{ V}$				50		50		50	μА
lozL <sup>§</sup>	$V_{CC} = 5.5 \text{ V},  V_{O} = 0.5 \text{ V}$				-50		-50		-50	μΑ
loff	$V_{CC} = 0 \text{ V},  V_{I} \text{ or } V_{O} \le 4.5$	V			±100				±100	μА
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
10 <sup>¶</sup>	$V_{CC} = 5.5 \text{ V},  V_{O} = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	V 55V 1 0	Outputs high							3	
Icc	$V_{CC} = 5.5 \text{ V},  I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low							60	mA
	ALT ACC OF CIVE	Outputs disabled							2	i I
Δlcc#	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND				1		1.5		1	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V									pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V									рF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup>This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

## SN54ABT162260, SN74ABT162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

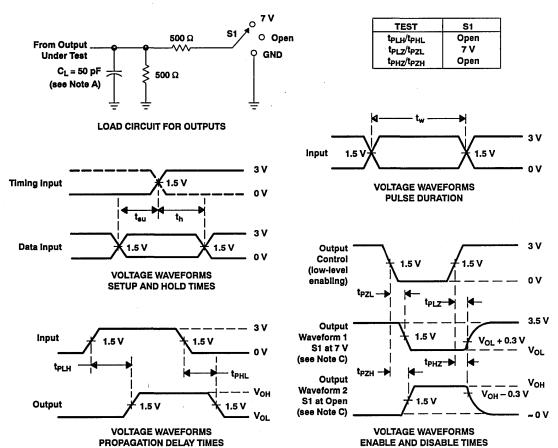
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT162260		SN74ABT162260		UNIT	
	( 0.)	(333.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	Α	В							5	ns	
t <sub>PHL</sub>		P P							5.5	115	
t <sub>PLH</sub>	В	Α							5	ns	
t <sub>PHL</sub>									5	115	
t <sub>PLH</sub>	LE.	A or B							5	ns	
t <sub>PHL</sub>										5	115
t <sub>PLH</sub>	SEL	Α							5		
t <sub>PHL</sub>	SEL	1 ^							5	ns	
t <sub>PZH</sub>	ŌĒ	A or B							5.5		
t <sub>PZL</sub>	OE .	_ AOIB							6	ns	
t <sub>PHZ</sub>	ŌE	A or B							5,5		
t <sub>PLZ</sub>	\ \begin{align*}	Aorb							5.5	ns	



## SN54ABT162260, SN74ABT162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- B-Port Outputs Have Equivalent 25-Ω
   Series Resistors, So No External Resistors
   Are Required
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

SN54ABT162500...WD PACKAGE SN74ABT162500...DL PACKAGE (TOP VIEW)

ОЕАВП	1	56	GND
LEAB	2	55	CLKAB
A1[	3	54	B1
GND	4	53	GND
A2[	5	52	] B2
A3[	6	51	] B3
Vcc[	7	50	] v <sub>cc</sub>
A4[	8	49	] B4
A5[]	9	48	] B5 .
A6[	10	47	] B6
GND[]	11	46	GND
A7[]	12	45	] B7
]8A	13	44	] B8
A9[]	14	43	] B9
A10[	15	42	] B10
A11	16	41	] B11
=	17	40	
GND	18		] GND
A13[]	19	38	[] B13
A14	20	37	] B14
A15[]	21	36	] B15
VccL	22	35	□ v <sub>cc</sub>
A16	23	34	_
A17	24		E
GND	25	32	] GND
A18	26	•	B18
OEBAI	27		] CLKBA
LEBA[]	28	29	GND

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

The B-port outputs, which are designed to sink up to 12 mA, include 25- $\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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#### description (continued)

The SN74ABT162500 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162500 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT162500 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

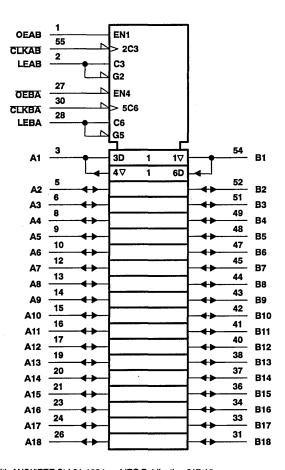
	INPUTS					
OEAB	LEAB	CLKAB	Α	В		
L	Х	Х	X	Z		
н	Н	X	L	L		
н	н	X	н	н		
H.	L	<b>↓</b>	L	L		
н	L	1	н	н		
Н	L	н	X	B₀‡		
Н	L	L	X	B <sub>0</sub> ‡ B <sub>0</sub> §		

<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

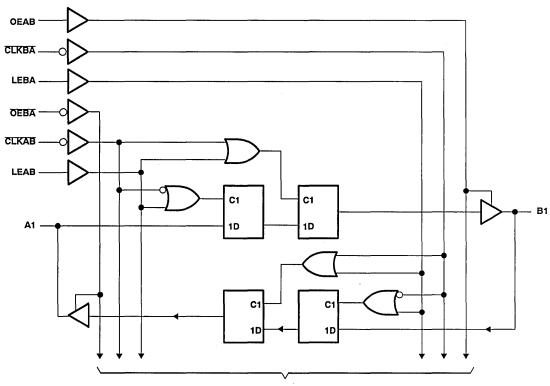
## logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## SN54ABT162500, SN74ABT162500 **18-BIT UNIVERSÁL BUS TRANSCEIVERS** WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### logic diagram (positive logic)



To 17 Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		
Input voltage range, V <sub>I</sub> (except I/O ports) (s		
Voltage range applied to any output in the	high state or power-off state, \	<b>/</b> <sub>O</sub> −0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT162500	96 mA
	SN74ABT162500	128 mA
Input clamp current, $I_{ K }(V_{ I } < 0)$		–18 mA
Output clamp current, IOK (VO < 0)		
Maximum power dissipation at T <sub>A</sub> = 55°C (		
Storage temperature range		

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



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## recommended operating conditions (see Note 2)

			SN54AB7	162500	SN74ABT162500		UNIT
l			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage	-	0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
l <sub>OL</sub>	Low lovel autout aurent	A ports		48		64	^
	Low-level output current	B ports		12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	40	85	ç

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT	162500	SN74ABT162500		
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	$I_{I} = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5			2.5		2.5		
, i	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2				l
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA			2‡					2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			
$V_{OL}$	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA	A ports			0.55‡				0.55	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA	B ports					0.8		0.8	1
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
l <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND				±100		±100		±100	μΑ	
l <sub>OZH</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$					50	```	50		50	μА
I <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$					-50		-50		-50	μΑ
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V},  V_1 \text{ or } V_0 \le 4.5 \text{ V}$					±100				±100	μА
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mΑ
	V <sub>CC</sub> = 5.5 V,	T	Outputs high			3		3		3	
lcc	I <sub>O</sub> = 0,	A or B ports	Outputs low			76		76		34	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	ports	Outputs disabled			3.3		3.3		3.3	1
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs			4						pF	
Cio	V <sub>O</sub> = 2.5 V or 0.5 V A or B ports			8						pF	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

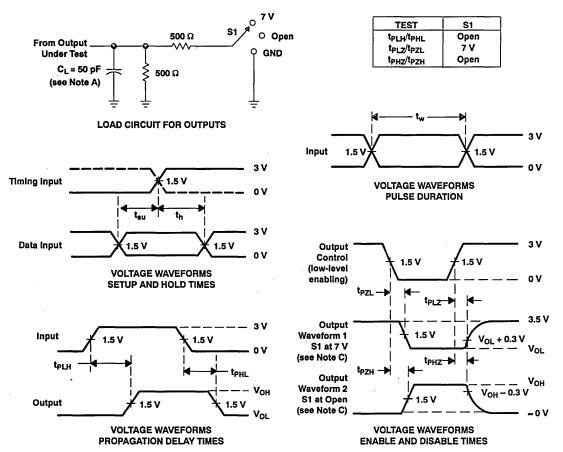
				SN54ABT	162500	SN74ABT162500		
				MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
t <sub>w</sub>	Pulse duration	LEAB or LEBA high						
		CLKAB or CLKBA high or low	1				ns	
t <sub>su</sub>	Setup time	A before CLKAB↓						
		B before CLKBA↓						
		A before LEAB tor B before LEBA	CLK high					ns
			CLK low	1				
t <sub>h</sub>	Hold time	A after CLKAB‡ or B after CLKBA‡		1				
		A after LEAB or B after LEBA						ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT162500		SN74ABT162500		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	l
f <sub>max</sub>			150	200		150		150		MHz
t <sub>PLH</sub>	A or B	B or A								ns
t <sub>PHL</sub>	1 100									115
t <sub>PLH</sub>	LEAB or LEBA	B or A								ns
t <sub>PHL</sub>										115
t <sub>PLH</sub>	CLKAB or CLKBA	B or A								
t <sub>PHL</sub>	CLINAB OF CLINBA									ns
tpzH	OEAB or OEBA	B or A								
t <sub>PZL</sub>	OEAB OF CEBA									ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A								
tpLZ	1 DEAD OF DEBA									ns

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_t \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- B-Port Outputs Have Equivalent 25-Ω
   Series Resistors, So No External Resistors
   Are Required
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

SN54ABT162501 ... WD PACKAGE SN74ABT162501 ... DL PACKAGE (TOP VIEW)

			_	
OEAB (	1	U	56	GND
LEAB [	2		55	CLKAB
A1 [	3		54	] B1
GND [	4		53	] GND
A2 [			52	] B2
А3 [				] B3
V <sub>CC</sub>			50	] v <sub>cc</sub>
A4 [				] B4
A5 [				] B5
A6 [				] B6
GND [				] GND
A7 [				] B7
A8 [				] B8
A9 [				] B9
A10				B10
A11				] B11
A12				B12
GND				GND
A13				] B13
A14				B14
A15				B15
V <sub>CC</sub>				] v <sub>cc</sub>
A16				B16
A17				B17
GND				GND
A18			31	B18
OEBA [	3			CLKBA
LEBA [	28		29	] GND

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

The B-port outputs, which are designed to sink up to 12 mA, include 25- $\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT162501 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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SEPTEMBER 1992-REVISED OCTOBER 1992

#### description (continued)

The SN54ABT162501 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT162501 is characterized for operation from -40°C to 85°C.

**FUNCTION TABLE<sup>†</sup>** 

	INPUTS						
OEAB	LEAB	CLKAB	В				
L	Х	Х	X	Z.			
н	Н	X	L	L			
н	Н	X	н	н			
н	L	†	L	L.			
н	L	t	Н	н			
н	L	н	X	B₀ <sup>‡</sup> B₀ <sup>§</sup>			
н	L.	L	_X	B <sub>0</sub> ⁵			

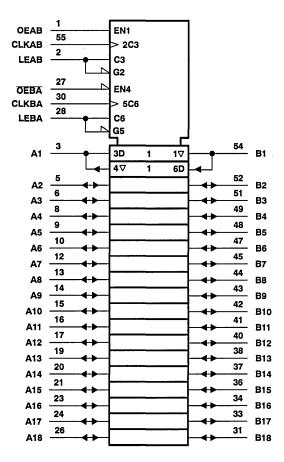
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

# SN54ABT162501, SN74ABT162501 **18-BIT UNIVERSAL BUŚ TRANSCEIVERS** WITH 3-STATE OUTPUTS SEPTEMBER 1992-REVISED OCTOBER 1992

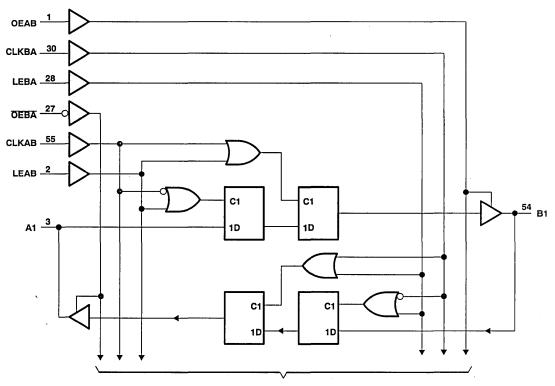
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SEPTEMBER 1992-REVISED OCTOBER 1992

#### logic diagram (positive logic)



To 17 Other Channels

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT162501	96 mA
SN74ABT162501	128 mA
input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	1 W
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



SEPTEMBER 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54ABT	162501	SN74ABT	162501	UNIT
			MIN	MAX	MIN	MAX	INI
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage	ĺ	0.8		0.8	V	
VI	Input voltage			Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
,	Low-level output current	A ports		48		64	mA
lor	Low-level output current	B ports		12		12	1117
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature	<del>-</del>	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		ST CONDITIO	NO	Т	A = 25°(	;	SN54ABT162501		SN74ABT162501		UNIT
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$					-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
17	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m/	4	2			2				] `
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -32 \text{ m/s}$	4	2‡					2		
	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 48 mA	A ports			0.55		0.55			
$V_{OL}$	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA	Aports			0.55‡				0.55	\ \
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA	B ports					0.8		0.8	]
t.	$V_{CC} = 5.5 \text{ V},$		Control inputs			±1		±1		±1	μА
li .	$V_I = V_{CC}$ or GND				±100		±100		±100		
l <sub>OZH</sub> §	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_I \text{ or } V_O \le 4.5$	V			±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A == D	Outputs high			3		3		3	
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low			76		76		34	·mA
	$V_I = V_{CC}$ or GND	porto	Outputs disabled			3.3		3.3		3.3	
#	V <sub>CC</sub> = 5.5 V, One i	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,				5		6		5	mA
Δlcc#			A or B ports			1.5		1.5		1.5	] ""A
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 \	/	A or B ports		8						pF

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

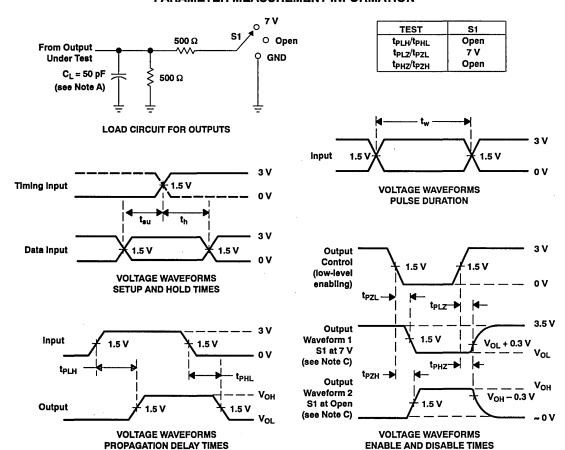
 $<sup>\</sup>S$  The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SEPTEMBER 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54ABT162600 . . . WD PACKAGE

SN74ABT162600 . . . DL PACKAGE

(TOP VIEW)

OEAB [] 1

LEAB 2

GND []4

A1 🛮 3

A2 🛮 5

A3 🛮 6

Vcc 🛛 7

A4 🛮 8

А5 П 9

A6 🛮 10

A7 🛮 12

A8 II 13

A9 🛮 14

A10 15

A11 [] 16

A12 17

GND [] 18

A13 🛮 19

A14 20

A15 [] 21

V<sub>CC</sub> 22

A16 23

A17 24

GND [ 25

A18 [ 26

OEBA [] 27

LEBA [ 28

GND [] 11

JUNE 1992-REVISED OCTOBER 1992

56 CLKENAB

55 CLKAB

54 B1

52 B2

51 B3

50 VCC

49 B4

48 B5 47 B6

46 GND

45 B7

44 ∏ B8

43 B9

42∏ B10

41 B11

40 N B12

39 GND

38 **∏** B13

37 🛮 B14

36∏ B15

35 VCC

34 N B16

33 B17

32 | GND

31 N B18

30 CLKBA

29 CLKENBA

53 T GND

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- B-Port Outputs Have Equivalent 25-Ω
   Series Resistors, So No External Resistors
   Are Required
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active-low. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The B-port outputs, which are designed to sink up to 12 mA, include 25- $\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162600 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162600 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT162600 is characterized for operation from -40°C to 85°C.

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# SN54ABT162600, SN74ABT162600 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPUTS							
CLKENAB	OEAB	LEAB	CLKAB	Α	В			
Х	Н	Х	Х	Х	Z			
Х	L	н	Х	L	L			
Х	L	н	X	н	Н			
н	L	L	,X	X	В <sub>0</sub> ‡			
н	L	L	X	X	Bo‡			
L	L	L	Į.	L	L			
L	L	Ĺ	ţ	н	н			
L	L	L	н	X	В <sub>0</sub> ‡			
L	L	L	L	X	B <sub>0</sub> §			

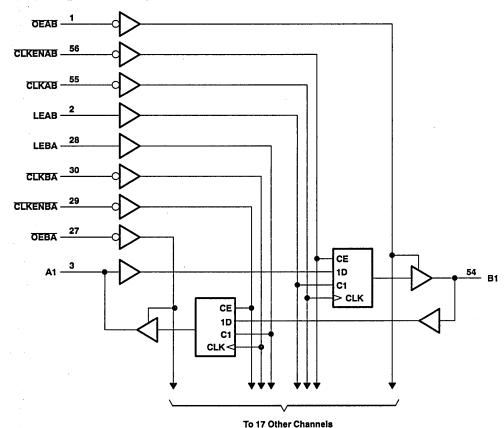
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

JUNE 1992-REVISED OCTOBER 1992

#### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>0</sub>	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT162600	96 mA
SN74ABT162600	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

JUNE 1992-REVISED OCTOBER 1992

#### recommended operating conditions (see Note 2)

			SN54ABT	162600	SN74ABT	162600	UNIT	
		MIN	MAX	MIN	MAX	UNII		
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V		
V <sub>IH</sub>	High-level input voltage		2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	٧		
Vi	Input voltage	0	Vcc	0	Vcc	V		
Гон	High-level output current			-24		-32	mA	
i	Low-level output current	A ports		48		64	mA .	
lor	Low-level output current	B ports		12		12	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		CT CONDITIO	NO	٦	A = 25°C	;	SN54ABT162600		SN74ABT162600		UNIT
PARAMETER	<b>'</b> 5	TEST CONDITIONS			TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_1 = -18 \text{ mA}$				•	-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5	-		2.5		2.5		
V	V <sub>CC</sub> = 5 V,						3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m/	4	2			2				1 °
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m/	A	2‡					2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA	A			0.55		0.55			
Vol	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA	A ports			0.55‡				0.55	٧
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA		B ports			0.8		0.8		0.8	1
	V <sub>CC</sub> = 5.5 V,	V <sub>CC</sub> = 5.5 V, Control inputs				±1		±1		±1	μА
կ	$V_I = V_{CC}$ or GND A or B ports					±100		±100		±100	μΛ
l <sub>OZH</sub> \$	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V					50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	5 V			±100				±100	μА
I <sub>CEX</sub>	V <sub>O</sub> = 5.5 V	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	$V_{CC} = 5.5 \text{ V},$		Outputs high			2		2		2	
Icc	I <sub>O</sub> = 0,	A or B ports	Outputs low			35		35		35	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	Ports	Outputs disabled			2		2		2	1
Δl <sub>CC</sub> #	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND		<del></del>		•	1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs				-						pF
Cio	Vo = 2.5 V or 0.5	v	A or B ports								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

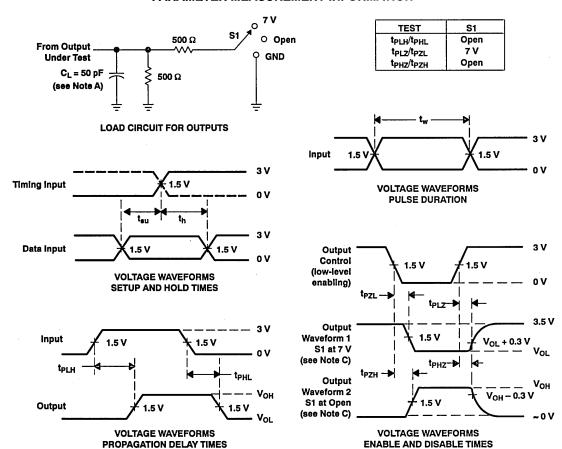
JUNE 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT	162600	SN74ABT			
				MIN	MAX	MIN	MAX	UNIT	
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz	
t <sub>w</sub> Pulse duration	Dulas duration	LEAB or LEBA high		1					
	Puise duration	CLKAB or CLKBA high or low					ns		
		A before CLKAB↓							
	Catua tima	B before CLKBA↓		1					
t <sub>su</sub>	Setup time	etup time	CLK high					ns	
		A before LEAB↓ or B before LEBA↓	CLK low		_				
	Hald time	A after CLKAB   or B after CLKBA	A after CLKAB or B after CLKBA			1		ns	
t <sub>h</sub>	Hold time	A after LEAB↓ or B after LEBA↓							

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

AUGUST 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- B-Port Outputs Have Equivalent 25-Ω
   Series Resistors, So No External Resistors
   Are Required
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink
   Small-Outline Packages (DL) and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

#### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

SN54ABT162601 ... WD PACKAGE SN74ABT162601 ... DL PACKAGE (TOP VIEW)

	_			
OEAB [	1	U	56	CLKENAB
LEAB [	2			CLKAB
A1 [				[] В1
GND [				GND
A2 [				B2
A3 [	6		51	] B3
Vcc [	]7			] v <sub>cc</sub>
A4 [	8		49	] B4
A5 [	9		48	] B5
A6 [			47	] B6
GND [	11			] GND
A7 [	12			] B7
A8 [	13			] B8
A9 [				] B9
A10 [				]B10
A11 [	16		41	] B11
A12 [	17		40	B12
GND [	18			GND
A13 [	19			]B13
A14 [	20		37	B14
A15 [	21		36	]B15
Vcc [	22		35	[]v <sub>cc</sub>
A16 [	23		34	]B16
A17 [	24			B17
GND [	25			GND
A18 [	26		31	]B18
OEBA [	1		30	CLKBA
LEBA [	28		29	CLKENBA

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active-low. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The B-port outputs, which are designed to sink up to 12 mA, include  $25-\Omega$  series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162601 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162601 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT162601 is characterized for operation from -40°C to 85°C.

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# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS AUGUST 1992-REVISED OCTOBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	OUTPUT				
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Х	Z
Х	L	н	X	L	L
X	L	Н	X	Н	н
Н	L	L	X	X	B₀‡
н	L	L	X	X	B₀‡
L	L	L	<b>†</b>	L	L
L	L	L	<b>†</b>	н	н
L	L	L	L	X	B <sub>0</sub> ‡
L	L	L	Н	X	B <sub>0</sub> §

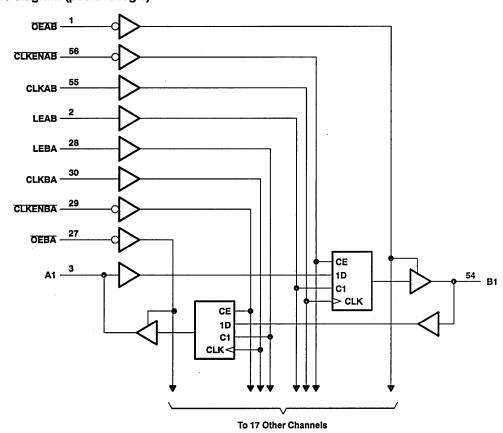
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

#### SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS AUGUST 1992-REVISED OCTOBER 1992

logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	−0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT162601	96 mA
SN74ABT162601	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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#### recommended operating conditions (see Note 2)

			SN54ABT	162601	SN74ABT	162601	LIMIT
l					MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage				2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current	-		-24		-32	mA
1	Low-level output current	A ports		48		64	mA
lor	Low-level output current	B ports		12		12	ША
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS -		Ţ	<sub>A</sub> = 25°C	;	SN54ABT	162601	SN74ABT162601		UNIT	
PANAMETER			No	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ mA}$		2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		<sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m/	4	2			2				*
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m/	4	2‡					2		1
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA	A ports			0.55		0.55			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA	Aports			0.55 <sup>‡</sup>				0.55	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 12 mA	B ports			0.8		0.8		0.8	ļ
I.	V <sub>CC</sub> = 5.5 V, Control inputs				±1		±1		.±1		
lı .	V <sub>I</sub> = V <sub>CC</sub> or GND A or B ports				±100		±100		±100	μΑ	
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		50		-50	μΑ
loff	V <sub>CC</sub> = 0 V,	$V_1$ or $V_0 \le 4.5$	<b>V</b>			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A D	Outputs high			2		2		2	
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		•	35		35		35	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	ports	Outputs disabled			2		2		2	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs									pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 \	/	A or B ports								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>^{\</sup>rm 9}$  The parameters  $\rm I_{OZH}$  and  $\rm I_{OZL}$  include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

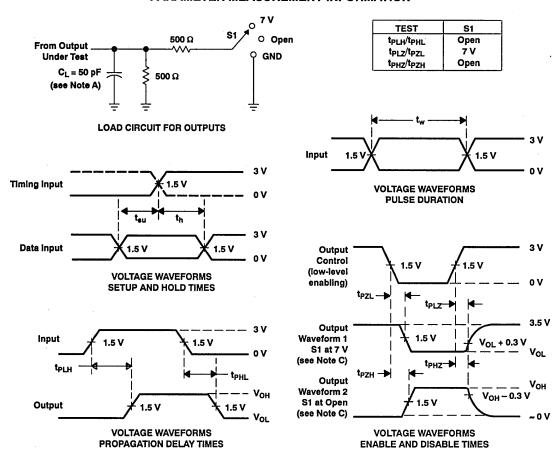
# SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS AUGUST 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT162601		SN74ABT		
				MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
		Pulse duration LEAB or LEBA high CLKAB or CLKBA high or low						
t <sub>w</sub> Pulse duration	1						ns	
		A before CLKAB†						
	Catua tima	B before CLKBA↑						
<sup>L</sup> SU	t <sub>su</sub> Setup time	Setup time	CLK high					ns
	A before LEAB tor B before LEBA	CLK low			<u> </u>			
	Hold time	A after CLKAB† or B after CLKBA†						
th	noia time	A after LEAB1 or B after LEBA1						ns

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	eran are are	1
ABT Octals	17871175	[ 2
ABT Widebus™		3
ABT Widebus+™		4
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#### ABT 25-Ω INCIDENT-WAVE SWITCHING DRIVERS

#### **Features**

- Incident-wave switching (IWS)
- Increased output-drive capability over standard ABT devices
- Designed for output drive of I<sub>OH</sub> = -80 mA, I<sub>OL</sub> = 188 mA across temperature and V<sub>CC</sub> conditions
- Sub-5-ns speed
- Power-on-demand active feedback circuitry
- Low input/output capacitance
- Widebus™ functionality planned with equivalent SSOP pinout

#### Benefits

- Improve system frequency response and reliability by eliminating 2 t<sub>pd</sub> delay shelf in the transition region caused by reflected waves
- Ideally suited to drive transmission lines on the incident wave at impedances as low as 10  $\Omega$  typically
- Ensure IWS at the input of receivers in highly capacitive, heavily loaded, or advanced backplane conditions where equivalent impedances go as low as 25 Ω worst case
- High-performance equivalent to standard ABT
- Allow for low static enable current consumption equivalent to standard ABT
- As receiving devices, do not load down the driving devices
- Low simultaneous switching noise, V<sub>OLP</sub> < 0.8 V typically</li>
- Drop-in replaceable to standard Widebus™ SSOP pinouts

The following table lists ABT  $25-\Omega$  incident-wave switching driver devices currently being evaluated for market introduction. Customers interested in learning more about Tl's plans for these devices should contact the General Purpose Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'ABT26245	48	25-Ω 16-Bit Transceiver

## SN54ABT25241, SN74ABT25241 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

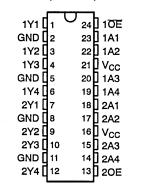
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>Δ</sub> = 25°C
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25  $\Omega$  or Greater
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

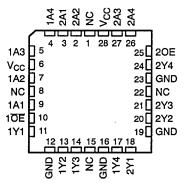
The 'ABT25241 is a  $25-\Omega$  octal buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The 'ABT25241 contains complementary output-enable (10E and 20E) inputs. When 10E is low and 20E is high, the device transmits data from the A inputs to the Y outputs. When 10E and 20E are high, the outputs are in the high-impedance state. Output-enable 10E affects only the 1Y outputs; output-enable 20E affects only the 2Y outputs.

SN54ABT25241 . . . JT PACKAGE SN74ABT25241 . . . DW OR NT PACKAGE (TOP VIEW)



SN54ABT25241 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

This buffer/driver is capable of sinking 188 mA of  $I_{OL}$  current, which facilitates switching 25- $\Omega$  transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.  $\overline{OE}$  should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT25241 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT25241 is characterized for operation from -40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



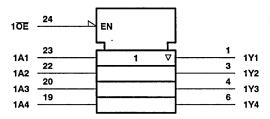
# SN54ABT25241, SN74ABT25241 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

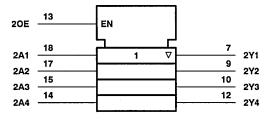
#### **FUNCTION TABLES**

INPU	JTS	OUTPUT
10E	1A	1Y
L	Н	н
L	L	L
Н	Х	Z

INP	JTS	ОПТРОТ
20E	2A	2Y
Н	Н	Н
н	L	L
L	Χ	Z

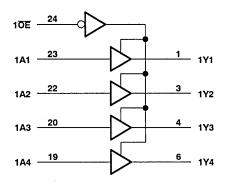
# logic symbol<sup>†</sup>

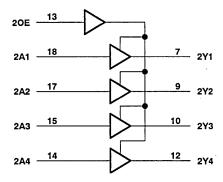




<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)





Pin numbers shown are for DW, JT, and NT packages.



# SN54ABT25241, SN74ABT25241 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> 0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the disabled or power-off state, V <sub>O</sub>
Voltage range applied to any output in the high state, V <sub>O</sub>
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Current into any output in the low state, Io: SN54ABT25241
SN74ABT25241
Operating free-air temperature range: SN54ABT25241
SN74ABT25241 –40°C to 85°C
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package
NT package
Storage temperature range –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions (see Note 2)

					SN74ABT25241		UNIT
1					MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage				2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vi	Input voltage			Vcc	0	Vcc	٧
lik	Input clamp current			-18		-18	mA
I <sub>OH</sub>	High-level output current			-53		-80	mA
loL	Low-level output current			125		188	- mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ပဲ

NOTE 2: Unused or floating inputs must be held high or low.



# SN54ABT25241, SN74ABT25241 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SN5	4ABT25	241	SN7	5241	UNIT	
PARAMETER				MIN	TYP	MAX	MIN	TYP <sup>†</sup>	MAX	UNI
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> =18 mA				-1.2			-1.2	٧
	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -3 mA					2.7			
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = 53 mA		2						V
	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -80 mA					2.4			
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 94 mA				0.55			0.55	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 125 mA		j		0.8				V
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 188 mA							0.7	7
11	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND		<u> </u>		±1			±1	μA
	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 0.8 V	1			100			100	
Inold	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 2 V	A pins			-100			-100	μΑ
lozH <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50			50	μА
l <sub>OZL</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50			-50	μΑ
1 <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±500			±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high	1		50			50	μА
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	•	-50		180	-50		180	mA
	., .,,,	0.1	Outputs high			500			500	μА
lcc	$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	Outputs open,	Outputs low	Î		30			30	mA
	1 - 4CC 01 CIAD	Outputs disabled				500			500	μΑ
A1 3	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,				1			4	mA	
Δl <sub>CC</sub> <sup>1</sup>	Other inputs at V <sub>CC</sub>	or GND				'				IIIA
Ci	V <sub>CC</sub> = 5 V,	V <sub>I</sub> =V <sub>CC</sub> or GND								pF
C <sub>o</sub>	V <sub>CC</sub> = 5 V,	V <sub>O</sub> =V <sub>CC</sub> or GND								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$ .

 $<sup>^{\</sup>ddagger}$  For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

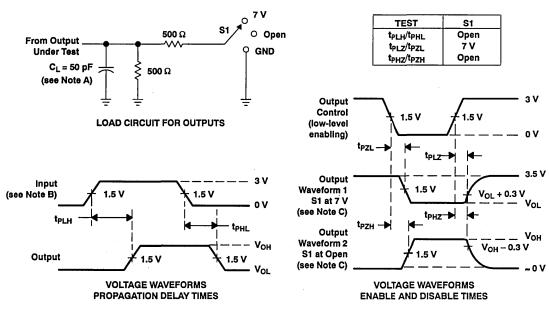
<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>&</sup>lt;sup>1</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54ABT25241, SN74ABT25241 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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## SN54ABT25244, SN74ABT25244 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

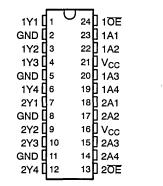
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25  $\Omega$  or Greater
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

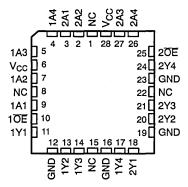
The 'ABT25244 is a  $25-\Omega$  octal buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

When the output-enable (1 $\overline{OE}$  and 2 $\overline{OE}$ ) inputs are low, the device transmits data from the A inputs to the Y outputs. When 1 $\overline{OE}$  and 2 $\overline{OE}$  are high, the outputs are in the high-impedance state.

#### SN54ABT25244...JT PACKAGE SN74ABT25244...DW OR NT PACKAGE (TOP VIEW)



# SN54ABT25244 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

This buffer/driver is capable of sinking 188 mA of  $I_{OL}$  current, which facilitates switching 25- $\Omega$  transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT25244 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT25244 is characterized for operation from  $-40^{\circ}$ C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



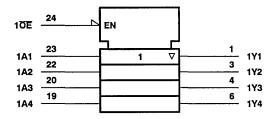
# SN54ABT25244, SN74ABT25244 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

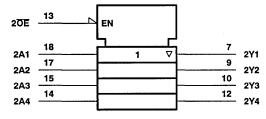
JUNE 1992-REVISED OCTOBER 1992

# FUNCTION TABLE (each buffer)

INPL	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	н
Н	X	Z

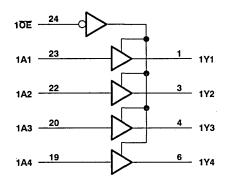
## logic symbol†

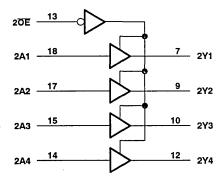




<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)





Pin numbers shown are for DW, JT, and NT packages.

## SN54ABT25244, SN74ABT25244 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	absolute maximum ratin	as over operating free	-air temperature range	(unless otherwise noted)†
---	------------------------	------------------------	------------------------	---------------------------

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, Vo	0.5 V to 5.5 V
Voltage range applied to any output in the high state, Vo	0.5 V to V <sub>CC</sub>
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mÅ
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Current into any output in the low state, Io: SN54ABT25244	250 mA
SN74ABT25244	376 mA
Operating free-air temperature range: SN54ABT25244	55°C to 125°C
SN74ABT25244	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

			SN54AB	SN54ABT25244		SN74ABT25244	
	Ţ			MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		
ViL	Low-level input voltage		1	0.8		0.8	V
VI	Input voltage		0	Vcc	0	Vcc	V
I <sub>IK</sub>	Input clamp current			-18		-18	mA
I <sub>OH</sub>	High-level output current			53		-80	mA
loL	Low-level output current			125		188	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

# SN54ABT25244, SN74ABT25244 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN54ABT25244			SN74ABT25244			UNIT		
PARAMETER			MIN TYP† MAX		MIN TYPT MAX						
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	V	
	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -3 mA					2.7				
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 53 mA		2						1 v	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -80 mA		7			2.4			l		
	V <sub>CC</sub> = 4.5 V,	4.5 V, I <sub>OL</sub> = 94 mA 4.5 V, I <sub>OL</sub> = 125 mA				0.55			0.55		
VoL	V <sub>CC</sub> = 4.5 V,				0.8					1 v	
	V <sub>CC</sub> = 4.5 V,								0.7	1	
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND		T		±1			±1	μА	
	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 0.8 V	A mine			100		100			
I <sub>hold</sub>	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 2 V	A pins	-					100	μA	
l <sub>OZH</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50			50	μА	
l <sub>OZL</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50			-50	μА	
loff	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±500			±100	μΑ	
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50			50	μΑ	
lo <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50		180	-50		180	mA	
	V <sub>CC</sub> = 5.5 V,	Outputs open,	Outputs high			500			500	μА	
1cc			Outputs low			30			30	mA	
	V <sub>I</sub> = V <sub>CC</sub> or GND Outputs disabled				500			500	μΑ		
Δlcc	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1			1	mA		
Ci	V <sub>CC</sub> = 5 V,	V <sub>I</sub> =V <sub>CC</sub> or GND		<b>—</b>						pF	
C <sub>o</sub>	V <sub>CC</sub> = 5 V,	Vo =Vcc or GND								pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$ .

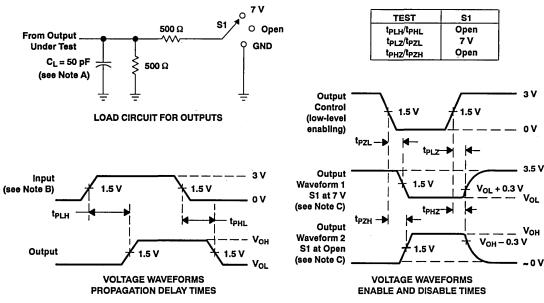
<sup>&</sup>lt;sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>5</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

#### SN54ABT25244, SN74ABT25244 25-OHM OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS JUNE 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns.  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54ABT25245, SN74ABT25245 25-OHM OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

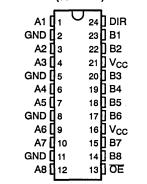
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Designed to Facilitate incident-Wave Switching for Line Impedances of 25  $\Omega$  or Greater
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Bus-Hold Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

#### description

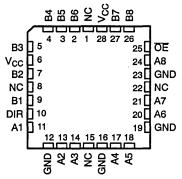
The 'ABT25245 is a 25- $\Omega$  octal bus transceiver designed for asynchronous communication between data buses. It improves both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that both buses are effectively isolated.

SN54ABT25245 ... JT PACKAGE SN74ABT25245 ... DW OR NT PACKAGE (TOP VIEW)



SN54ABT25245 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

This transceiver is capable of sinking 188 mA of  $I_{OL}$  current, which facilitates switching 25- $\Omega$  transmission lines on the incident wave. The distributed  $V_{CC}$  and GND pins minimize switching noise for more reliable system operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT25245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT25245 is characterized for operation from  $-40^{\circ}$ C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



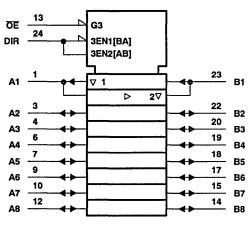
# SN54ABT25245, SN74ABT25245 25-OHM OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

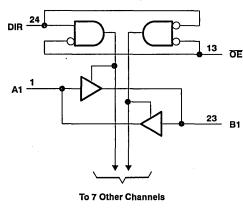
#### **FUNCTION TABLE**

INPUTS		OPERATION			
QE	DIR	OPERATION			
L	L	B data to A bus			
L	Н	A data to B bus			
Н	X	Isolation			

## logic symbol†



#### logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, Vo	0.5 V to 5.5 V
Voltage range applied to any output in the high state, Vo	0.5 V to V <sub>CC</sub>
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Current into any output in the low state, Io: SN54ABT25245 (A port)	250 mA
SN54ABT25245 (B port)	96 mA
SN74ABT25245 (A port)	376 mA
SN74ABT25245 (B port)	128 mA
Operating free-air temperature range: SN54ABT25245	55°C to 125°C
SN74ABT25245	40°C to 85°C
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	1 W
NT package	
Storage temperature range	

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT25245, SN74ABT25245 25-OHM OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS JUNE 1992-REVISED OCTOBER 1992

# recommended operating conditions (see Note 2)

			SN54AB	T25245	SN74ABT25245		
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
ViH	High-level input voltage		2		2		V
VIL	Low-level input voltage			8.0		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	٧
I <sub>IK</sub>	Input clamp current			-18		-18	mA
1	OH High-level output current	A ports		-53		-80	^
Іон		B ports		-24		-32	mA
1	I <sub>OL</sub> Low-level output current	A ports		125		188	
1OL		B ports		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



# SN54ABT25245, SN74ABT25245 25-OHM OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			TEGT COMPLETION		SN5	4ABT25	245	SN74ABT25245			
P/	ARAMETER		TEST CONDITION	S	MIN	TYP <sup>†</sup>	MAX	MIN	TYP	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	V
		$V_{CC} = 4.75 V$ ,	l <sub>OH</sub> = -3 mA					2.7			
•	A ports	$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -53 mA		2						
Ì		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -80 mA					2.4			
VoH		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5			V
l	B ports	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3			
		$V_{CC} = 4.5 \text{ V},$	I <sub>OH</sub> = -32 mA					2			
		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 94 mA				0.55			0.55	
ļ	A ports	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 125 mA				0.8				i
VOL		$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 188 mA							0.7	l v l
ĺ .	D. no. do	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 55 mA				0.55				i i
	B ports	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA							0.55	İ
Ī	Control inputs	V 55V	V V ~ CND				±1			±1	
4	A or B ports	VCC = 5.5 V,	$V_I = V_{CC}$ or GND				±100			±100	μА
	A or B name	$V_{CC} = 4.5 \text{ V},$	V <sub>I</sub> = 0.8 V				100			100	
hold	A or B ports	V <sub>CC</sub> = 4.5 V,	V <sub>I</sub> = 2 V				-100			-100	μΑ
lozH‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50			50	μА
l <sub>OZL</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50			-50	μА
loff		V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±500			±100	μА
ICEX		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50			50	μА
10 <sup>§</sup>	B ports	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50		180	-50		180	mA
			0.1-1-1-1-1	Outputs high			500			500	μА
lcc		$V_{CC} = 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GN}$	Outputs open,	Outputs low			30			30	mA
1		AI - ACC OLCIV		Outputs disabled			500			500	μА
. ,		V <sub>CC</sub> = 5.5 V,	One input at 3.4 V,				-				
∆lcc*		Other inputs at	V <sub>CC</sub> or GND		ŀ		1			'	mA
Ci	Control inputs	V <sub>CC</sub> = 5 V,	V <sub>I</sub> =V <sub>CC</sub> or GND								pF
Cio	A or B ports	V <sub>CC</sub> = 5 V,	V <sub>O</sub> =V <sub>CC</sub> or GND								pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT25245		SN74AB1	UNIT			
	( 01)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A or B	B or A							4.6	ns	
t <sub>PHL</sub>									4.6	115	
tpzh	Œ	A or B							5.3	ns	
t <sub>PZL</sub>	OE .	Aorb							6.3	7 "S	
t <sub>PHZ</sub>	ŌĒ	A or B							7.2		
t <sub>PLZ</sub>	<u> </u>								6.3	ns	



<sup>&</sup>lt;sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

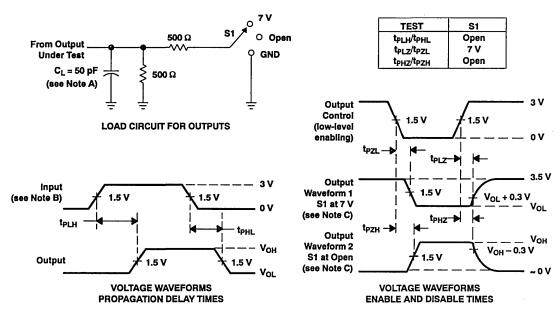
<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT25245, SN74ABT25245 25-OHM OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

JUNE 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All Input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

	General Information
	ABT Octals 2
	ABT Widebus™
	ABT Widebus+™
	ABT Memory Drivers 5
	ABT 25-Ω Incident-Wave Switching Drivers
•	Futurebus+/BTL Transceivers 7
	JTAG SCOPE™ Testability Devices
	LVT Octals 9
	LVT Widebus™
	Application Notes and Articles
	ABT Characterization Information 12
	Mechanical Data

#### Futurebus+/BTL TRANSCEIVERS

#### **Features**

- Fully compatible with IEEE 1194.1-1991 (BTL) and IEEE 896-1991 (Futurebus+) standards
- Sub-5-ns performance
- 7-, 8-, and 9-bit versions
- 18-channel transceiver version
- TTL A port and BTL B port
- BTL edge rates > 2 ns/V
- Split I/O TTL port
- Bias V<sub>CC</sub> pin
- TTL input clamp circuitry
- Open-collector BTL outputs
- Isolated logic GNDs and bus GNDs
- JTAG test access port (TAP) availability on Futurebus+ transceivers
- 52-pin standard quad flat pack and 100-pin shrink quad flat pack availability
- TI has established an alternate source

#### **Benefits**

- Execute proper BTL and Futurebus+ protocol
- ABT speed for Futurebus+ or advanced backplane transceiving
- Perform status/synch functions in Futurebus+ applications as well as UBT™ function in general-purpose BTL applications
- Can implement a full Futurebus+ interface with single-side mounting
- TTL-BTL and BTL-TTL translation
- High-throughput interface ideally suited for low-noise backplane applications
- Input and output pin separation allows for simultaneous data load/unload
- Minimize distortion during live insertion/withdrawal
- Allow for active termination
- High-drive 100-mA sink capability provides IWS capability down to 10  $\Omega$
- Minimize device-generated noise and transmission environment noise
- Pins allocated for 4-wire IEEE 1149.1-1990 standard test bus, which will be implemented in future versions
- Fine-pitch surface-mount packaging saves valuable board space and meets Futurebus+ connector requirements
- Standardization that comes from a common product approach

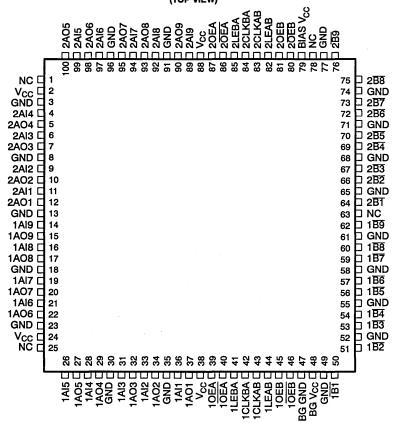
The following table lists Futurebus+/BTL transceiver devices currently being evaluated for market introduction. Customers interested in learning more about TI's plans for these devices should contact the General Purpose Logic Marketing hotline at (214) 997-5202.

DEVICE	PIN COUNT	DESCRIPTION
'FB2042	52	8-Bit Futurebus+ Transceiver
'FB2043	52	7-Bit Futurebus+ Transceiver

UBT is a trademark of Texas Instruments Incorporated.

- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transcelver Logic B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- Packaged in the High-Power Shrink Quad Flat Packages (SQFP) With 0.5-mm Pin Pitch
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL Input Structures Incorporate Active Clamping and Bus Hold Networks

#### PCA PACKAGE (TOP VIEW)



NC - No internal connection

## description

The SN74FB1650 contains two 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The B port operates at BTL signal levels. The open-collector B ports are specified to sink 100 mA. Two output enables, OEB and OEB, are provided for the B outputs. When OEB is low, OEB is high, or V<sub>CC</sub> is typically less than 2.5 V, the B port is turned off.

The A port operates at TTL signal levels. The A outputs reflect the inverse of the data at the B port when the A-port output enable, OEA, is high. When OEA is low or when V<sub>CC</sub> is typically less than 2.5 V, the A outputs are in the high-impedance state.

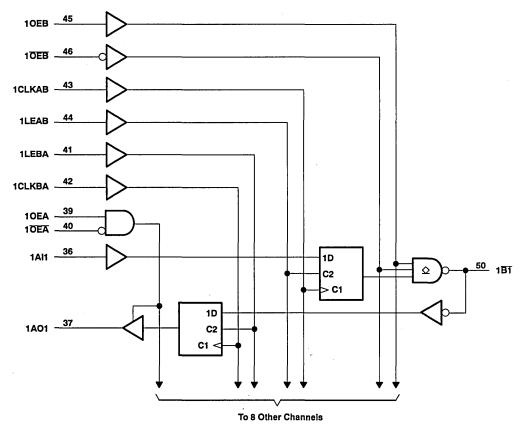
Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS V<sub>CC</sub> establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V<sub>CC</sub> is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

The SN74FB1650 is characterized for operation from 0°C to 70°C.

# functional block diagram





PRODUCT PREVIEW

# PRODUCT PREVIEW

# TRANSCEIVER FUNCTION TABLE

	INP	UTS		FUNCTION			
OEA	OEA	OEB	OEB	FUNCTION			
Х	<b>X</b> ,	Н	L,	A data to B bus			
L	н	X	X	B data to A bus			
L	н	н	L	A data to B bus, B data to A bus			
X	X	L	Х	D hus isolation			
X	X	X	Н	B-bus isolation			
н	Х	X	X	A hun inclusion			
Y	1	Y	Y	A-bus isolation			

#### STORAGE MODE TABLE

INP	UTS	FUNCTION
LE CLK		PUNCTION
Н	Х	Transparent
L	<b>†</b>	Store data
L	L	Storage

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range: (except B port)	–1.2 V to 7 V
(B port)	
Input current range (except B port)	40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state	5 V to 5.5 V
Voltage range applied to any output in the high state	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

# recommended operating conditions (see Note 1)

Storage temperature range ......

·			MIN	NOM	MAX	UNIT
V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.75	5	5.25	V
BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	B port	1.62			v
VIН	nigh-level input voltage	Except B port	2			
V	Low-level input voltage	B port	1.4		1.47	V
V <sub>IL</sub>	Low-level input voltage	Except B port			0.8	. •
l <sub>I</sub> K	Input clamp current				-18	mA
Іон	High-level output current	A port			-3	mA
1	Low-level output current	A port				A
lor	Low-level output current	B port			100	mA
TA	Operating free-air temperature		0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN74FB1650 18-BIT TTL/BTL UNIVERSAL STORAGE TRANSCEIVER

**AUGUST 1992** 

#### electrical characteristics over recommended operating free-air temperature range

	PARAMETER	TEST	CONDITIONS	MIN	TYP†	MAX	UNIT
V	B port	V <sub>CC</sub> = 4.75 V,	l <sub>I</sub> = -18 mA	ĺ		-1.2	٧
VIK	Except B port and AO port	V <sub>CC</sub> = 4.75 V,	l <sub>1</sub> = -40 mA			-0.5	V
V.	AO port	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -1 mA				V
V <sub>OH</sub>	AO port	VCC = 4.75 V	$I_{OH} = -3 \text{ mA}$	2.5	3.3		, v
	AO port	V <sub>CC</sub> = 4.75 V	I <sub>OL</sub> = 24 mA		0.35	0.5	
Vol	B port	V <sub>CC</sub> = 4.75 V	I <sub>OL</sub> = 80 mA	0.75		1.1	V
	B poit	VCC = 4.75 V	l <sub>OL</sub> = 100 mA	-		1.15	
l <sub>l</sub>	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 5.25 V	1		50	μΑ
l <sub>IH</sub> ‡	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2.7 V			50	μΑ
I <sub>IL</sub> ‡	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.5 V			-50	
ILL*	B port <sup>†</sup>	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.75 V			-100	μΑ
1	Al port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2 V	-100			
Inold	Al port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.5 V	100			μΑ
lozh	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 2.7 V			50	μА
lozL	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0.5 V			-50	μΑ
Іон	B port	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>O</sub> = 2.1 V			100	μΑ
los	A port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0	- 30		-150	mA
	A port to B port				25		
Icc	B port to A port	V <sub>CC</sub> = 5.25 V,	l <sub>0</sub> = 0		60		mA
	Outputs disabled	1					
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND				5	pF
Co	A port	V <sub>O</sub> = V <sub>CC</sub> or GND					pF
_	D nort nor D4404.0	V <sub>CC</sub> = 0 to 4.75 V	· · · · · · · · · · · · · · · · · · ·	i		6	pF
Cio	B port per P1194.0	V <sub>CC</sub> = 4.75 V to 5.25 V			5		

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C.

# live insertion specifications over recommended operating free-air temperature range

		•		• •		_		
PAR/	METER		TEST COND	ITIONS	MIN	TYP	MAX	UNIT
I (BI/	AS V <sub>CC</sub> )	V <sub>CC</sub> = 0 to 4.75 V,	V <sub>B</sub> = 0 to 2 V	V (BIAS V ) 45 V to 55 V			450	
ICC (DIX	45 VCC)	V <sub>CC</sub> = 4.25 to 5.25 V	V <sub>B</sub> = 0 to 2 V	$V_{I}$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V			10	μΑ
V <sub>O</sub>	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V	V to 5.5 V	1.62		2.1	٧
		V <sub>CC</sub> = 0,	V <sub>B</sub> = 1 V,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	-1			
lo	B port	V <sub>CC</sub> = 0 to 5.25 V,	OEB = 0 to 0.8 V				100	μΑ
		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V				100	

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			MIN	TYP	MAX	UNIT
t <sub>w</sub>	Pulse duration, LCA or LCB					ns
	Setup time	A or B before LE			2	
ī <sub>SU</sub>	Setup time	A or B before CLK↑			2	ns
	Hold time	A or B after LE			1	
ιή		A or B after CLK↑			1	ns



For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>9</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Α	В			5	ns
t <sub>PHL</sub>	7 ^ I	8			5	115
t <sub>PLH</sub>	LEAB	B			6	ns
t <sub>PHL</sub>	LEAD				6	2
t <sub>PLH</sub>	CLKAB	В			6	ns
t <sub>PHL</sub>	CLIVIB				6	10
t <sub>PLH</sub>	LEBA	A			6	ns
t <sub>PHL</sub>	LEDA	^			6	2
t <sub>PLH</sub>	CLKBA	A			6	ns
t <sub>PHL</sub>		^			6	115
t <sub>PLH</sub>	В	A			5	ns
t <sub>PHL</sub>	7	^			5	113
t <sub>PLH</sub>	OEB or OEB	В			5	ns
t <sub>PHL</sub>		В			5	115
<sup>t</sup> PZH	OEA or OEA	A			5	ns
t <sub>PZL</sub>	T OEAGIOEA	<u> </u>			5	113
t <sub>PHZ</sub>	OEA or OEA	Α			5	ns
t <sub>PLZ</sub>		^			5	119
t <sub>sk(p)</sub> ‡	Skew for any single channel   t <sub>PHL</sub> – t <sub>PLH</sub>	A to B or B to A		0.5		ns
t <sub>sk(o)</sub> ‡	Skew between drivers in the same package	A to B or B to A		1		ns
t <sub>t</sub>	Transition time, B outputs (1.3 V to 1.8 V	)	1	2	3	ns
t <sub>PR</sub>	B-port input pulse rejection			1		ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. ‡ Skew values are applicable for through mode only.

#### PARAMETER MEASUREMENT INFORMATION **16.5** Ω TEST **S1** From Output From Output Test **500** Ω Open **Under Test** t<sub>PLH</sub>/t<sub>PHL</sub> **Under Test Point** tpLZ/tpZL 7 V O GND t<sub>PHZ</sub>/t<sub>PZH</sub> GND 30 pF $C_L = 50 pF$ 500 Ω (see Note A) (see Note A) LOAD CIRCUIT FOR A OUTPUTS LOAD CIRCUIT FOR B OUTPUTS 1.5 V Timing Input 3 V 3 V **Data Input** 1.5 V 1.5 V Input 1.5 V 0 V **VOLTAGE WAVEFORMS** SETUP AND HOLD TIMES **VOLTAGE WAVEFORMS PULSE DURATION** Input 1.5 V (see Note B) 0 V **t**PLH V<sub>OH</sub> 3 V 1.55 V 1.5 V Output Output 1.5 V VOL Control **VOLTAGE WAVEFORMS** (see Note B) PROPAGATION DELAY TIMES (A to B) 3.5 V Input .55 V Output (see Note B) V<sub>OL</sub> + 0.3 V S1 at 7 V (see Note C) t<sub>PHL</sub> t<sub>PHZ</sub> tpzH - $V_{OH}$ Output V<sub>OH</sub> -- 0.3 V 1.5 V Output (see Note C)

- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: TTL Inputs PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ . BTL Inputs PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

**VOLTAGE WAVEFORMS** 

**ENABLE AND DISABLE TIMES (A PORT)** 

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES (B to A)

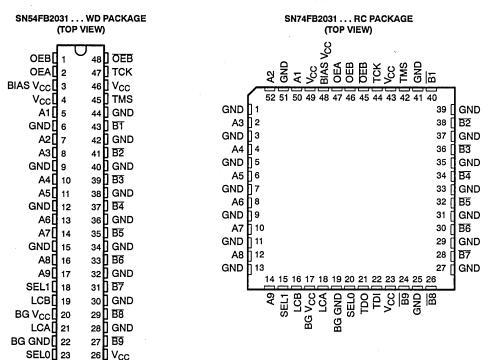
Figure 1. Load Circuit and Voltage Waveforms



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- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transceiver Logic B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Minimum B-Port Edge Rate = 2 ns
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise

- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- Available in Plastic Quad Flatpack (RC) and Ceramic Flatpack (WD) Packages
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination



#### description

The 'FB2031 is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and  $\overline{OEB}$ , are provided for the  $\overline{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the B port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.



TDO 1 24

25 TDI

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# description (continued)

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2031. Currently TMS and TCK are not connected and TDI is shorted to TDO.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

The SN54FB2031 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74FB2031 is characterized for operation from 0°C to 70°C.

#### TRANSCEIVER FUNCTION TABLE

	INPUTS		FUNCTION			
OEA	OEB	OEB	FONCTION			
L	Н	L	A data to B bus			
н	L	X	B data to A bus			
Н	Х	Н	D data to A bus			
н	Н	L	A data to B bus, B data to A bus			
L	L	X	Isolation			
L	Х	Н				

#### STORAGE MODE TABLE

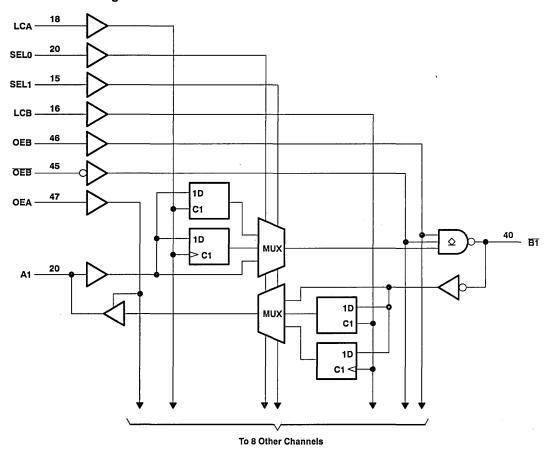
LCA, LCB	RESULT
0	Transparent
1	Latches latched
<b>.</b> ↑	Flip-flops triggered

#### **SELECT FUNCTION TABLE**

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Thru	Thru
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

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# functional block diagram



Pin numbers shown are for RC package.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range: (except B port)	1.2 V to 7 V
	–1.2 V to 5.5 V
Input current range (except B port)	40 mA to 5 mA
Voltage range applied to any B output in the disabled or po	wer-off state5 V to 5.5 V
Voltage range applied to any output in the high state	–5 V to V <sub>CC</sub>
Current applied to any single output in the low state: (A p	ort) 96 mA
( <u>B</u> p	ort)
Storage temperature range	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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# recommended operating conditions (see Note 1)

			SN	SN54FB2031		SN74FB2031			
			MIN	NOM	MAX	MIN	МОМ	MAX	UNIT
V <sub>CC,</sub> BIAS V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V	High lavel innut valtage	B port	1.62			1.62			· V
V <sub>IH</sub>	High-level input voltage	Except B port	2			2			l <sup>v</sup>
V <sub>IL</sub>	Low-level input voltage	B port			1.47			1.47	٧
VIL.	Low-level Input voltage	Except B port			0.8			0.8	
I <sub>IK</sub>	Input clamp current				-18			-18	mA
Гон	High-level output current	A port				1		-3	mA
I	Low-level output current	A port						24	A
loL	Low-level output current	B port			100			100	mA
TA	Operating free-air temperature		-55		125	0		70	ô

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN	SN54FB2031			SN74FB2031		
	PARAMETER	IESI C	TEST CONDITIONS			MAX	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA		240				-1.2	
VIK	Except B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -40 mA						-0.5	V
Voн	A port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA							v '
VOH	Apon	VCC = 4.5 V	I <sub>OH</sub> = -3 mA				2.5	3.3		V
	A port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 μA							
V	A port	VCC = 4.5 V	I <sub>OL</sub> = 24 mA					0.35	0.5	v
V <sub>OL</sub>	Doort	V 45V	I <sub>OL</sub> = 80 mA				0.75		1.1	
	B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 100 mA							
1	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V						50	μΑ
I <sub>IH</sub> ‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V		-				50	μΑ
l <sub>IL</sub> ‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V						-50	
ıtr.	B port†	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.75 V						-100	μΑ
Іон	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	V <sub>O</sub> = 2.1 V						100	μΑ
los§	A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0				- 30		-150	mA
	A port to B port							25		
lcc	B port to A port	V <sub>CC</sub> = 5.5 V,	l <sub>O</sub> = 0					60		mA
	Outputs disabled	1								
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND							5	pF
С	A port	Vo = Vcc or GND								pF
	B	V <sub>CC</sub> = 0 to 4.5 V							6	
Cio	B port per P1194.0	V <sub>CC</sub> = 4.5 V to 5.5 V							5	pF

<sup>†</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C. ‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54FB2031		SN74FB2031		
	( 17	(02.1.2.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A (thru mode)	В			5					ns	
t <sub>PHL</sub>	// (una modo)				5					_ :	
t <sub>PLH</sub>	A (transparent)	В			6					ns	
t <sub>PHL</sub>	A (transparent)				6						
t <sub>PLH</sub>	LCA	B			7					ns	
t <sub>PHL</sub>					7						
t <sub>PLH</sub>	LCB	A			9					ns	
t <sub>PHL</sub>					9						
t <sub>PLH</sub>	SEL1 or SEL0	Α		-	5.5					ns	
t <sub>PHL</sub>	OLLI OI OLLO				5.5					- 15	
t <sub>PLH</sub>	SEL1 or SEL0	B			7					ns	
t <sub>PHL</sub>	SELI OI SELO				7					115	
t <sub>PLH</sub>	B (thru mode)	Α			6					ns	
t <sub>PHL</sub>	B (till tillode)	^			6						
t <sub>PLH</sub>	B (transparent)	Α			7					ns	
t <sub>PHL</sub>	D (transparent)	^			7					115	
t <sub>PLH</sub>	OEB or OEB	B	5.5					ns			
t <sub>PHL</sub>	T OEB OI OEB	b		5.5						ns	
t <sub>PZH</sub>	OEA	Α			4						
t <sub>PZL</sub>		^	4						ns		
t <sub>PHZ</sub>	OEA	A			5						
t <sub>PLZ</sub>		^			5	<del> </del>				ns	
t <sub>sk(p)</sub>	Skew for any single channel   t <sub>PHL</sub> – t <sub>PLH</sub>	A to B or B to A		0.5						ns	
t <sub>sk(o)</sub>	Skew between drivers in the same package A to B or B to A			1					•	ns	
t <sub>t</sub>	Transition time, B outputs (1.3 V to 1.8 V)			2				1	3	ns	
t <sub>PR</sub>	B-port input pulse rejection							1		ns	

# live insertion specifications over recommended operating free-air temperature range

PARAMETER		TECT COMPITIONS			SN54FB2031		SN74F	B2031	UNIT
			TEST CONDITIONS		MIN	MAX	MIN	MAX	UNII
I /DI	AC \/\	V <sub>CC</sub> = 0 to 4.5 V	V <sub>R</sub> = 0 to 2 V	0V V (BIAGY ) 45V4-55V			ĺ	450	
I <sub>CC</sub> (BIAS V <sub>CC</sub> )		V <sub>CC</sub> = 4.5 to 5.5 V	J AB = 0 10 5 A	2  V (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V				10	μΑ
V <sub>O</sub>	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> )	= 4.5 V to 5.5 V			1.62	2.1	V
		V <sub>CC</sub> = 0,	V <sub>B</sub> = 1 V,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V			-1		
$I_O$ B port $V_{CC} = 0$ to 5.5		V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V					100	μΑ
	$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V	·				100		



#### PARAMETER MEASUREMENT INFORMATION **16.5** Ω From Output TEST S1 From Output 500 Ω **Under Test** tplh/tphl Open **Under Test Point** 7 V tplz/tpzl t<sub>PHZ</sub>/t<sub>PZH</sub> Open 30 pF C<sub>L</sub> = 50 pF 500 Ω (see Note A) (see Note A) LOAD CIRCUIT FOR A OUTPUTS LOAD CIRCUIT FOR B OUTPUTS **Timing Input** 1.5 V 3 V **Data Input** 1.5 V 1.5 V Input 1.5 V **VOLTAGE WAVEFORMS** 0 V **SETUP AND HOLD TIMES VOLTAGE WAVEFORMS PULSE DURATION** Input (see Note B) 0 V t<sub>PLH</sub> ٧он 1.55 V Output Output Control (see Note B) **VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES (A to B) - t<sub>PZL</sub> 3.5 V Input 1.55 V Output (see Note B) S1 at 7 V (see Note C) t<sub>PHZ</sub> →

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

Output

B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns. BTL Inputs - PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.

t<sub>PZH</sub> →

Output

(see Note C)

VoH

V<sub>OH</sub> – 0.3 V

**VOLTAGE WAVEFORMS** 

**ENABLE AND DISABLE TIMES (A PORT)** 

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

**t**PLH

D. The outputs are measured one at a time with one transition per measurement.

**VOLTAGE WAVEFORMS** 

PROPAGATION DELAY TIMES (B to A)

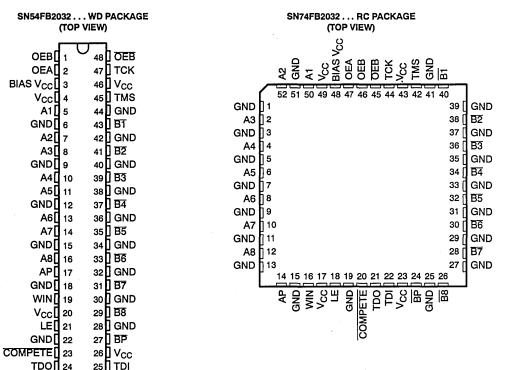
Figure 1. Load Circuit and Voltage Waveforms



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- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transceiver Logic B
  Port
- Open-Collector B-Port Outputs Sink 100 mA
- Minimum B-Port Edge Rate = 2 ns
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise

- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- Available in Plastic Quad Flatpack (RC) and Ceramic Flatpack (WD) Packages
- B-Port Blasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination



# description

The 'FB2032 is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The  $\overline{B}$  port operates at BTL-signal levels. The open-collector  $\overline{B}$  ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and  $\overline{OEB}$ , are provided for the  $\overline{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is typically less than 2.5 V, the  $\overline{B}$  port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the B port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.



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#### description (continued)

The A-port data can be latched by taking the latch enable (LE) high. When LE is low, the latches are transparent.

The Futurebus+ protocol logic can be activated by taking COMPETE low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the B arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and B8 are the most significant bits, and A1 and B1 are the least significant bits. If OEB is high and OEB is low during this operation, and the A bus of the first module wins priority, it will assert its arbitration number on the B-arbitration bus.

AP and BP are the bus parity bits. The winning module may assert BP low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus+ arbitration controller will latch its arbitration number into the A port and wait for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller will read back the current value of the B bus (by taking OEA high) and determine the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2032. Currently TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V<sub>CC</sub> establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V<sub>CC</sub> is not connected.

BG V<sub>CC</sub> and BG GND are the supply inputs for the bias generator.

The SN54FB2032 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74FB2032 is characterized for operation from 0°C to 70°C.

#### TRANSCEIVER FUNCTION TABLE

	INPUTS		FUNCTION				
OEA	OEB	OEB	1 FUNCTION				
L	Н	L	Ā data to B bus				
H	L	Х	B data to A bus				
Н	Ĥ	L	Ā data to B bus, B data to A bus				
L L	L X	X H	Isolation				

#### STORAGE MODE TABLE

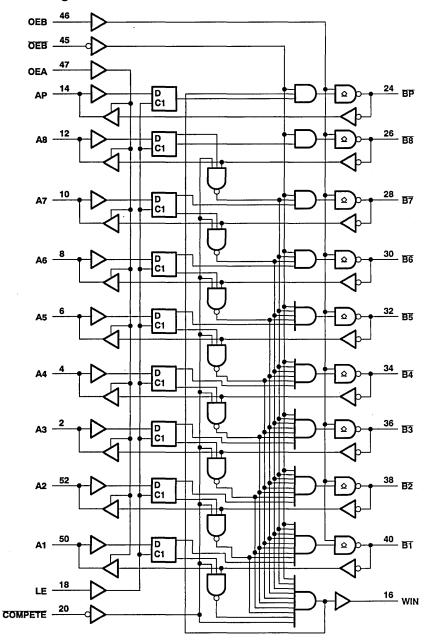
LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

#### **SELECT FUNCTION TABLE**

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Thru	Thru
] 1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch



# functional block diagram



Pin numbers shown are for RC package.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>					
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V				
Input voltage range: (except BP, B port)	1.2 V to 7 V				
(BP, B port)					
Input current range (except B port)	40 mA to 5 mA				
Voltage range applied to any B output in the disabled or power-off state	0.5 V to 5.5 V				

 (B port)
 200 mA

 Storage temperature range
 -65°C to 150°C

## recommended operating conditions (see Note 1)

			SN	54FB20	32	SN74FB2032			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
.,	Lijeh level innstrukture	BP, B port	1.62			1.62			٧
V <sub>IH</sub>	High-level input voltage	Except B port	2			2			
.,	Low-level input voltage	BP, B port	1		1.47			1.47	٧
V <sub>IL</sub>		Except B port			0.8			0.8	
l <sub>IK</sub>	Input clamp current				-18			-18	mA
Гон	High-level output current	AP, WIN, A port						-3	mA
1.		AP, WIN, A port						24	
lor	Low-level output current	BP, B port			100			100	mA
TA	Operating free-air temperature		-55		125	0		70	°C

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST CONDITIONS		SN	SN54FB2032			SN74FB2032		
l	PARAMETER	I EST CC	TEST CONDITIONS		TYP <sup>†</sup>	MAX	MIN	TYP	MAX	UNIT
V	BP, B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA						-1.2	V
VIK	Except BP, B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -40 mA						-0.5	<b>V</b>
VoH	AP, WIN, A port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA							v
VOH	Ar, Will, A poli	VCC = 4.5 V	$I_{OH} = -3 \text{ mA}$				2.5	3.3		
	AP, WIN, A port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 μA							
VOL	Ar, Will, A poli	VCC - 4.5 V	I <sub>OL</sub> = 24 mA					0.35	0.5	v
VOL	BP, B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 80 mA				0.75		1.1	·
	pr, b poit	VCC = 4.5 V	I <sub>OL</sub> = 100 mA							
I	Except BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V						50	μΑ
I <sub>IH</sub> ‡	Except BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	T					50	μА
1 2	Except BP, B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V						-50	μΑ
1,1,2	BP, B port†	V <sub>CC</sub> = 5.5 V,	V <sub>i</sub> = 0.75 V						-100	μΛ
ЮН	BP, B port	V <sub>CC</sub> = 0 to 5.5 V,	V <sub>O</sub> = 2.1 V						100	μА
los§	AP, WIN, A port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0				- 30		-150	mA
	A port to B port							25		
lcc	B port to A port	V <sub>CC</sub> = 5.5 V,	l <sub>O</sub> = 0					60		mA
	Outputs disabled	1								
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND		1					5	pF
Co	A port	Vo = Vcc or GND								pF
	E nort nor B1104.0	V <sub>CC</sub> = 0 to 4.5 V							6	"E
Cio	B port per P1194.0 V <sub>CC</sub> = 4.5 V to 5.5 V			<u> </u>					5	pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25 ^{\circ}\text{C}$ .

<sup>\*</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54FB2032		SN74FB2032		UNIT	
	(INPUT)	(001201)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>РLН</sub>	4 45	N NN							8		
t <sub>PHL</sub>	A or AP	B or BP							8	ns	
t <sub>PLH</sub>		<b>F</b>							9		
t <sub>PHL</sub>	^	B <sub>n−1</sub>							9	ns	
t <sub>PLH</sub>	A	BP				i			10		
t <sub>PHL</sub>	<b>-</b>   ^	БР							10	ns	
t <sub>PLH</sub>	В	ъ.							9	20	
t <sub>PHL</sub>	7 P	B <sub>n−1</sub>							9	ns	
<sup>‡</sup> PLH	LE	B							7.5	no	
t <sub>PHL</sub>	7	В							7.5	ns	
t <sub>PLH</sub>	LE	ВР							7.5	ns	
t <sub>PHL</sub>		Dr.							7.5	112	
t <sub>PLH</sub>	B or BP	A or AD							7.5		
t <sub>PHL</sub>	B or BP	B or BP A or AP							7.5	ns	
t <sub>PLH</sub>	В	WIN	1						8.5	ns	
t <sub>PHL</sub>	7 °	AAMA							8.5		
<sup>t</sup> PLH	A WIN	VAZINI							7.6	ns	
t <sub>PHL</sub>	7 ^	AAIIA							7.6		
t <sub>PLH</sub>	LE	WIN							7	J ne	
t <sub>PHL</sub>		AAIIA							7	115	
tpLH	COMPETE	WIN							5.5	ns	
t <sub>PHL</sub>	COMPETE	AAIIA							5.5	115	
t <sub>PLH</sub>	OEB	WIN				·			6	1	
t <sub>PHL</sub>		VVIIN							6	ns	
t <sub>PLH</sub>	COMPETE	В						i	7.5		
t <sub>PHL</sub>	COMPETE	Р							7.5	ns	
t <sub>PLH</sub>	COMPETE	ВР							6.5		
t <sub>PHL</sub>	COMPETE	ВР							6.5	ns	
t <sub>PLH</sub>	OEB	В	<u> </u>						6.5		
t <sub>PHL</sub>									6.5	ns	
t <sub>PLH</sub>	OEB	B							6.5	ns	
t <sub>PHL</sub>		<sup>B</sup>							6.5	HS	
t <sub>PZH</sub>	OEA.	Α							5.5		
t <sub>PZL</sub>	7 054	OEA A							5.5	ns	
t <sub>PHZ</sub>	054					l	<del></del>		7		
t <sub>PLZ</sub>	OEA	A							7	ns	
t <sub>t</sub>	Transition time, B output	ts (1.3 V to 1.8 V)	. 2					1	3	ns	
t <sub>PR</sub>	B-port input pulse reject								1	ns	

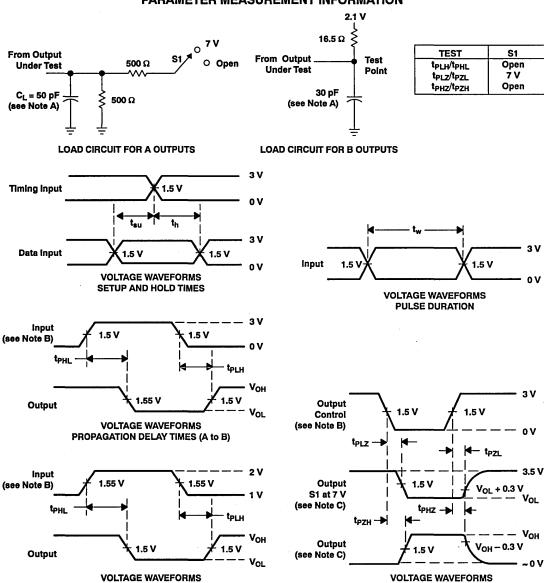


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# live insertion specifications over recommended operating free-air temperature range

PARAMETER TEST CONDITIONS		TEGT COMPLETIONS			B2032	SN74FB2032		UNIT
		TEST CONDITIONS	MIN	MAX	MIN	MAX	IINU	
Haa (BIAS Vaa)		V <sub>CC</sub> = 0 to 4.5 V	V <sub>B</sub> = 0 to 2 V, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V				450	
		V <sub>CC</sub> = 4.5 to 5.5 V	VB = 0 to 2 V, VI (BIAS VCC) = 4.5 V to 5.5 V			10	μΑ	
V <sub>O</sub>	B port	$V_{CC} = 0$ ,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V			1.62	2.1	٧
		V <sub>CC</sub> = 0,	$V_B = 1 \text{ V}, \qquad V_I \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$			-1		
IO B port	B port	V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V				100	μΑ
	- 1	V <sub>CC</sub> = 0 to 2.2 V,	OEB = 0 to 5 V				100	

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: TTL Inputs PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>t</sub> ≤ 2.5 ns, t<sub>t</sub> ≤ 2.5 ns. BTL Inputs PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>t</sub> ≤ 2.5 ns, t<sub>t</sub> ≤ 2.5 ns.

**ENABLE AND DISABLE TIMES (A PORT)** 

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

PROPAGATION DELAY TIMES (B to A)

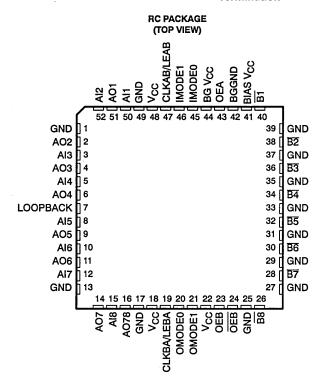
Figure 1. Load Circuit and Voltage Waveforms



# SN74FB2033 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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- TTL A Port, Backplane Transceiver Logic (BTL) B Port
- Open-Collector B-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- Packaged in Plastic Quad-Flat Packages (PQFP) With 0.65-mm Pin Pitches
- B-Port Blasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination



#### description

The SN74FB2033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector B port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as transparent-high latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.



# SN74FB2033 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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#### description (continued)

The AO port enable/disable control is provided by OEA. When OEA is low or when  $V_{CC}$  is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The B port is controlled by OEB and  $\overline{\text{OEB}}$ . If OEB is low or  $\overline{\text{OEB}}$  is high or when  $V_{CC}$  is typically less than 2.5 V the B port is inactive. If OEB is high and  $\overline{\text{OEB}}$  is low, the B port is active.

BG V<sub>CC</sub> and BG GND are the bias generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive (B port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on  $V_{OH}$  during a low-to-high transition. The other clamps out ringing below the BTL  $V_{OL}$  voltage of 0.75 V. Both these clamps are only active during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS V<sub>CC</sub> establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V<sub>CC</sub> is not connected.

The SN74FB2033 is characterized for operation from 0°C to 70°C.

#### **FUNCTION TABLE**

			INPUTS				FUNCTION/MODE
OEB	OEB	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	1 GNOTION/MODE
L	Х	Х	X	Х	X	X	Isolation
X	н	X	X	X	X	X	isolation
Н	L	L	L	Х	Х	X	Al to B, buffer mode
Н	L	L	H	Х	Х	X	Al to B, flip-flop mode
н	L	Н	Х	Х	Х	Х	Al to B, latch mode
L	Х	Х	X	L	L	L	B to AO, buffer mode
X	Н	X	X	L	L	L	B to AO, buller mode
L	×	Х	X	L	Н	L	Pto AO die des mode
X	Ĥ	X	X	L	Н	L	B to AO, flip-flop mode
L	Х	X	X	Н	Х	L	Tto AO Joseph mode
X	н	X	X	н	X	L	B to AO, latch mode
L	×	X	Х	L	L	Н	Alas AO buffer made
X	н	X	X	L	L	н	Al to AO, buffer mode
L	×	Х	Х	L	Н	н	Also AO die des mode
X	н	X	×	L	н	н [	Al to AO, flip-flop mode
L	×	Х	х	Н	Х	Н	Alta AO Isiib aasta
X	н	X	X	н	X	н	Al to AO, latch mode
Н	L	Х	X	Х	Х	L	Al to B, B to AO
	L X H H C X L X L X L X L X X L X	L X X H H L H L L X X H L X X H L X X H L X X H L X X H L X X H L X X H L X X H L X X H	L X X X H X H L L H L L H L H L X X X H X L X X X H X L X X X H X L X X X H X L X X X H X L X X X H X L X X X H X L X X X H X X H X X H X X H X X H X X H X X H X X H X	OEB         OEB         OMODE1         OMODE0           L         X         X         X           X         H         X         X           H         L         L         L           H         L         L         H           H         L         H         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X         H         X         X           X	OEB         OEB         OMODE1         OMODE0         IMODE1           L         X         X         X         X           X         H         X         X         X           H         L         L         L         X           H         L         L         H         X           H         L         H         X         X           L         X         X         X         L           X         H         X         X         L           X         H         X         X         X         H           L         X         X         X         X         H           L         X         X         X         X         L           X         H         X         X         X         L           X         H         X         X         X         L           X         H         X         X         X         L           X         H         X         X         X         L           X         H         X         X         X         L           X         H	OEB         OEB         OMODE1         OMODE0         IMODE1         IMODE0           L         X         X         X         X         X           X         H         X         X         X         X           X         H         L         L         L         X         X           X         H         L         H         X         X         X         X           L         X         X         X         L         L         L         L         L         L         L         L         L         L         L         L         L         H         X         X         X         L         L         H         X         X         L <td>OEB         OEB         OMODE1         OMODE0         IMODE1         IMODE0         LOOPBACK           L         X         X         X         X         X         X         X           X         H         X         X         X         X         X         X           H         L         L         L         X         X         X         X           H         L         H         X         X         X         X         X           L         X         X         X         L         L         L         L           X         H         X         X         L         H         L         L           X         H         X         X         L         H         L         L           X         H         X         X         L         H         L         L           X         H         X         X         X         H         X         L           X         H         X         X         X         H         X         L           X         H         X         X         X         L         H         &lt;</td>	OEB         OEB         OMODE1         OMODE0         IMODE1         IMODE0         LOOPBACK           L         X         X         X         X         X         X         X           X         H         X         X         X         X         X         X           H         L         L         L         X         X         X         X           H         L         H         X         X         X         X         X           L         X         X         X         L         L         L         L           X         H         X         X         L         H         L         L           X         H         X         X         L         H         L         L           X         H         X         X         L         H         L         L           X         H         X         X         X         H         X         L           X         H         X         X         X         H         X         L           X         H         X         X         X         L         H         <



# PRODUCT PREVIEW

#### **ENABLE/DISABLE FUNCTION TABLE**

	INPUTS		OUTPUTS		
OEA	OEB	OEB	AO	B	
L	Х	Х	Z		
н	X	X	Active (H or L)		
×	L	L		Inactive (H)	
×	L	н	<b>.</b>	Inactive (H)	
×	н	L		Active (H or L)	
×	н	н		Inactive (H)	

# **BUFFER FUNCTION TABLE**

INPUT	OUTPUT
L	Н
Н	L

#### **LATCH FUNCTION TABLE**

INPU	OUTPUT		
CLK/LE	DATA	OUIFUI	
Н	L	Н	
Н	н	L	
L	Х	Qo	

#### LOOPBACK FUNCTION TABLE

LOOPBACK	Q†
L	B port
Н	Point P‡

<sup>&</sup>lt;sup>†</sup> Q is the input to the B-to-A logic element.

## **FUNCTION SELECT TABLE**

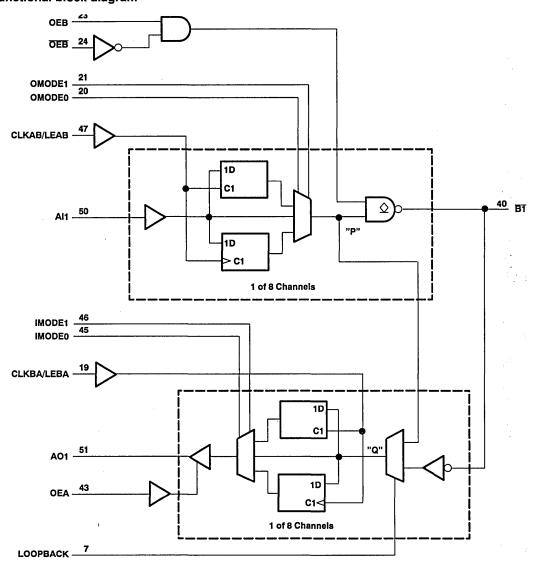
INP	UTS	SELECTED LOGIC
MODE1	MODE0	ELEMENT
L	L	Buffer
L	Н	Flip-flop
Н	X	Latch

#### **FLIP-FLOP FUNCTION TABLE**

INPU	OUTPUT	
CLK/LE	DATA	COTPUT
L	Х	Qo
<b>†</b>	L	Н
1	Н	L

<sup>&</sup>lt;sup>‡</sup> P is the output of the A-to-B logic element (see functional block diagram).

# functional block diagram





PRODUCT PREVIEW

# SN74FB2033 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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absolute maximum ratings over operating free-air	temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range: (except B port)	–1.2 V to 7 V
	–1.2 V to 5.5 V
Input current range, (except B port)	–40 mA to 5 mA
Voltage range applied to any B output in the disabled	or power-off state0.5 V to 5.5 V
	0.5 V to V <sub>CC</sub>
Current applied to any single output in the low state:	(A port) 96 mA
	(B port) 200 mA
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# recommended operating conditions (see Note 1)

			MIN	МОМ	MAX	UNIT	
V <sub>CC</sub> , BG V <sub>CC</sub>	Supply voltage		4.75	5	5.25	V	
BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	٧	
VIH	High level innervables	B port	1.62	1.62		V	
	High-level input voltage	Except B port	2			l	
V	Low-level input voltage	B port			1.47	v	
V <sub>IL</sub>		Except B port			0.8	· •	
Гон	High-level output current	AO port			-3	mA	
L	1 and level autout autout	AO port			24	A	
IOL	Low-level output current B port				100	mA	
T <sub>A</sub>	Operating free-air temperature		0		70	ç	

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.



# SN74FB2033 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>IK</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>I</sub> = -18 mA			-1.2	٧	
	AO port	V <sub>CC</sub> = 4.75 V to 5.25 V,	I <sub>OH</sub> = -10 μA			V <sub>CC</sub> -1.1		
VoH		V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -3 mA	2.5	2.85	3.4	V	
			$I_{OH} = -32 \text{ mA}$	2			•	
	AO port	V <sub>CC</sub> = 4.75 V	I <sub>OL</sub> = 20 μA		0.33	0.5		
V		VCC = 4.75 V	I <sub>OL</sub> = 55 mA			0.8	v	
V <sub>OL</sub>	Dood	V 475 V	1 <sub>OL</sub> = 100 mA	0.75		1.1	V	
	B port	V <sub>CC</sub> = 4.75 V	I <sub>OL</sub> = 4 mA	0.5				
l <sub>l</sub>	Except B port	V <sub>CC</sub> = 0,	V <sub>I</sub> = 5.25 V			100	μΑ	
	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2.7 V			50		
lн	B port <sup>†</sup>	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>I</sub> = 2.1 V			100	μΑ	
	Except B port	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.5 V			-50		
ΙţĽ	B port†	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.75 V			-100	μΑ	
Гон	B port	V <sub>CC</sub> = 0 to 5.25 V,	V <sub>O</sub> = 2.1 V	1		100	μΑ	
lozh	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 2.7 V			50	μΑ	
lozL	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0.5 V			-50	μΑ	
los‡	AO port	V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0	40	-80	-150	mA	
Icc	All outputs on	V <sub>CC</sub> = 5.25 V,	I <sub>O</sub> = 0		45	85	mA	
Ci	Al port and control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND				5	pF	
Co	AO port	V <sub>O</sub> = V <sub>CC</sub> or GND					pF	
^	E-04-04-04-0	V <sub>CC</sub> = 0 to 4.75 V				6	25	
Cio	B port per P1194.0	V <sub>CC</sub> = 4.75 V to 5.25 V				5	pF	

 $<sup>^{\</sup>dagger}$  For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	MIN MAX	UNIT
		MIN MAX		
t <sub>w</sub>	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	4	4	ns
t <sub>su</sub>	Setup time, data before CLKAB/LEAB or CLKBA/LEBA†	4	4	ns
th	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	1	1	ns



<sup>\*</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

# PRODUCT PREVIEW

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	то (оитрит)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN MAX	MAX	UNIT
	(1147-01)		MIN	TYP	MAX			
t <sub>PLH</sub>	Al (thru mode)	В	1	3	4.5	1	5	ns
t <sub>PHL</sub>	Ai (uiid iiiode)		1	3	4.5	1	5	2
t <sub>PLH</sub>	B (thru mode)	AO	1	4	6	1	7	ns
t <sub>PHL</sub>	B (till till till de)		1	4	6	1	7	113
tpLH	Al (transparent)	В	1		5	1	6	ns
t <sub>PHL</sub>	Ai (transparent)	ь .	1		5	1	6	113
t <sub>PLH</sub>	B (transparent)	AO	1		6.5	1	7.5	ns
t <sub>PHL</sub>	B (transparent)	A0	1		6.5	1	7.5	113
t <sub>PLH</sub>	OEB	В	1	3	4.5	1	5	ns
t <sub>PHL</sub>	7 025	ь	1	3	4.5	1	5	113
tpLH	OEB	В	1.5	3.4	5	1.5	5	20
t <sub>PHL</sub>			1.5	3.4	5	1.5	5	ns
tpzH	OEA	AO	1	4	5	1	6	ns
t <sub>PZL</sub>			1	4	5	1	6	113
t <sub>PHZ</sub>	OEA	AO	1	3	4	. 1	5	ns
t <sub>PLZ</sub>	7		1	3	4	1	5	113
t <sub>PLH</sub>	CLKAB/LEAB	В	1.5	4	6	1.5	7	ns
t <sub>PHL</sub>			1.5	4	6	1.5	7	113
tpLH	CLKBA/LEBA	AO	1.5	4	5	1.5	6	ns
t <sub>PHL</sub>	CLRBAYLEBA		1.5	4	5.5	1.5	6.5	115
t <sub>PLH</sub>	OMODE	В	1	4	6	1	7	ns
tpHL		ь	1	4	6	1	7	115
t <sub>PLH</sub>	IMODE	10	1	4	5	1	6	
t <sub>PHL</sub>		AO	1	4	5.5	1	6.5	ns
t <sub>PLH</sub>	LOOPBACK	AO	1		8	1	9	ns
t <sub>PHL</sub>	T LOOPBACK	AU	1		8	1	9	115
	Rise time 1.3 V to 1.8 V	В	1			1	2.5	
t <sub>t</sub>	Fall time 1.8 V to 1.3 V	ن	1			0.5	2.5	ns
	Rise or fall time 10% to 90%	AO	2			2	5	
tpR	B-port input pulse rejection					1		ns

# live insertion specifications over recommended operating free-air temperature range

PARAMETER			TEST COND	DITIONS	MIN	TYP	MAX	UNIT
I Ioo (BIAS Voo)		V <sub>CC</sub> = 0 to 4.5 V,	V <sub>R</sub> = 0 to 2 V.	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	SV) - 45V to 55V		400	μА
		$V_{CC} = 4.5 \text{ to } 5.5 \text{ V},$	- VB = 0 t0 ≥ V,	VB = 0 to 2 v, V  (BIAS VCC) = 4:5 V to 5:5 V			10	μ.
Vo	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5	V to 5.5 V	1.62		2.1	V
		V <sub>CC</sub> = 0,	V <sub>B</sub> = 1 V,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	-1			
lo	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	OEB = 0 to 0.8 V				100	μΑ
		$V_{CC} = 0 \text{ to } 2.2 \text{ V},$	OEB = 0 to 5 V				100	

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#### miscellaneous characteristics

	•		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OHP</sub> †	Peak bus voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1			4	٧
V <sub>OHV</sub> †	Minimum bus voltage during turnoff of 100 mA into 40 nH	B port	See Figure 1	1.62			٧
Volv	Minimum bus voltage during high to low switch	B port	I <sub>OL</sub> = -50 mA	0.3			٧

<sup>†</sup> Parameter is based on characterization data but not tested.

# PARAMETER MEASUREMENT INFORMATION

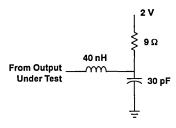
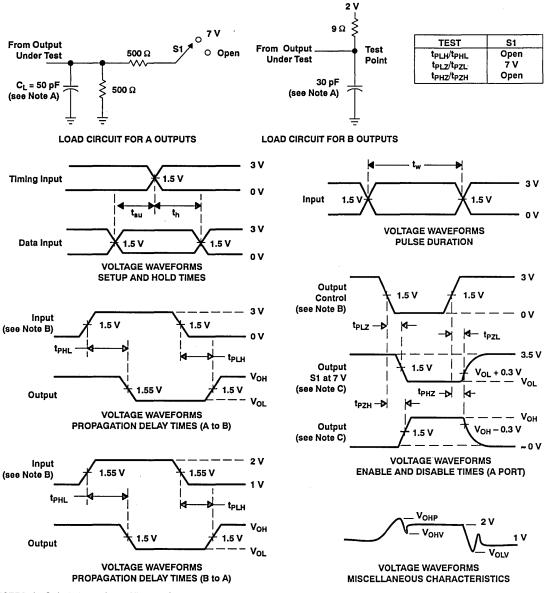


Figure 1. Load Circuit V<sub>OHP</sub>, V<sub>OHV</sub>



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

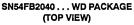
- B. All input pulses are supplied by generators having the following characteristics: TTL Inputs PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns. BTL Inputs PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

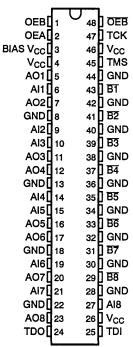
Figure 2. Load Circuit and Voltage Waveforms

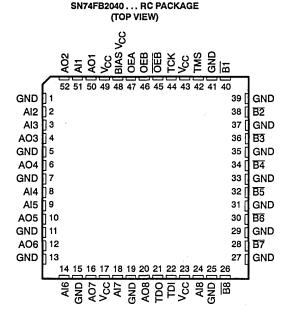


- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transceiver Logic B
- Open-Collector B-Port Outputs Sink 100 mA
- Minimum B-Port Edge Rate = 2 ns
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise

- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- Available in Plastic Quad Flatpack (RC) and Ceramic Flatpack (WD) Packages
- B-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage







# description

The 'FB2040 is an 8-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The B port operates at BTL-signal levels. The open-collector B ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and OEB, are provided for the B outputs. When OEB is high and OEB is low, the B port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, OEB is high, or V<sub>CC</sub> is typically less than 2.5 V, the B port is turned off.



#### SN54FB2040, SN74FB2040 8-BIT TTL/BTL TRANSCEIVERS

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#### description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the B port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2040. Currently TMS and TCK are not connected and TDI is shorted to TDO.

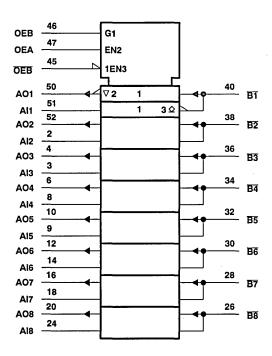
BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

The SN54FB2040 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74FB2040 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE** 

	INPUTS		FUNCTION			
OEB	OEB	OEA	FUNCTION			
L	X H	L L	Isolation			
L	X H	H H	B data to AO bus			
Н	L	L	Al data to B bus			
н	L	Н	All data to B bus, B data to AO bus			

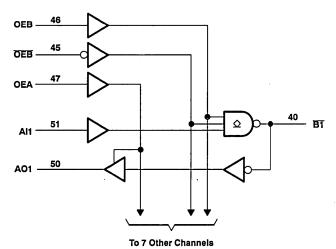
#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for RC package.



#### functional block diagram



Pin numbers shown are for RC package.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range: (except B port)	1.2 V to 7 V
(B port)	. −1.2 V to 5.5 V
Input current range (except B port)	-18 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state	. −0.5 V to 5.5 V
Voltage range applied to any output in the high state	0.5 V to V <sub>CC</sub>
Current applied to any single output in the low state: (A port)	96 mA
(B port)	200 mA
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 1)

			SN54FB2040			SN74FB2040			UNIT	
					MAX	MIN	NOM	MAX	UNII	
V <sub>CC</sub> , BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
V <sub>IH</sub>	High-level input voltage	B port	1.62			1.62			٧	
	nigri-level input voltage	Except B port	2			2				
V <sub>IL</sub>	Law level input veltage	B port			1.47			1.47	V	
	Low-level input voltage	Except B port			0.8			0.8	<b>v</b> ,	
l <sub>IK</sub>	Input clamp current				-18			-18	mA	
Гон	High-level output current	AO port						-3	mA	
1	Law lovel output ourrent	AO port						24		
loL	Low-level output current B port				100			100	mA	
TA	Operating free-air temperature		-55		125	0		70	ç	

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.



# SN54FB2040, SN74FB2040 8-BIT TTL/BTL TRANSCEIVERS

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	7507.00	TEST CONDITIONS		54FB20	40	SN	74FB20	10	UNIT
	PARAMETER	IESI CC	SNOTTIONS	MIN	TYP	MAX	MIN	TYP†	MAX	UNII
V	B port	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA					-	-1.2	٧
Viķ	Except B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -40 mA						-0.5	٧
.,	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA							V
VoH	AC port	VCC = 4.5 V	I <sub>OH</sub> = -3 mA				2.5	3.3		ľ
	AO port	V 45V	l <sub>OL</sub> = 20 μA							
V	AO poit	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 24 mA			,		0.35	0.5	v
V <sub>OL</sub>	B port	V 45V	I <sub>OL</sub> = 80 mA				0.75		1.1	·
,		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 100 mA						1.15	
1	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V						50	μΑ
l <sub>iH</sub> ‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V						50	μΑ
I <sub>IL</sub> ‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V						-50	μΑ
	B port†	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.75 V						-100	μΑ
IOH	B port	V <sub>CC</sub> = 0 to 5.5 V,	V <sub>O</sub> = 2.1 V						100	μΑ
lozh	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V						50	μΑ
lozL	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V						50	μΑ
los	AO port	V <sub>CC</sub> = 5.5 V <sub>i</sub>	V <sub>O</sub> = 0				- 30		-150	mA
	Al port to B port			1				25		
Icc	B port to AO port	V <sub>CC</sub> = 5.5 V,	l <sub>O</sub> = 0					60		mA
	Outputs disabled	1								
C <sub>i</sub>	Al port and control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND								pF
C <sub>o</sub>	AO port	V <sub>O</sub> = V <sub>CC</sub> or GND								pF
_	P nort nor P1104 0	V <sub>CC</sub> = 0 to 4.5 V V <sub>CC</sub> = 4.5 V to 5.5 V				1			6	nE
Cio	B port per P1194.0								5	pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

# PRODUCT PREVIEW

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	CC = 5 V 4 = 25°C		SN54F	B2040	SN74FB2040		UNIT	
	. (1117-01)	(0011-01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	- Al	В		3.9						ns	
t <sub>PHL</sub>		ь		3.6						113	
t <sub>PLH</sub>	В	AO		3.9						ns	
t <sub>PHL</sub>		ΑΟ		3.8						ns	
t <sub>PLH</sub>	OEB	B		5.1						ns	
t <sub>PHL</sub>		ь		4.3						113	
t <sub>PLH</sub>	OEB	B		4.4						ns	
t <sub>PHL</sub>				4.1						29	
t <sub>PZH</sub>	OEA	AO		3.2						ns	
t <sub>PZL</sub>	J OLA	ΑΘ	3								
t <sub>PHZ</sub>	OEA	, AO		3.2						ns	
t <sub>PLZ</sub>		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		2.7						110	
t <sub>sk(p)</sub>	Skew for any single channel   t <sub>PHL</sub> - t <sub>PLH</sub>	Al to B or B to AO							0.75	ns	
t <sub>sk(o)</sub>	Skew between drivers in the same package	Al to B or B to AO		1	1.5				2	ns	
t <sub>t</sub>	Transition time, B outpu	ts (1.3 V to 1.8 V)		2				1	3	ns	
t <sub>PR</sub>	B-port input pulse reject	ion						1		ns	

#### live insertion specifications over recommended operating free-air temperature range

PARAMETER			TECT CONDITIONS		SN54FB2040		SN74FB2040	
PAR	AMETER	ETER TEST CONDITIONS		MIN	MAX	MIN	MAX	UNIT
I <sub>CC</sub> (BIAS V <sub>CC</sub> )		V <sub>CC</sub> = 0 to 4.5 V	V 0 to 2 V V /PIAC V ) - 4 E V to E E V				450	μА
ICC (DI	MS VCC)	V <sub>CC</sub> = 4.5 to 5.5 V	$V_B = 0 \text{ to } 2 \text{ V},  V_I \text{ (BIAS } V_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$				10	μΛ
V <sub>O</sub>	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V			1.62	2.1	V
		$V_{CC} = 0$ , $V_{B} = 1 V$ , $V_{I} (BIAS V_{CC}) = 4.5 V to 5.5$	V <sub>B</sub> = 1 V, V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		-	-1		
Io B po	B port	V <sub>CC</sub> = 0 to 5.5 V,	OEB = 0 to 0.8 V				100	μΑ
	1	$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V				100	

#### PARAMETER MEASUREMENT INFORMATION 16.5 Ω **TEST** S1 From Output From Output Test 500 Ω Open **Under Test** tplH/tpHL **Under Test Point** Żν tpLZ/tpZL t<sub>PHZ</sub>/t<sub>PZH</sub> Open 30 pF C<sub>L</sub> = 50 pF 500 $\Omega$ (see Note A) (see Note A) LOAD CIRCUIT FOR B OUTPUTS LOAD CIRCUIT FOR A OUTPUTS input (see Note B) $v_{oh}$ 3 V 1.55 V Output Output Control **VOLTAGE WAVEFORMS** (see Note B) PROPAGATION DELAY TIMES (A to B) 3.5 V Input Output (see Note B) 1.55 V V<sub>OL</sub> + 0.3 V S1 at 7 V (see Note C) tpHZ **t**PHL tezn : $\mathbf{v}_{\text{OH}}$ VOH Output V<sub>OH</sub> – 0.3 V 1.5 V 1.5 V (see Note C) Output ~0V VOL **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS**

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: TTL Inputs - PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ ,  $t_r \leq$  2.5 ns. BTL Inputs - PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ ,  $t_r \leq$  2.5 ns.  $t_r \leq$  2.5 ns.

**ENABLE AND DISABLE TIMES (A PORT)** 

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

PROPAGATION DELAY TIMES (B to A)

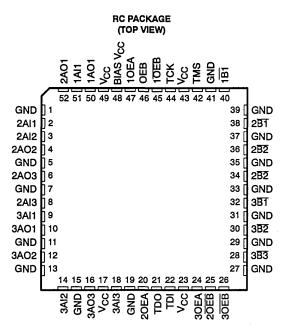
Figure 1. Load Circuit and Voltage Waveforms

#### SN74FB2041 7-BIT TTL/BTL TRANSCEIVER

NOVEMBER 1991-REVISED JUNE 1992

- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transceiver Logic B
   Port
- Open-Collector B-Port Outputs Sink 100 mA
- Minimum B-Port Edge Rate = 2 ns
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise

- BIAS V<sub>CC</sub> Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- Packaged in Plastic Quad-Flat Packages (PQFP) With 0.65-mm Pin Pitches
- B-Port Blasing Network Preconditions the Connector and PC Trace to the Backplane Transcelver Logic High-Level Voltage



#### description

The SN74FB2041 is a 7-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The B port operates at BTL-signal levels. The open-collector B ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and OEB, are provided for the B outputs. When OEB is high and OEB is low, the B port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, OEB is high, or V<sub>CC</sub> is typically less than 2.5 V, the B port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the  $\overline{B}$  port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the SN74FB2041. Currently TMS and TCK are not connected and TDI is shorted to TDO.



#### SN74FB2041 7-BIT TTL/BTL TRANSCEIVER

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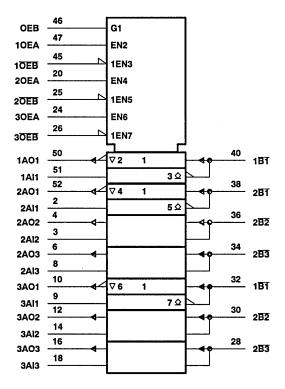
#### description (continued)

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected. The SN74FB2041 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE** 

	INPUTS		FUNCTION				
OEB	OEB	OEA	FONCTION				
L	Х	L	Isolation				
Х	Н	L	isolation				
L	Х	Н	B data to AO bus				
Х	Н	н	B data to AO bus				
н	L	L	Al data to B bus				
н	L	Н	Al data to B bus, B data to AO bus				

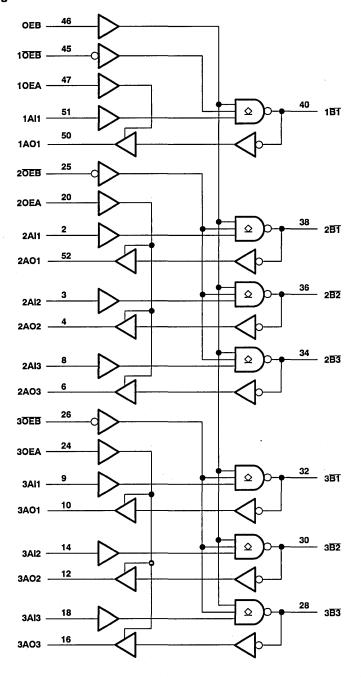
#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



#### functional block diagram





#### SN74FB2041 7-BIT TTL/BTL TRANSCEIVER

NOVEMBER 1991-REVISED JUNE 1992

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range: (except B port)	
(B port)	1.2 V to 5.5 V
Input current range (except B port)	–18 mA to 5 mA
Voltage range applied to any B output in the disabled or	
Voltage range applied to any output in the high state .	
Current applied to any single output in the low state: (A	
	B port) 200 mA
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT	
V <sub>CC,</sub> BIAS V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V	
V	High-level input voltage	B port	1.62			v	
V <sub>IH</sub>	High-level input voltage	Except B port	2			·	
V <sub>IL</sub>	Levelevel innet voltage	B port			1.47	V	
	Low-level input voltage	Except B port			0.8		
lık	Input clamp current				-18	mA	
Гон	High-level output current	AO port			-3	mA	
•	Law layed extent extent	AO port			24	mA	
I <sub>OL</sub>	Low-level output current B port				100		
TA	Operating free-air temperature		0		70	°C	

NOTE 1: Unused or floating pins (input or I/O) must be held high or low.



#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TES"	T CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
.,	B port	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA			-1.2	٧
VIK	Except B port	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -40 mA			-0.5	V
VoH	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA				V
∨он	AC port	VCC = 4.5 V	I <sub>OH</sub> = -3 mA	2.5	3.3		<b>V</b>
	AO port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 μA				
VoL	AO poit	VCC = 4.5 V	I <sub>OL</sub> = 24 mA		0.35	0.5	,
<b>V</b> OL	B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 80 mA	0.75		1.1	•
	15 poil	VCC = 4.5 V	I <sub>OL</sub> = 100 mA			1.15	
l <sub>l</sub>	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			50	μΑ
1 <sub>IH</sub> ‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			50	μА
I <sub>IL</sub> ‡	Except B port	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V			-50	μА
ılL.	B port†	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.75 V			-100	μΛ
loH	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	V <sub>O</sub> = 2.1 V			100	μΑ
lozh	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50	μΑ
lozL	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50	μΑ
los§	AO port	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-30		-150	mA
	Al port to B port				25		
Icc	B port to AO port	V <sub>CC</sub> = 5.5 V,	l <sub>O</sub> = 0		65		mA
	Outputs disabled	1					
Ci	Al port and control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND					pF
Co	AO port	V <sub>O</sub> = V <sub>CC</sub> or GND					pF
C.	B port per P1194.0	V <sub>CC</sub> = 0 to 4.5 V				6	pF
Cio	D poit per F 1194.0	V <sub>CC</sub> = 4.5 V to 5.5 V				5	PΓ

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25$ °C. ‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

#### SN74FB2041 7-BIT TTL/BTL TRANSCEIVER

NOVEMBER 1991-REVISED JUNE 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

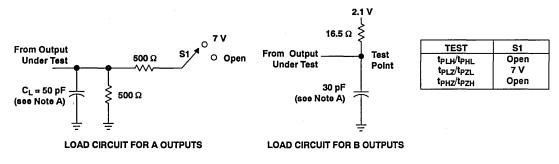
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 \ T <sub>A</sub> = 25°		MIN	MAX	UNIT	
	(	(0011.01)	MIN TYP	MAX				
t <sub>PLH</sub>	, Al	В	3.9	i			ns	
t <sub>PHL</sub>	, AI	<b>.</b>	3.6					
tры	В	AO	3.8				ns	
t <sub>PHL</sub>			3.8			,	110	
t <sub>PLH</sub>	OEB	B	4.8			n		
t <sub>PHL</sub>	025		4.3					
t <sub>PLH</sub>	OEB	В	4.2				ns	
t <sub>PHL</sub>	OLD	5	3.8			19		
t <sub>PZH</sub>	OEA	AO	3					
t <sub>PZL</sub>	) VEA	Α0	3			ns		
t <sub>PHZ</sub>	OEA	AO	3.3				ns	
t <sub>PLZ</sub>		Α0	2.6				2	
t <sub>sk(p)</sub>	Skew for any single channel   t <sub>PHL</sub> – t <sub>PLH</sub>	Al to B or B to AO				0.75	ns	
t <sub>sk(o)</sub>	Skew between drivers in the same package	Al to B or B to AO	1	1.5		2	ns	
t <sub>t</sub>	Transition time, B outputs (1.3 V	2		1	3	ns		
t <sub>PR</sub>	B-port input pulse rejection				1		ns	

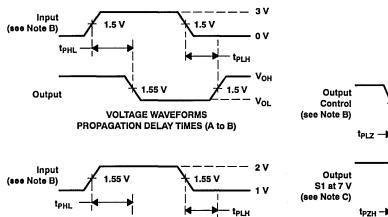
#### live insertion specifications over recommended operating free-air temperature range

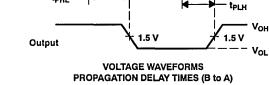
PARA	METER		TEST CONDITIONS			TYP	MAX	UNIT	
I <sub>CC</sub> (BIAS V <sub>CC</sub> )		V <sub>CC</sub> = 0 to 4.5 V,	$V_B = 0 \text{ to } 2 \text{ V}$ , $V_L \text{ (BIAS V}_{CC}) = 4.5 \text{ V to } 5.5 \text{ V}$				450	μА	
ICC (BIA	3 VCC)	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V},$	] VB = 0 t0 2 V,	V  (BIAS VCC) = 4.5 V to 5.5 V			10	μ	
V <sub>O</sub>	B port	V <sub>CC</sub> = 0,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V			2.1	V	
		V <sub>CC</sub> = 0,	V <sub>B</sub> = 1 V,	V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V	-1				
lo lo	B port	$V_{CC} = 0 \text{ to } 5.5 \text{ V,}$	OEB = 0 to 0.8 V				100	μΑ	
l		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V				100		

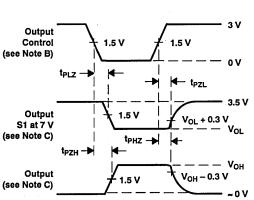


#### PARAMETER MEASUREMENT INFORMATION









VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES (A PORT)

NOTES: A. C<sub>L</sub> Includes probe and jig capacitance.

- B. All Input pulses are supplied by generators having the following characteristics: TTL Inputs PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns. BTL Inputs PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	
ABT Octals	2
ABT Widebus™	3
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#### JTAG SCOPE™ TESTABILITY DEVICES

#### **Features**

- Compatibility with IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) and boundary-scan architecture
- EPICIIB™ submicron process technology
- Sub-6-ns maximum propagation delays
- Octal and Widebus™ availability
- EIAJ SSOP, JEDEC SSOP, and EIAJ SQFP fine-pitch surface-mount packaging
- Bus-hold circuitry
- 18- and 20-bit UBT™ architectures
- Additional SCOPE™ instructions available such as:
  - INTEST
  - Parallel Signature Analysis (PSA)
  - Pseudo-Random Pattern Generation (PRPG)
- Test-mode or normal-mode operation
- Members of the Texas Instruments SCOPE™ family of testability products
- TI has established an alternate source

#### **Benefits**

- Facilitate testing of complex circuit board assemblies via a 4-wire test access port
- High-performance, low-power, high-drive, low-noise equivalents of standard ABT buffers/drivers/transceivers
- No system throughput or cycle time penalty for boundary-scan implementation
- Functional equivalents to standard ABT devices offer system and test designers flexible integration options
- Save valuable board space
- Reduce component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Advanced integration, as one UBT™ can replace nearly all common bus interface logic
- Built-in self-test feature allows easy upgrade for advanced JTAG test applications
- IEEE Standard 1149.1-1990 protocol can be bypassed for applications not requiring boundary scan
- Compatible with complete line of system-level test products including controllers, SCOPE™ DIARY, bus monitors, scan path linkers, scan path selectors, application specific products, and very large scale integration products
- Standardization that comes from a common product approach

The information relating to the JTAG/IEEE 1149.1-1990 state diagram, instructions, and boundary control register opcodes is common to each of the data sheets for the 'ABT8245, 'ABT8543, 'ABT8646, 'ABT8652, and 'ABT8952. Therefore, this information is only shown for the 'ABT8245. To obtain these descriptions for the JTAG Widebus™ products, please contact your local TI sales representative.

#### SN54ABT8245, SN74ABT8245 SCAN TEST DEVICES WITH OCTAL BUS TRANSCEIVERS

SCBS124A-D4505, AUGUST 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments SCOPE ™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74F245 and SN54/74ABT245 in the Normal Function Mode
- SCOPE ™ Instruction Set:
  - IEEE Standard 1149.1-1990 Required instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
     With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample inputs/Toggle Outputs
  - Binary Count From Outputs
- Even-Parity Opcodes
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPICIIB™ BICMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs

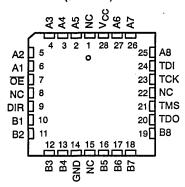
#### description

The SN54ABT8245 and SN74ABT8245 scan test devices with octal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54ABT8245...JT PACKAGE SN74ABT8245...DB OR DW PACKAGE (TOP VIEW)

DIR[ B1] B2[ B3] B4[ GND[ B5]	3 4 5 6 7	24 OE 23 A1 22 A2 21 A3 20 A4 19 A5 18 V <sub>CC</sub> 17 A6	
	-		
		18[] V <sub>CC</sub>	
В6Д	8		
В7[	9	16 🛮 A7	
ва[		15 🛛 A8	
TDO	11	14 🛛 TDI	
тмѕ[	12	13 TCK	

SN54ABT8245...FK PACKAGE (TOP VIEW)



NC - No internal connection

In the normal mode, these devices are functionally equivalent to the SN54/74F245 and SN54/74ABT245 octal bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable (OE) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

SCOPE and EPICIIB are trademarks of Texas instruments incorporated.



#### SN54ABT8245, SN74ABT8245 SCAN TEST DEVICES WITH OCTAL BUS TRANSCEIVERS

SCBS124A-D4505, AUGUST 1992-REVISED OCTOBER 1992

#### description (continued)

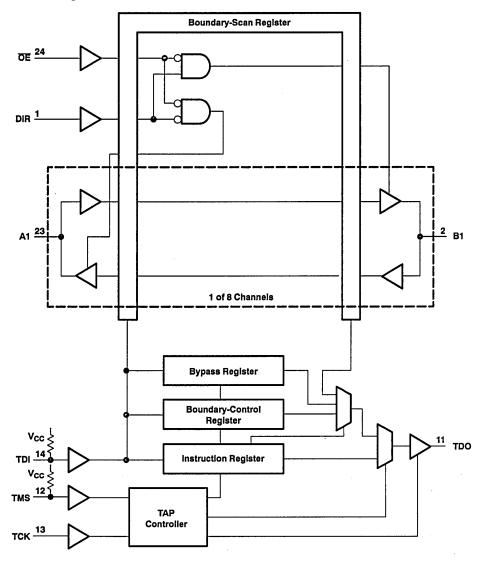
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8245 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74ABT8245 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

### FUNCTION TABLE (normal mode)

INP	UTS	OPERATION				
OE	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
н	X	Isolation				

#### functional block diagram



Pin numbers shown are for DB, DW, and JT packages.

# SN54ABT8245, SN74ABT8245 SCAN TEST DEVICES WITH OCTAL BUS TRANSCEIVERS SCBS124A-D4505, AUGUST 1992-REVISED OCTOBER 1992

**Terminal Functions** 

PIN NAME	DESCRIPTION
A1-A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1-B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
DIR	Normal-function direction-control input. See function table for normal-mode logic.
GND	Ground
ŌĒ	Normal-function output-enable input. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage

#### test architecture

Serial test information is conveyed by means of a 4-wire test bus, or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. NO TAG shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test data registers: a 36-bit boundary-scan register, an 11-bit boundary-control register, and a one-bit bypass register.

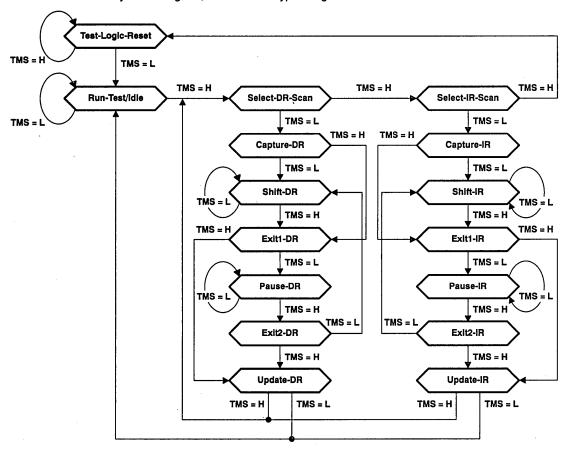


Figure 1. TAP Controller State Diagram



#### SN54ABT8245. SN74ABT8245 **SCAN TEST DEVICES** WITH OCTAL BUS TRANSCEIVERS SCBS124A-D4505, AUGUST 1992-REVISED OCTOBER 1992

#### state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in NO TAG and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register may be accessed at a time.

#### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction, Certain data registers may also be reset to their power-up values.

The state machine is constructed such that the TAP controller will return to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that will force it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8245, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0. The boundary-control register is reset to the binary value 0000000010, which selects the PSA test operation with no input masking.

#### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state may also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic may be actively running a test or may be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

#### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller will exit either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

#### Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register may capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

#### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.



#### state diagram description (continued)

#### Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

#### Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

#### Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

#### Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8245, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

#### Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

#### Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

#### Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

#### Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.



#### register overview

With the exception of the bypass register, any test register may be thought of as a serial shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

#### instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

NO TAG lists the instructions supported by the 'ABT8245. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction.

The instruction register order of scan is illustrated in Figure 2.

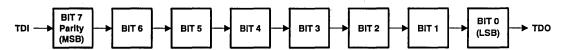


Figure 2. Instruction Register Order of Scan

#### data register description

#### boundary-scan register

The boundary-scan register (BSR) is 36 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, two BSCs for each normal-function I/O pin (one for input data and one for output data), and one BSC for each of the internally decoded output-enable signals (OEA and OEB). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR may change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0.

When external data is to be captured, the BSCs for signals OEA and OEB capture logic values determined by the following positive-logic equations: OEA =  $\overline{OE} \cdot \overline{DIR}$ , and OEB =  $\overline{OE} \cdot DIR$ . When data is to be applied externally, these BSCs control the drive state (active or high-impedance) of their respective outputs.

The boundary-scan register order of scan is from TDI through bits 35-0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
35	OEB	31	B8-I	23	B8-O	15	A8-I	7	A8-O
34	OEA	30	B7-I	22	B7-O	14	A7-I	6	A7-O
33	DIR	29	B6-I	21	B6-O	13	A6-I	5	A6-O
32	ŌĒ	28	B5-I	20	B5-O	12	A5-I	4	A5-O
	_	27	B4-I	19	B4-O	11	A4-I	3	A4-O
		26	B3-I	18	B3-O	10	A3-I	2	A3-O
	_	25	B2-I	17	B2-O	9	A2-I	1	A2-O
	i —	24	B1-l	16	B1-O	8	A1-I	0	A1-0

Table 1. Boundary-Scan Register Configuration

#### boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 4 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The boundary-control register order of scan is from TDI through bits 10-0 to TDO. NO TAG shows the boundary-control register bits and their associated test control signals.

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1		

**Table 2. Boundary-Control Register Configuration** 

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#### data register description (continued)

#### bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0.

The bypass register order of scan is illustrated in Figure 3.

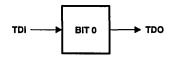


Figure 3. Bypass Register Order of Scan

**Table 3. Instruction Register Opcodes** 

BINARY CODE <sup>†</sup> BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary-scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary-scan	Normal
00000011	INTEST	Boundary scan	Boundary-scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary-scan	Normal
10001011	READBT	Boundary read	Boundary-scan	Test
00001100	CELLTST	Boundary self test	Boundary-scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary-control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary-control	Test
Ali others	BYPASS	Bypass scan	Bypass	Normal

<sup>&</sup>lt;sup>†</sup> Bit 7 is used to maintain even parity in the 8-bit instruction.

<sup>\*</sup> The BYPASS instruction is executed in lieu of a SCOPE" instruction that is not supported in the 'ABT8245.

#### instruction register opcode description

The instruction register opcodes are shown in NO TAG. The following descriptions detail the operation of each instruction.

#### boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

#### bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

#### sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

#### control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

#### control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

#### boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

#### boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

#### boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches may be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.



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#### instruction register opcode description (continued)

#### boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

#### boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

Table 4. Boundary-Control Register Opcodes

#### boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2-0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

It should be noted, in general, that while the control input BSCs (bits 35-32) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 35-34 of the BSR) do control the drive state (active or high-impedance) of the selected device output pins. It also should be noted that these BCR instructions are only valid when the device is operating in one direction of data flow (that is, OEA = OEB). Otherwise, the bypass instruction is operated.

#### PSA input masking

Bits 10-3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin A8 during A-to-B data flow or for device input pin B8 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in NO TAG. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.



#### sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shift register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK.

#### pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift register elements of the selected BSCs on each rising edge of TCK and then updated in the shadow latches and thereby applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 16-bit linear-feedback shift register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

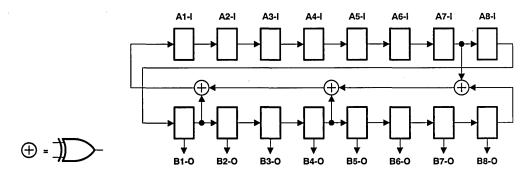


Figure 4. 16-Bit PRPG Configuration (OEA = 0, OEB = 1)

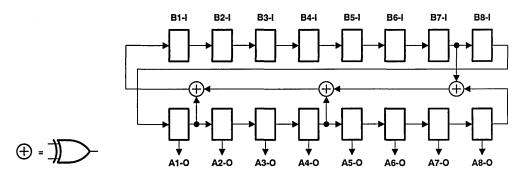


Figure 5. 16-Bit PRPG Configuration (OEA = 1, OEB = 0)

#### parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 16-bit parallel signature in the shift register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 16-bit linear-feedback shift register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

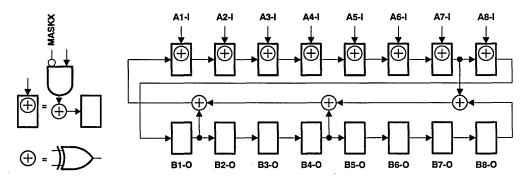


Figure 6. 16-Bit PSA Configuration (OEA = 0, OEB = 1)

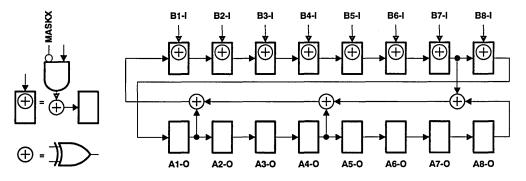


Figure 7. 16-Bit PSA Configuration (OEA = 1, OEB = 0)

#### simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 8-bit linear-feedback shift register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. Note that a seed value of all zeroes will not produce additional patterns.

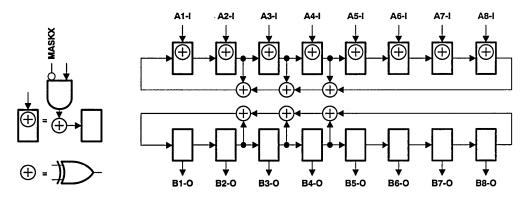


Figure 8. 8-Bit PSA/PRPG Configuration (OEA = 0, OEB = 1)

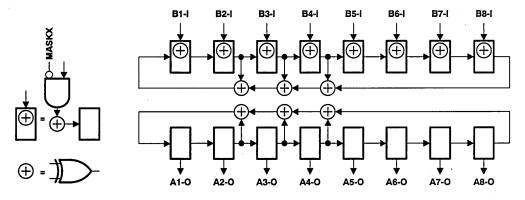


Figure 9. 8-Bit PSA/PRPG Configuration (OEA = 1, OEB = 0)

#### simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into an 8-bit parallel signature in the shift register elements of the selected input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and, thereby, applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift register elements of the selected output BSCs on each rising edge of TCK and then updated in the shadow latches and, thereby, applied to the associated device output pins on each falling edge of TCK. In addition, the shift register elements of the opposite output BSCs are used to count carries out of the selected output BSCs and, thereby, extend the count to 16 bits. Figures 10 and 11 illustrate the 8-bit linear-feedback shift register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

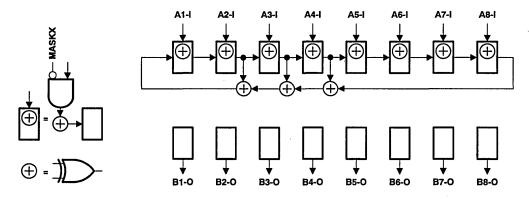


Figure 10. 8-Bit PSA/COUNT Configuration (OEA = 0, OEB = 1)

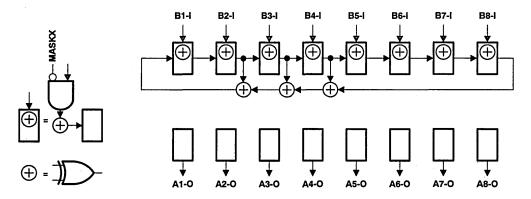


Figure 11. 8-Bit PSA/COUNT Configuration (OEA = 1, OEB = 0)

#### timing description

All test operations of the 'ABT8245 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in NO TAG) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in NO TAG. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active, and TDI is made valid, on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active, and TDI is made valid, on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19-20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

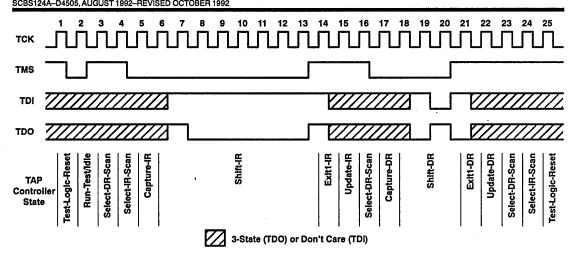


Figure 12. Timing Example

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (I/O ports) (see Note 1)	-0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT8245	96 mA
SN74ABT8245	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		SN54ABT8245		SN74ABT8245		UNIT
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5,5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2	80	2		٧
VIL	Low-level input voltage		<i>∰</i> 0.8	•	0.8	V
VI	Input voltage	0,4	∛ V <sub>CC</sub>	0	Vcc	٧
Іон	High-level output current	Ş	-24		-32	mA
loL	Low-level output current	ŞÕ	48		64	mA
Δt/Δν	Input transition rise or fall rate	, KF	10		10	ns/V
T <sub>A</sub>	Operating free-air temperature	ີ −55	125	-40	85	ů

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT8245		SN74ABT8245		UNIT
PARAMETER	16:	SI CONDINO	NS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
VIK	V <sub>CC</sub> = 4.5 V,	i V, I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			2.5		***********	2.5		2.5		
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m	A	2			2				· •
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -32 \text{ m}$	A	2‡					2		
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	V
	V <sub>CC</sub> = 5.5 V,		DIR, OE, TCK			±1		±1		±1	μА
. կ	V <sub>I</sub> = V <sub>CC</sub> or GND	V <sub>I</sub> = V <sub>CC</sub> or GND				±100		±,100		±100	μΑ
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub>	TDI, TMS			10		J 10		10	μΑ
l <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = GND	TDI, TMS			-160	بر	2~160		-160	μA
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	. A	50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	్ట్రా	-50		-50	μА
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 5.	5 V			±100	, O			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50	Q <sup>N</sup>	50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		0.9	2		2		2	
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		30	38		38		38	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	Ports	Outputs disabled		0.9	2		2		2	
Δlcc#	V <sub>CC</sub> = 5.5 V, One input at Other inputs at V <sub>CC</sub> or GND		3.4 V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V	·	A or B ports		10						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V	,	TDO		8						рF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			SN54ABT8245		SN74ABT8245		UNIT
			MIN	MIN MAX MIN	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
t <sub>w</sub>	Pulse duration	TCK high or low	5		5		ns
t <sub>su</sub>		A or B or DIR or OE before TCK†	5	40°	5		
	Setup time	TDI before TCK†	6	G.	6		ns
		TMS before TCK†	6 2	₹°	6		
t <sub>h</sub>		A or B or DIR or OE after TCK†	ρ,		0		
	Hold time	TDI after TCK†	100		0		ns
		TMS after TCK†	€00		0		
t <sub>d</sub>	Delay time	Power up to TCK†	<b>Q</b> 50		50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up	1		1		μs

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

 $<sup>^{\</sup>S}$  The parameters  $I_{\mbox{\scriptsize OZH}}$  and  $I_{\mbox{\scriptsize OZL}}$  include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

#### SN54ABT8245, SN74ABT8245 SCAN TEST DEVICES WITH OCTAL BUS TRANSCEIVERS SCBS124A-D4505, AUGUST 1992-REVISED OCTOBER 1992

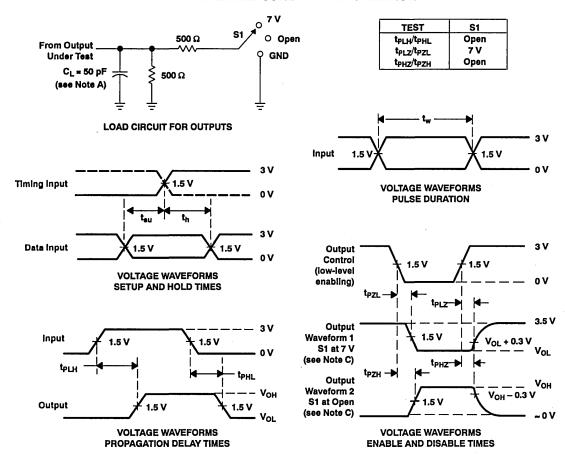
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8245		SN74ABT8245		UNIT
1	(	(000.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	7
t <sub>PLH</sub>	A or B	B or A	2	3.5	4.3	2	5.1	2	4.8	ns
t <sub>PHL</sub>			2	3.4	4.2	2 💸	5.5	2	5.1	
t <sub>PZH</sub>	ŌĒ	B or A	B or A 2.5 4.5	5.5	2.5	6.9	2.5	6.8	ns	
t <sub>PZL</sub>		BOIA	3	5.2	6	್ರೌ	7.6	3	7.5	110
t <sub>PHZ</sub>	ŌĔ	B or A	3	6.1	7.1	°,0,3	8.7	3	8.4	ns
t <sub>PLZ</sub>		]	3	5.5	6.6	<b>Q</b> 3	8	3	7.5	113

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8245		SN74ABT8245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	TCK		50	90		50		50		MHz
t <sub>PLH</sub>	тскі	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t <sub>PHL</sub>		A OF B	3	7.7	9	3	12	3	11.5	
t <sub>PLH</sub>	TCKĮ	TDO	2.5	4.3	5.5	2.5	7.7	2.5	6.5	ns
t <sub>PHL</sub>			2.5	4.2	5.5	2.5	<u>,5,7</u>	2.5	6.5	
t <sub>PZH</sub>	тскі	A or B	4.5	8.2	9.5	4.5	Q 12.5	4.5	12	ns
t <sub>PZL</sub>		AOIB	4.5	9	10.5	4.5		4.5	13	] "
<sup>t</sup> PZH	тскі	TDO	2.5	4.3	5.5	2,5	7	2.5	6.5	ns
t <sub>PZL</sub>		100	2.5	4.9	6	€2.5	7.5	2.5	7	115
t <sub>PHZ</sub>	TCKĮ	A or B	3.5	8.4	10.5	<b>⊘</b> 3.5	14	3.5	13.5	
t <sub>PLZ</sub>			3	8	10.5	3	13.5	3	13	ns
t <sub>PHZ</sub>	тскі	TCKĮ TDO	3	5.9	7	3	9	3	8.5	20
t <sub>PLZ</sub>			3	5	6.5	3	8	3	7.5	ns

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω, t₁ ≤ 2.5 ns, t₁ ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 13. Load Circuit and Voltage Waveforms

# SN54ABT8543, SN74ABT8543 SCAN TEST DEVICES WITH OCTAL REGISTERED BUS TRANSCEIVERS

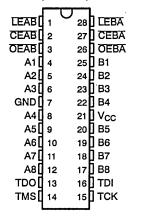
SCBS120A-D4509, AUGUST 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74F543 and SN54/74ABT543 in the Normal Function Mode
- SCOPE ™ Instruction Set:
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPICIIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs

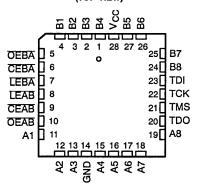
#### description

The SN54ABT8543 and SN74ABT8543 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54ABT8543 . . . JT PACKAGE SN74ABT8543 . . . DL OR DW PACKAGE (TOP VIEW)



SN54ABT8543...FK PACKAGE (TOP VIEW)



In the normal mode, these devices are functionally equivalent to the SN54/74F543 and SN54/74ABT543 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

Data flow in each direction is controlled by latch-enable (LEAB and LEBA), chip-enable (CEAB and CEBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB and CEAB are both low. When either LEAB or CEAB is high, the A data is latched. The B outputs are active when OEAB and CEAB are both low. When either OEAB or CEAB is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B but uses LEBA, CEBA, and OEBA.

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# SN54ABT8543, SN74ABT8543 SCAN TEST DEVICES WITH OCTAL REGISTERED BUS TRANSCEIVERS SCBS120A-D4509, AUGUST 1991-REVISED OCTOBER 1992

#### description (continued)

In the test mode, the normal operation of the SCOPE™ registered bus transceiver is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8543 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT8543 is characterized for operation from -40°C to 85°C.

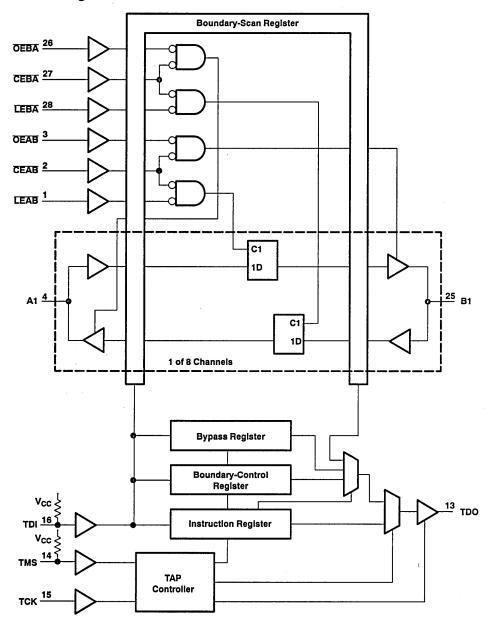
**FUNCTION TABLE<sup>†</sup>** (normal mode, each register)

	INPU		OUTPUT	
CEAB	OEAB	LEAB	Α	В
L	L	L	L	L
L	L	L	н	н
Ļ	L	Н	X	B₀ <sup>‡</sup> Z
L	Н	Х	X	z
Н	X	Х	X	z

<sup>†</sup> A-to-B data flow is shown. B-to-A data flow is similar but uses CEBA, OEBA, and LEBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

# functional block diagram



Pin numbers shown are for DL, DW, and JT packages.



#### **Terminal Functions**

PIN NAME	DESCRIPTION
A1-A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1-B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CEAB, CEBA	Normal-function chip-enable inputs. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch-enable inputs. See function table for normal-mode logic.
OEAB, OEBA	Normal-function output-enable inputs. See function table for normal-mode logic.
тск	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
тмѕ	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V <sub>CC</sub>	Supply voltage

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, VI (except I/O ports) (se	ee Note 1)	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (I/O ports) (see Note	1)	0.5 V to 5.5 V
Voltage range applied to any output in the hi	igh state or power-off state, VO	0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT8543	96 mA
	SN74ABT8543	128 mA
Input clamp current, $I_{IK}(V_I < 0)$		–18 mA
Output clamp current, $I_{OK}(V_O < 0)$		–50 mA

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

		SN54AE	T8543	SN74AB	LIAUT	
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5,5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2	8	2		٧
$V_{IL}$	Low-level input voltage		<i>‰</i> 0.8		0.8	V
VI	Input voltage	0,4	∛ V <sub>CC</sub>	0	Vcc	٧
1он	High-level output current	Ç	-24		-32	mA
loL	Low-level output current	Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Ş.E.	10		10	ns/V
TA	Operating free-air temperature	~55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



# SN54ABT8543, SN74ABT8543 **SCAN TEST DEVICES** WITH OCTAL REGISTERED BUS TRANSCEIVERS SCBS120A-D4509, AUGUST 1991-REVISED OCTOBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		T CONDITIO	vo	T	A = 25°0	;	SN54AE	T8543	SN74ABT8543		112117
PARAMETER	12:	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	5 V, I <sub>I</sub> = –18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	$V_{CC} = 5 \text{ V}$ , $I_{OH} = -3 \text{ mA}$			3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 m	A	2			2				v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	A	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			٧
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	v
ŀı			CE, LE, OE, TCK			±1		±1		±1	μА
	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		<b>£</b> 100		±100	
l <sub>iH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub>	TDI, TMS			10		₹ 10		10	μΑ
I <sub>I</sub> L	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = GND	TDI, TMS			-160	\ \h_{\text{``}}	-160		-160	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	Ş	50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				50	N.	-50		-50	μΑ
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_1$ or $V_0 \le 5$ .	5 V			±100	55			±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,		Outputs high		0.9	2		2		2	
Icc	l <sub>O</sub> = 0,	A or B ports	Outputs low		30	38		38		38	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	ports	Outputs disabled		0.9	2		2		2	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		10						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	V <sub>O</sub> = 2.5 V or 0.5 V TDO			8						рF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT8543, SN74ABT8543 **SCAN TEST DEVICES** WITH OCTAL REGISTERED BUS TRANSCEIVERS SCBS120A-D4509, AUGUST 1991-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 1)

			SN54ABT8543	SN74ABT8543	UNIT
			XAMO, NIM	MIN MAX	) ONII
tw	Pulse duration	LEAB or LEBA high or low	(4),(C),	3	ns
t <sub>su</sub>	Setup time	A before LEAB† or B before LEBA†	Q 34	3	ns
th	Hold time	A after LEAB† or B after LEBA†	0.5	0.5	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 1)

			SN54AB	T8543	SN74AB	T8543	UNIT
			MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	TCK	0	50	0	50	MHz
tw	Pulse duration	TCK high or low	5		5		ns
		A or B or CE or LE or OE before TCK†	5	Ţ,	5		
t <sub>su</sub>	Setup time	TDI before TCK†	6	67	6		ns `
		TMS before TCK↑	6 2	ŞC-	6		
		A or B or CE or LE or OE after TCK†	ρ		0		
t <sub>h</sub>	Hold time	TDI after TCK†	60		0		ns
		TMS after TCK†	್ದರ್		0		
t <sub>d</sub>	Delay time	Power up to TCK†	<b>4</b> 50		50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up	1		1		μs

# SN54ABT8543, SN74ABT8543 **SCAN TEST DEVICES** WITH OCTAL REGISTERED BUS TRANSCEIVERS SCBS120A-D4509, AUGUST 1991-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 1)

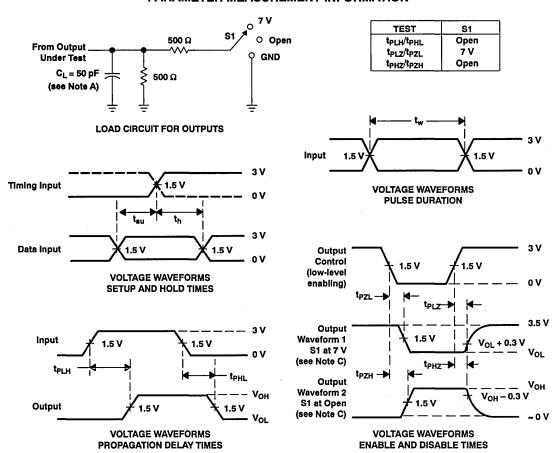
PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8543		SN74ABT8543	
	(IMPO1)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t <sub>PHL</sub>	AUID	BOLA	1.5	3.5	4.4	1.5	5.8	1.5	5.5	115
tрLH	CEAB or LEBA	B or A	2	4.7	5.6	2	,8,1	2	7.8	ns
<sup>‡</sup> PHL	LEAD OF LEDA	D 01 A	1.5	4.1	5	1.5	\$7.3	1.5	6.9	115
<sup>t</sup> PZH	CEAB or CEBA	B or A	2	4.2	5.2		& <sup>√</sup> 7.5	2	7.2	ns
t <sub>PZL</sub>	CEAD OF CEBA	BOIA	2	4.7	5.7	2/	8.4	2	8.3	113
tрzн	OEAB or OEBA	B or A	2	4.4	5.4	ॐ	6.7	2	6.5	ns
t <sub>PZL</sub>	OEAB OI OEBA	BOIA	2	5.2	6.2	\ <sup>2</sup> 2	7.6	2	7.5	l lis
t <sub>PHZ</sub>	CEAB or CEBA	B or A	2.5	5.8	6.8	₹ <sup>©</sup> 2.5	9.1	2.5	8.8	
<sup>†</sup> PLZ	CEAB OF CEBA	BOTA	2.5	5.3	6.3	2.5	8.7	2.5	8	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A	2	5.9	6.9	2	8.3	. 2	7.9	
t <sub>PLZ</sub>	OEAD OF OEBA	. DOFA	2	5.2	6.2	2	7.8	2	7.4	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8543		SN74ABT8543		
	( 01)	(001/01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>	TCK		50	90		50		50		MHz	
t <sub>PLH</sub>	TCK‡	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns	
t <sub>PHL</sub>	1014	7018	3	7.7	9	3	12	3	11.5	113	
tРLН	TCKĮ	TDO	2.5	4.3	5.5	2.5	,27	2.5	6.5	ns	
t <sub>PHL</sub>	TOR	150	2.5	4.2	5.5	2.5	_S∑ 7	2.5	6.5		
tрzн	TCKĮ	A or B	4.5	8.2	9.5	4.5	<b>₹12.5</b>	4.5	12	——Ins	
t <sub>PZL</sub>	1004	7018	4.5	9	10.5	4.5	13.5	4.5	13		
tpzH	TCKĮ	TDO	2.5	4.3	5.5	2,5′	7	2.5	6.5	ne	
t <sub>PZL</sub>	TOR	100	2.5	4.9	6	<b>2</b> .5	7.5	2.5	7	ns	
t <sub>PHZ</sub>	TCKI	A or B	3.5	8.4	10.5	© <sup>€</sup> 3.5	14	3.5	13.5	200	
t <sub>PLZ</sub>	TORT		3	8	10.5	3	13.5	3	13	ns	
t <sub>PHZ</sub>	TCK‡	TDO	3	5.9	7	3	9	3	8.5	ne	
t <sub>PLZ</sub>	TORT	1 100	3	5	6.5	3	8	3	7.5 ns		

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>r</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74F646 and SN54/74ABT646 in the Normal Function Mode
- SCOPE ™ Instruction Set:
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPICIIB™ BICMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs

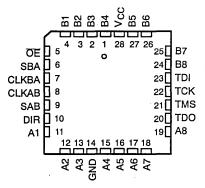
#### description

The SN54ABT8646 and SN74ABT8646 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54ABT8646 . . . JT PACKAGE SN74ABT8646 . . . DL OR DW PACKAGE (TOP VIEW)

1				ĺ
CLKAB[		<u> </u>	28	CLKBA
SAB[	2		27	] SBA
DIR[	3		26	) DE
A1 [	4		25	] B1
A2[	5		24	] B2
A3[			23	] B3
GND[	7		22	] B4
A4[			21	] v <sub>cc</sub>
A5[	9			] B5
A6[			19	] B6
A7[	11		18	] B7
A8[			17	] B8
TDO[	13		16	וסד [
TMS[	14		15	] тск
				,

SN54ABT8646 . . . FK PACKAGE (TOP VIEW)



In the normal mode, these devices are functionally equivalent to the SN54/74F646 and SN54/74ABT646 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

Transceiver function is controlled by output-enable ( $\overline{OE}$ ) and direction (DIR) inputs. When  $\overline{OE}$  is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When  $\overline{OE}$  is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

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#### description (continued)

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT8646.

In the test mode, the normal operation of the SCOPE<sup>™</sup> bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8646 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8646 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

		INP	INPUTS DATA I/O				A I/O	OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Х	Х	Ť	Х	Х	X	Input	Unspecified <sup>†</sup>	Store A, B unspecified†
X	X	X	1	X	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>
Н	Х	†	Î	х	X	Input	Input	Store A and B data
Н	Х	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L.	Х	Х	×	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	н	Output	Input disabled	Stored B data to A bus
L	Н	Х	X	L	Х	Input	Output	Real-time A data to B bus
L	Н	L	X	Н	Х	Input disabled	Output	Stored A data to B bus

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

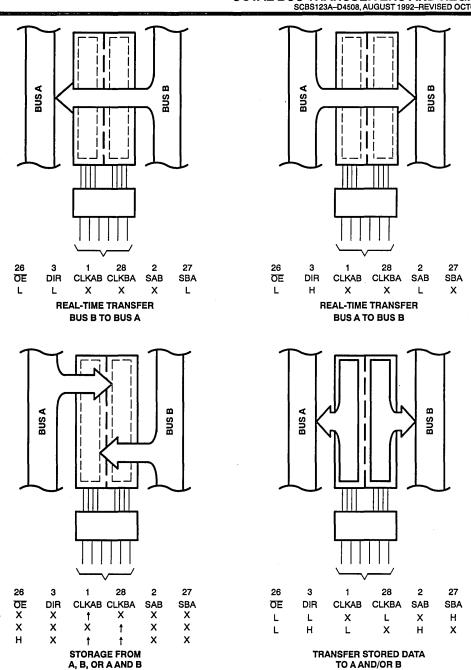
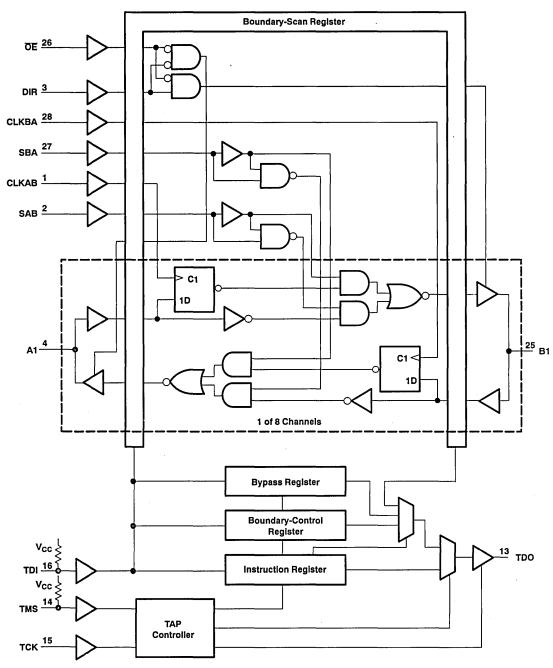


Figure 1. Bus-Management Functions

Pin numbers shown are for DL, DW, and JT packages.



### functional block diagram



Pin numbers shown are for DL, DW, and JT packages.



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#### **Terminal Functions**

PIN NAME	DESCRIPTION
A1-A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
DIR	Normal-function direction-control input. See function table for normal-mode logic.
GND	Ground
ŌĒ	Normal-function output-enable input. See function table for normal-mode logic.
SAB, SBA	Normal-function select inputs. See function table for normal-mode logic.
тск	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
тмѕ	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V <sub>cc</sub>	Supply voltage

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>		0.5 V to 7 V
Input voltage range, VI (except I/O ports) (se	ee Note 1)	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (I/O ports) (see Note	1)	-0.5 V to 5.5 V
Voltage range applied to any output in the hi	gh state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT8646	96 mA
	SN74ABT8646	128 mA
Input clamp current, $I_{iK}$ ( $V_i < 0$ )		–18 mA
Storage temperature range		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		SN54AE	T8646	SN74AB	UNIT	
ı		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5,5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2	34	2		V
V <sub>IL</sub>	Low-level input voltage		<i>∰</i> 0.8		0.8	V
VI	Input voltage	0,4		0	Vcc	V
Гон	High-level output current	Ç	-24		-32	mA
loL	Low-level output current	2	48		64	mA
Δt/Δv	Input transition rise or fall rate	S. S. S. S. S. S. S. S. S. S. S. S. S. S	10		10	ns/V
TA	Operating free-air temperature	*-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		T CONDITIO	NO	Т	A = 25°0	;	SN54AE	T8646	SN74AB	T8646	UNIT
PARAMETER	153	ST CONDITIO	NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	וואט
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$		3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m	A	2			2				\ <b>V</b>
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	A	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	· ·
· II	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		CLK, DIR, ŌĒ, S, TCK			±1	i	<u>*</u> 1		±1	μА
	AI = ACC OL GIAD		A or B ports			±100		<u>.</u> ≇100		±100	
Iн	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub>	TDI, TMS			10		¿¥ 10		10	μΑ
I₁∟	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = GND	TDI, TMS			-160	À	-160		-160	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	Š	50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	ి -	-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 5.	5 V			±100	55			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μA
lo <sup>1</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high		0.9	2		2		2	
Icc	I <sub>O</sub> = 0,	ports	Outputs low		30	38		38		38	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.9	2		2		2	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>CC</sub>	One input at or GND	3.4 V,			1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		10						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		TDO		8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

			SN54ABT8646		SN74AE	UNIT	
			MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	0.4	<del>్స్ 100</del>	0	100	MHz
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low	(4)	<u> </u>	3		ns
t <sub>su</sub>	Setup time	A before CLKAB† or B before CLKBA†	2450		4.5		ns
th	Hold time	A after CLKAB† or B after CLKBA†	<b>V</b> 0		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

			SN54AB	T8646	SN74AB	T8646	
			MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
tw	Pulse duration	TCK high or low	5		5		ns
		A, B, CLK, DIR, OE, or S before TCK†	5	Ú,	5		
t <sub>su</sub>	Setup time	TDI before TCK↑	6	G.	6		ns
		TMS before TCK↑	6 &	Ç.	, 6		
		A, B, CLK, DIR, OE, or S after TCK†	95		0		
th	Hold time	TDI after TCK†	50		0		ns
		TMS after TCK†	Ω0		0		
t <sub>d</sub>	Delay time	Power up to TCK†	₹ 50		50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up	1		1		μs

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

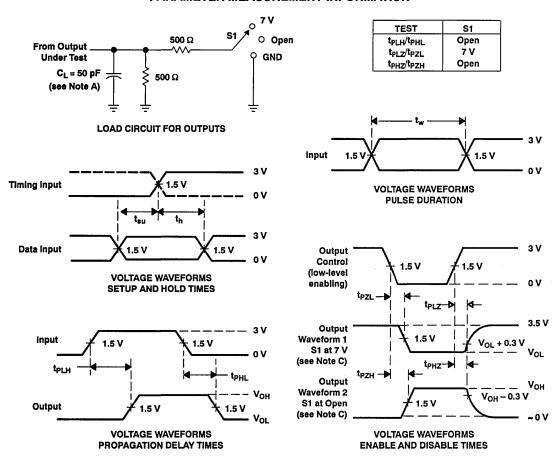
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8646		SN74ABT8646	
	( 5.)	(0011 01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLKAB or CLKBA		100	130		100		100		MHz
t <sub>PLH</sub>	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ns
t <sub>PHL</sub>	7018		2	3.5	4.4	2	5.8	2	5,5	115
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	3	4.4	5.3	3	6.3	3	6	
t <sub>PHL</sub>		BOIA	2.5	4.3	5.2	2.5	,6.7	2.5	6.2	ns
t <sub>PLH</sub>	SAB or SBA	B or A	2	4.8	6	2	<b>\$7.5</b>	2	7.3	ns
t <sub>PHL</sub>			2	4.7	5.9	2	7.8	2	7.4	
<sup>t</sup> PZH	DIR	B or A	2.5	4.4	5.3	2.5	6.6	2.5	6.5	
t <sub>PZL</sub>	1 DIN	D OF A	3	4.8	6.2	37	7.3	3	7.1	ns
t <sub>PZH</sub>	ŌĒ	B or A	2.5	4.4	5.4	€2.5	6.7	2.5	6.5	ns
t <sub>PZL</sub>	]	BUIA	3	5.2	6.2	₫ <sup>©</sup> 3	7.6	3	7.5	115
t <sub>PHZ</sub>	DIB	B or A	3	6	7	3	8.9	3	8.6	
t <sub>PLZ</sub>	——— DIR I		3	5.2	6.2	3	8.1	3	7.9	ns
t <sub>PHZ</sub>		B or A	3	5.9	6.9	3	8.3	3	7.9	
t <sub>PLZ</sub>	]	D OF A	3	5.2	6.2	3	7.8	3	7.4	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54ABT8646		SN74ABT8646		UNIT
	<b>(</b>	(0011.01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	TCK		50	90		50		50		MHz
t <sub>PLH</sub>	TCK1	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
t <sub>PHL</sub>	10/4		3	7.7	9	3	12	3	11.5	115
t <sub>PLH</sub>	TCKĮ	тро	2.5	4.3	5.5	2.5	,37	2.5	6.5	ns
tpHL	t <sub>PHL</sub>	100	2.5	4.2	5.5	2.5	, S* 7	2.5	6.5	13
t <sub>PZH</sub>	TCKĮ	A or B	4.5	8.2	9.5	4.5	<b>⊘</b> 12.5	4.5	12	ns
t <sub>PZL</sub>	1014	AOIB	4.5	9	10.5	4.5	13.5	4.5	13	115
tpzH	TCKI	TDO	2.5	4.3	5.5	2,5	7	2.5	6.5	ns
t <sub>PZL</sub>	iont	100	2.5	4.9	6	€2.5	7.5	2.5	7	115
t <sub>PHZ</sub>	TCKĮ	A or B	3.5	8.4	10.5	₫ <sup>≪</sup> 3.5	14	3.5	13.5	no
t <sub>PLZ</sub>	ION	A OF B	3	8	10.5	3	13.5	3	13	ns
t <sub>PHZ</sub>	TCKĮ	TDO	3	5.9	7	3	9	3	8.5	
t <sub>PLZ</sub>	1004		3	5	6.5	3	8	3	7.5	ns

SCBS123A-D4508, AUGUST 1992-REVISED OCTOBER 1992

### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

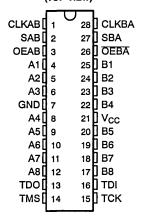
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- Members of the Texas Instruments
   SCOPE™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74F652 and SN54/74ABT652 in the Normal Function Mode
- SCOPE ™ Instruction Set:
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPICIIB™ BICMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs

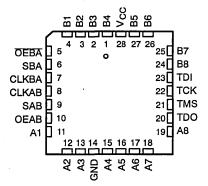
#### description

The SN54ABT8652 and SN74ABT8652 scan test devices with octal bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54ABT8652...JT PACKAGE SN74ABT8652...DL OR DW PACKAGE (TOP VIEW)



SN54ABT8652...FK PACKAGE (TOP VIEW)



In the normal mode, these devices are functionally equivalent to the SN54/74F652 and SN54/74ABT652 octal bus transceivers and registers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers and registers.

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#### description (continued)

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and OEBA inputs. Since the OEBA input is active-low, the A outputs are active when OEBA is low and are in the high-impedance state when OEBA is high. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT8652.

In the test mode, the normal operation of the SCOPE<sup>™</sup> bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8652 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8652 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

INPUTS						DAT	A I/O	OPERATION OR FUNCTION
OEAB OEBA		CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	L	L	Х	Х	Input disabled	Input disabled	Isolation
L	Н	<b>†</b>	1	X	X	Input	Input	Store A and B data
X	Н	<b>†</b>	L	X	X	Input	Unspecified <sup>†</sup>	Store A, hold B
Н	Н	<b>†</b>	Ť	X <sup>‡</sup>	X	Input	Output	Store A in both registers
L	X	L	<b>†</b>	Х	Х	Unspecified <sup>†</sup>	Input	Hold A, store B
L	L	<b>†</b>	<b>↑</b>	X	X <sup>‡</sup>	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input .	Real-time B data to A bus
L	L	X	L	X	Н	Output	Input	Stored B data to A bus
Н	Н	X	X	L	X	Input	Output	Real-time A data to B bus
н	Н	L	X	н	X	Input	Output	Stored A data to B bus
Н	L	L	L	н	н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

<sup>&</sup>lt;sup>‡</sup> Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.

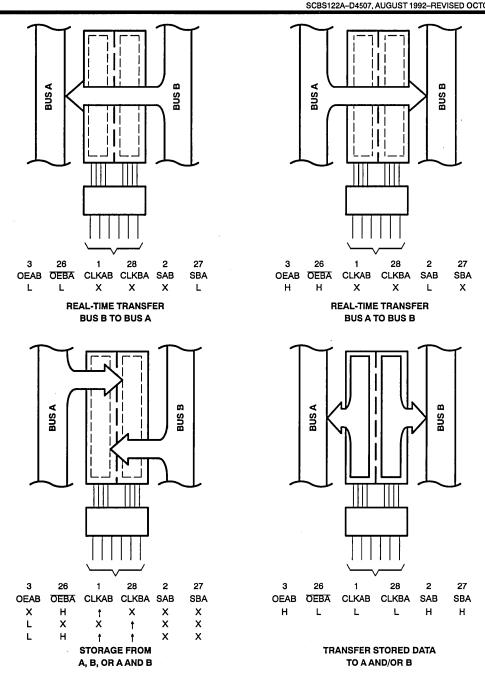


Figure 1. Bus-Management Functions

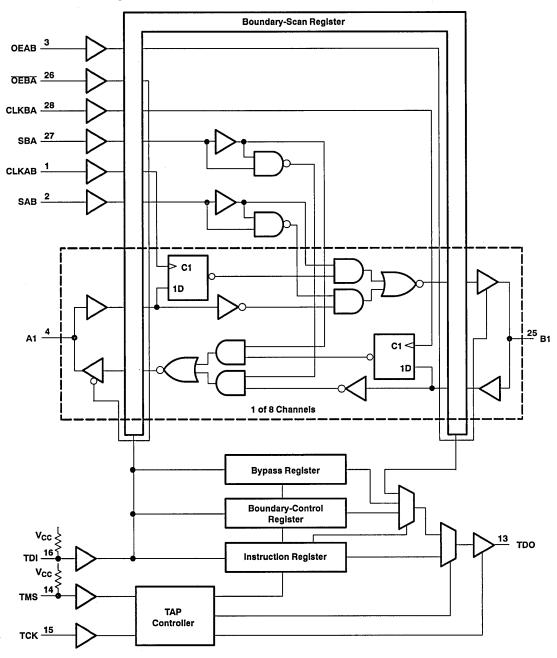
Pin numbers shown are for DL, DW, and JT packages.



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SCBS122A-D4507, AUGUST 1992-REVISED OCTOBER 1992

# functional block diagram



Pin numbers shown are for DL, DW, and JT packages.



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#### **Terminal Functions**

PIN NAME	DESCRIPTION
A1-A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1-B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
OEAB, OEBA	Normal-function output-enable inputs. See function table for normal-mode logic.
SAB, SBA	Normal-function select inputs. See function table for normal-mode logic.
тск	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V <sub>CC</sub>	Supply voltage

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Input voltage range, V <sub>I</sub> (I/O ports) (see Note 1)	to 5.5 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> 0.5 V	to 5.5 V
Current into any output in the low state, Io: SN54ABT8652	. 96 mA
SN74ABT8652	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	-50 mA
Storage temperature range ——65°C t	to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		SN54AB	T8652	SN74AB	T8652	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5,5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2	.59	2		٧
V <sub>IL</sub>	Low-level input voltage	,	<i>∰</i> 0.8		0.8	٧
VI	Input voltage	0,4	V <sub>CC</sub>	0	Vcc	٧
Іон	High-level output current	ŞÜ	-24		-32	mA
loL	Low-level output current	ŞĬ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Æ	10		10	ns/V
TA	Operating free-air temperature	ື−55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		T CONDITIO	NIC .	T	A = 25°0	5	SN54AE	T8652	SN74AB	T8652	UNIT
PARAMETER	'E	ST CONDITIO	)NS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 m/	4	2.5			2.5		2.5		
W.	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 m/	4	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24 m	nA	2			2				, v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 n	nA .	2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	<b>V</b>
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,		CLK, OEAB, OEBA, S, TCK			±1		<u>*</u> 1		±1	μΑ
•	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		₹100		±100	
I <sub>tH</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = V <sub>CC</sub>	TDI, TMS			10		<b>₹</b> 10		10	μА
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = GND	TDI, TMS			-160	٨	-160		-160	μΑ
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	39	50		50	μА
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	•			-50	l ô'	-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 5	.5 V			±100	8			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>1</sup>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high		0.9	2		2		2	
Icc	l <sub>O</sub> = 0,	ports	Outputs low		30	38		38		38	mA
	$V_I = V_{CC}$ or GND	Porto	Outputs disabled		0.9	2		2		2	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>CC</sub>	One input a	t 3.4 V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	,	A or B ports		10						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V	,	TDO		8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT8652, SN74ABT8652 SCAN TEST DEVICES WITH OCTAL BUS TRANSCEIVERS AND REGISTERS SCBS122A-D4507, AUGUST 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

			SN54ABT8652	SN74AE	UNIT	
1			MIN MAX	MIN	MAX	0.411
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	0 , 0 , 100	0	100	MHz
tw	Pulse duration	CLKAB or CLKBA high or low	(4).(C).	3		ns
t <sub>su</sub>	Setup time	A before CLKAB† or B before CLKBA†	Q*4.5(**	4.5		ns
th	Hold time	A after CLKAB† or B after CLKBA†	₹0	0	, , ,	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

			SN54AE	T8652	SN74AB	T8652	LIMIT
			MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency	TCK	0	50	0	50	MHz
t <sub>w</sub>	Pulse duration	TCK high or low	5	``	5		ns
		A, B, CLK, OEAB, OEBA, or S before TCK†	5	W	5		
t <sub>su</sub>	Setup time	TDI before TCK†	6	<i>167</i>	6		ns
i		TMS before TCK†	6 ¿	\$C*	6		
		A, B, CLK, OEAB, OEBA, or S after TCK†	ρ,·		0		
t <sub>h</sub>	Hold time	TDI after TCK†	30		0		ns
		TMS after TCK†	€00		0		
t <sub>d</sub>	Delay time	Power up to TCK†	<b>Q</b> 50		50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up	1	•	1		μs

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 2)

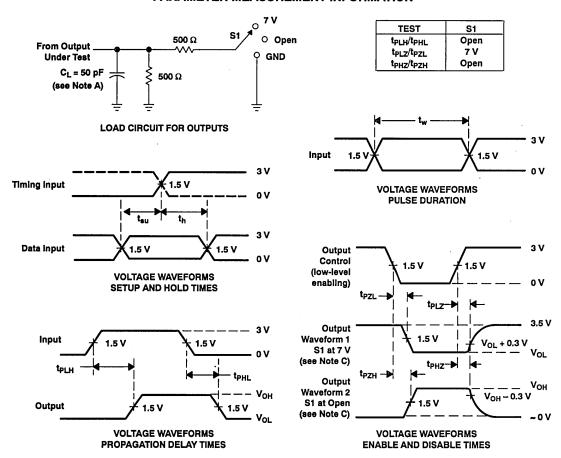
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8652		SN74ABT8652		UNIT	
	( 0.)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>	CLKAB or CLKBA		100	130		100		100		MHz	
t <sub>PLH</sub>	A or B	B or A	2	3.7	4.5	2	5.5	2	5.2	ne	
t <sub>PHL</sub>	AUIB	BUIA	1.5	3.5	4.4	1.5	,5,8	1.5	5.5	ns	
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	2.5	4.4	5.3	2.5	<b>£6.3</b>	2.5	6	ns	
tpHL	CLIVAB OF CLIVBA		2.5	4.3	5.2	2.5	<b>⊘</b> ₹ 6.7	2.5	6.2		
t <sub>PLH</sub>	SAB or SBA	B or A	2	4.8	6	2,	7.5	2	7.3	ns	
t <sub>PHL</sub>	SAD OF SDA	BUIA	2	4.7	5.9	ॐ	7.8	2	7.4	115	
t <sub>PZH</sub>	OEAB or OEBA	D or A	2	4.4	5.4	్ <sup>2</sup> 2	6.7	2	6.5		
t <sub>PZL</sub>	OEAB OF OEBA	B or A	2	5.2	6.2	o <sup>(C)</sup> 2	7.6	2	7.5	ns	
t <sub>PHZ</sub>	OEAB or OEBA	P or A	2	5.9	6.9	2	8.3	2	7.9		
t <sub>PLZ</sub>	) OEAD OF OEBA	B or A	2	5.2	6.2	2	7.8	2	7.4	ns	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8652		SN74ABT8652	
		(555.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	TCK		50	90		50		50		MHz
t <sub>PLH</sub>	TCKĮ	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ne
t <sub>PHL</sub>	10/4	Aorb	3	7.7	9	3	12	3	11.5	ns
t <sub>PLH</sub>	TCKĮ	TDO	2.5	4.3	5.5	2.5	7.7	2.5	6.5	ns
t <sub>PHL</sub>	1014	100	2.5	4.2	5.5	2.5	<b>~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~</b>	2.5	6.5	113
t <sub>PZH</sub>	TCKĮ	A or B	4.5	8.2	9.5	4.5	<2 <sup>√</sup> 12.5	4.5	12	ns
t <sub>PZL</sub>	iont	Aorb	4.5	9	10.5	4.5	13.5	4.5	13	] "
t <sub>PZH</sub>	TCKĮ	TDO	2.5	4.3	5.5	2,5	7	2.5	6.5	
t <sub>PZL</sub>	1004	100	2.5	4.9	6	<b>2</b> .5	7.5	2.5	7	ns
t <sub>PHZ</sub>	TCKĮ	A or B	3.5	8.4	10.5	₹3.5	14	3.5	13.5	no
t <sub>PLZ</sub>	ION	A OF B	3	8	10.5	3	13.5	3	13	ns
t <sub>PHZ</sub>	TCKĮ	TDO	3	5.9	7	3	9	3 .	8.5	
t <sub>PLZ</sub>	1004	100	3	5	6.5	3	8	3	7.5	ns

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### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{<}$  10 MHz,  $Z_{0}$  = 50  $\Omega$ ,  $t_{f}$   $_{<}$  2.5 ns,  $t_{f}$   $_{<}$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

# SN54ABT8952, SN74ABT8952 SCAN TEST DEVICES WITH OCTAL REGISTERED BUS TRANSCEIVERS

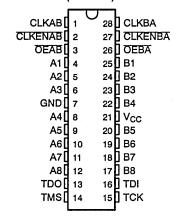
SCBS121A-D4506, AUGUST 1992-REVISED OCTOBER 1992

- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74BCT2952 and SN54/74ABT2952 in the Normal Function Mode
- SCOPE ™ Instruction Set:
  - IEEE Standard 1149.1-1990 Required instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Even-Parity Opcodes
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPICIIB™ BICMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs

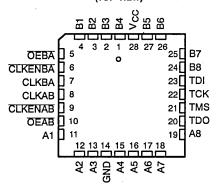
#### description

The SN54ABT8952 and SN74ABT8952 scan test devices with octal registered bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54ABT8952 . . . JT PACKAGE SN74ABT8952 . . . DL OR DW PACKAGE (TOP VIEW)



SN54ABT8952...FK PACKAGE (TOP VIEW)



In the normal mode, these devices are functionally equivalent to the SN54/74BCT2952 and SN54/74ABT2952 octal registered bus transceivers. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal registered bus transceivers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), clock-enable (CLKENAB and CLKENBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, A-bus data is stored in the associated registers on the low-to-high transition of CLKAB provided that CLKENAB is low. Otherwise, if CLKENAB is high or CLKAB remains at a static low or high level, the register contents are not changed. When OEAB is low, the B outputs are active. When OEAB is high, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B but uses CLKBA. CLKENBA, and OEBA.

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# SN54ABT8952, SN74ABT8952 SCAN TEST DEVICES WITH OCTAL REGISTERED BUS TRANSCEIVERS

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### description (continued)

In the test mode, the normal operation of the SCOPE™ registered bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations as described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

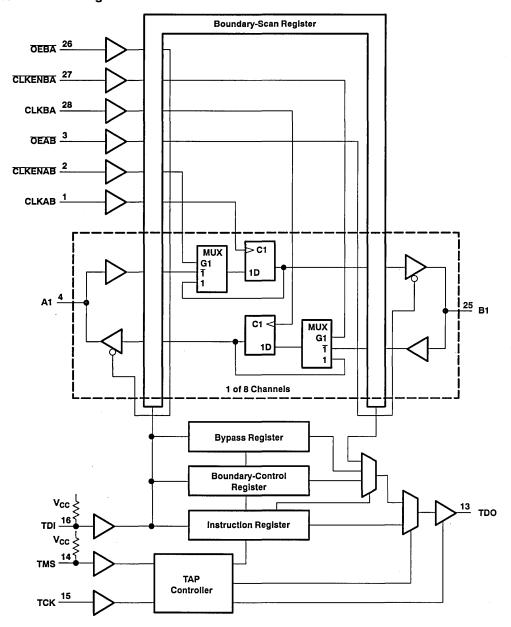
The SN54ABT8952 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN74ABT8952 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

	INPU	TS		OUTPUT
OEAB	CLKENAB	CLKAB	Α	В
L	L	<b>†</b>	L	L
L	L	Ť	Н	н
L	Н	X	X	B <sub>0</sub>
l L	Х	L	X	B <sub>0</sub>
н	Х	Х	X	z

<sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses OEBA, CLKENBA, and CLKBA.

### functional block diagram



Pin numbers shown are for DL, DW, and JT packages.



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#### **Terminal Functions**

PIN NAME	DESCRIPTION
A1-A8	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1-B8	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
CLKENAB, CLKENBA	Normal-function clock-enable inputs. See function table for normal-mode logic.
GND	Ground
OEAB, OEBA	Normal-function output-enable inputs. See function table for normal-mode logic.
тск	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
тмѕ	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V <sub>CC</sub>	Supply voltage

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (I/O ports) (see Note 1)	. −0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT8952	96 mA
SN74ABT8952	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions (see Note 2)

		SN54AE	T8952	SN74AB	T8952	UNIT
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5,5	4.5	5.5	V
VIH	High-level input voltage	2		2		٧
ViL	Low-level input voltage		<i>ķ</i> ./ 0.8		0.8	V
Vi	Input voltage	0,<	∛ V <sub>CC</sub>	0	Vcc	V
Іон	High-level output current	Ç	-24		-32	mA
loL	Low-level output current	ŞŸ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Q.	10		10	ns/V
TA	Operating free-air temperature	~55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			7	A = 25°0	;	SN54AB	T8952	SN74ABT8952		
PARAMETER	'5	SI CONDIIIO	NS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 mA				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -3 \text{ m/s}$	· ·	2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = - 3 m/	\	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,						2				v
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32 m	A	2 <sup>‡</sup>					2		
V	V <sub>CC</sub> = 4.5 V,	1 <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	· •
1 <sub>1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		CLK, CLKEN, OE, TCK			±1		,±1		±1	μА
	AI = ACC OLGIND		A or B ports		-	±100		±100		±100	
ItH	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub>	TDI, TMS			10		₹ 10		10	μΑ
l <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = GND	TDI, TMS			-160	, a	-160		-160	μА
lozh <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	3	50		50	μΑ
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50	l ô'	-50		-50	μΑ
loff	V <sub>CC</sub> = 0,	$V_1$ or $V_0 \le 5$ .	5 V			±100	8			±100	μΑ
I <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	180	50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high		0.9	2		2		2	
Icc	I <sub>O</sub> = 0,	ports	Outputs low		30	38		38		38	mA
	$V_i = V_{CC}$ or GND	Ports	Outputs disabled		0.9	2		2		2	
Δl <sub>CC</sub> #	$V_{CC} = 5.5 \text{ V},$ Other inputs at $V_{CC}$	One input at or GND	3.4 V,			1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		10						pF
Co	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	,	TDO		8						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

# SN54ABT8952, SN74ABT8952 SCAN TEST DEVICES

# WITH OCTAL REGISTERED BUS TRANSCEIVERS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 1)

			SN54AB	T8952	SN74AE	11117		
			MIN	MAX	MIN	MAX	UNIT	
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	0.	<i>₹</i> 2,100	0	100	MHz	
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low	3,0	•	3		ns	
	0-1	A before CLKAB† or B before CLKBA†	4.5 4.5					
<sup>T</sup> su	Setup time	CLKEN before CLK†	4)5		4.5		ns	
	Hald time	A after CLKAB† or B after CLKBA†	& 0		0			
th	Hold time	CLKEN after CLK†	₹ 0		0		ns	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 1)

			SN54AB	T8952	SN74AB	T8952	
			MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
t <sub>w</sub>	Pulse duration	TCK high or low	5	4	5		ns
	****	A, B, CLK, CLKEN, or OE before TCK†	5	N.	5		
t <sub>su</sub>	Setup time	TDI before TCK†	6 ,	39	6		ns
		TMS before TCK†	6, 3		6		
		A, B, CLK, CLKEN, or OE after TCK†	, Q)		0		
th	Hold time	TDI after TCK†	ξ,0		0		ns
		TMS after TCK†	₹ 0		0		
t <sub>d</sub>	Delay time	Power up to TCK†	50		50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up	1		1		μs

# SN54ABT8952, SN74ABT8952 **SCAN TEST DEVICES** WITH OCTAL REGISTERED BUS TRANSCEIVERS SCBS121A-D4506, AUGUST 1992-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 1)

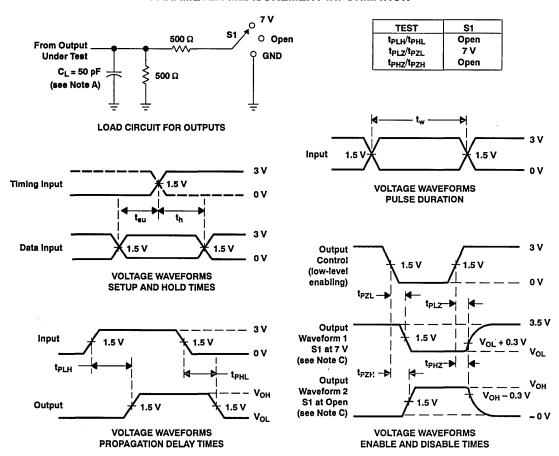
PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			T8952	SN74ABT8952		UNIT
	( 5.)	(656.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLK	A or B	100	130		100	84	100		MHz
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	3	4.6	5.4	3 ,	<b>4</b> 6.5	3	6.3	ns
t <sub>PHL</sub>	CLIVAB OI CLIVBA		2.5	3.8	4.6	2.5,	5.5	2.5	5.3	] "
t <sub>PZH</sub>	OEAB or OEBA	B or A	2	4.1	4.9	ري.	5.9	2	5.8	ns
t <sub>PZL</sub>	OEAB OI OEBA	B or A	2.5	4.7	5.5	<b>2</b> 25	7.1	2.5	6.9	113
t <sub>PHZ</sub>	OEAB or OEBA	B or A	2.5	5.3	6.1	€°2.5	7.5	2.5	7.3	ns
t <sub>PLZ</sub>	CEAB OF CEBA		3	4.5	5.3	3	6.3	3	6.1	115

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT8952		SN74ABT8952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	TCK		50	90		50		50		MHz
t <sub>PLH</sub>	TCK.	A or B	3.5	8	9.5	3.5	12.5	3.5	12	ns
tpHL			3	7.7	9	3	<u>, 1</u> 2	3	11.5	
t <sub>PLH</sub>	TCK	TDO	2.5	4.3	5.5	2.5	₹ 7	2.5	6.5	ns
t <sub>PHL</sub>			2.5	4.2	5.5	2.5	<b>⊘</b> 7	2.5	6.5	
t <sub>PZH</sub>	TCK.	A or B	4.5	8.2	9.5	4.5	12.5	4.5	12	ns
t <sub>PZL</sub>			4.5	9	10.5	4:5	13.5	4.5	13	
t <sub>PZH</sub>	TCK.	TDO	2.5	4.3	5.5	<b>Č</b> 2.5	7	2.5	6.5	ns
t <sub>PZL</sub>			2.5	4.9	6	¿ <sup>₹</sup> 2.5	7.5	2.5	7	
t <sub>PHZ</sub>	TCK‡	A or B	3.5	8.4	10.5	3.5	14	3.5	13.5	ns
t <sub>PLZ</sub>			3	8	10.5	3	13.5	3	13	
t <sub>PHZ</sub>	TCK.	TDO	3	5.9	7	3	9	3	8.5	ns
t <sub>PLZ</sub>			3	5	6.5	3	8	3	7.5	

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns,
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN54ABT18245, SN74ABT18245 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS

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- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- SCOPE ™ Instruction Set
  - IEEE Standard 1149.1-1990-Required Instructions and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation
     From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### description

The SN54ABT18245 and SN74ABT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54ABT18245... WD PACKAGE SN74ABT18245... DL PACKAGE (TOP VIEW)

	$\overline{}$		
1DIR[	<sub>1</sub>	56	] 10E
1B1[	2	55	] 1A1
1B2[	3	54	] 1A2
GND[	4	53	] GND
1B3[	5	52	] 1A3
1B4[	6	51	] 1A4
V <sub>CC</sub> [	7	50	] v <sub>cc</sub>
1B5[	8	49	] 1A5
1B6[	9	48	] 1A6
1B7[	10	47	] 1A7
GND[	11	46	] GND
1B8[	12	45	1A8
1B9[	13	44	1A9
2B1 [	14	43	] 2A1
2B2[	15	42	] 2A2
2B3[	16	41	2A3
2B4[	17	40	] 2A4
GND[	18	39	] GND
2B5[	19	38	] 2A5
2B6[	20	37	2A6
2B7[	21	36	] 2A7
v <sub>cc</sub> [	22	35	] v <sub>cc</sub>
2B8[	23	34	2A8
2B9[	24	33	2A9
GND[	25	32	] GND
2DIR[	26	31	20E
TDO[	27	30	] TDI
TMS[	28	29	] тск

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable (OE) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable (OE) can be used to disable the device so that the buses are effectively isolated.

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

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#### SN54ABT18245, SN74ABT18245 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS SCBS110A-AUGUST 1992-REVISED OCTOBER 1992

# description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

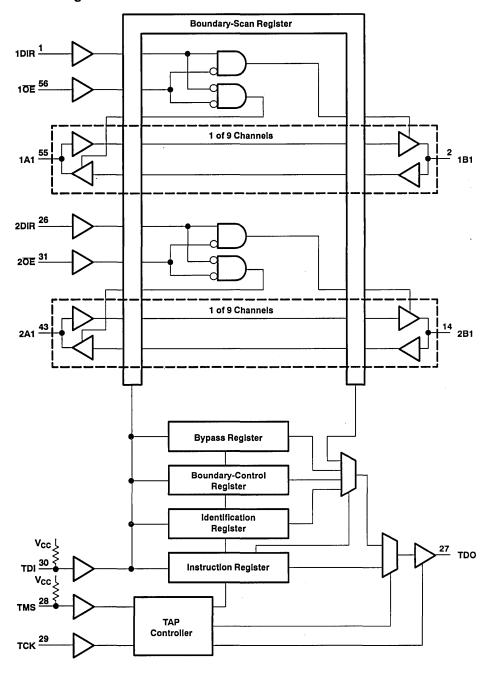
The SN74ABT18245 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT18245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (normal mode, each 9-bit section)

		,				
INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	X	Isolation				

#### functional block diagram





#### SN54ABT18245, SN74ABT18245 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS SCB5110A-AUGUST 1992-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

			•	
Supply voltage range, V <sub>CC</sub>				0.5 V to 7 V
Input voltage range, VI (except I/O ports) (se	ee Note 1)			0.5 V to 7 V
Input voltage range, VI (I/O ports) (see Note	: 1)			-0.5 V to 5.5 V
Voltage range applied to any output in the h	igh state or power	-off state, V <sub>O</sub>		-0.5 V to 5.5 V
Current into any output in the low state, Io:	SN54ABT18245			96 mA
	SN74ABT18245			128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )				–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)				–50 mA
Maximum package power dissipation at T <sub>A</sub> :	= 55°C (in still air)	(see Note 2)		950 mW
Storage temperature range				-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		SN54AE	T18245	SN74ABT18245		
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		8.0	V
VI	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24	[	-32	mA
loL	Low-level output current		48	ľ	64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> For the SN74ABT18245 (DL package), the power derating factor for ambient temperatures greater than 55°C is -11.3 mW/°C.

# SN54ABT18245, SN74ABT18245 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	750	CONDITION	0110	T	A = 25°0	;	SN54AB1	T18245	SN74AB1	18245	UNIT
PARAMETER	les:	CONDITION	UNS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 m	Α			-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3	mA	2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3		mA	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 24	# mA	2			2				· ·
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32	2 mA	2‡					2		
V-	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 r		nΑ			0.55		`0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 n	nA			0.55‡				0.55	, v
t.	V <sub>CC</sub> = 5.5 V,		DIR, OE, TCK			±1		±1		±1	
1 <sub>1</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΑ
1 <sub>IH</sub>	$V_{CC} = 5.5 \text{ V, } V_I = V_{CC}$		TDI,TMS			10		10	İ	10	μА
l <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND TDI,TMS					-160		-160		-160	μА
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.7	V			50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5	V			-50		-50		-50	μΑ
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤	: 5.5 V			±100				±100	μΑ
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5	5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>0</sub> = 2.5 \	/	-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high			4		4		4	
lcc	l <sub>O</sub> = 0,	ports	Outputs low			80		80		80	mA
	$V_I = V_{CC}$ or GND	Ports	Outputs disabled			4		4		4	
Δlcc#	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		-		1.5		1.5		1.5	mA	
Ci	V <sub>1</sub> = 2.5 V or 0.5 V Control inputs				4						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 V	<del>,</del>	A or B ports		10						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	,	TDO		8						pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

			SN54AB	T18245	SN74AB	Г18245	UNIT
ĺ			MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	TCK	0	50	0	50	MHz
t <sub>w</sub>	Pulse duration	TCK high or low			5		ns
		A, B, DIR or OE before TCK↑			5		
t <sub>su</sub>	Setup time	TDI before TCK↑			6		ns
		TMS before TCK†			6		
		A, B, DIR or OE after TCK†			0		
t <sub>h</sub>	Hold time	TDI after TCK↑			0		ns
		TMS after TCK†			0		
ч	Delay time	Power up to TCK†			50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up			1		μs

NOTE 4: Preliminary specifications based on SPICE analysis



<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

### SN54ABT18245, SN74ABT18245 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS SCBS110A-AUGUST 1992-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

•		• •					•	•		
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT18245		SN74ABT18245		UNIT
	(INFOT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	.
t <sub>PLH</sub>	A or B	B or A						1	6	ns
t <sub>PHL</sub>		B 01 A						. 1	6	115
tpzH	ŌĒ	B or A						2	7.5	ns
t <sub>PZL</sub>	OE .							2	7.5	115
t <sub>PHZ</sub>	ŌE	OE B or A						2	7.5	ns
t <sub>PLZ</sub>		B or A						2	7.5	115

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

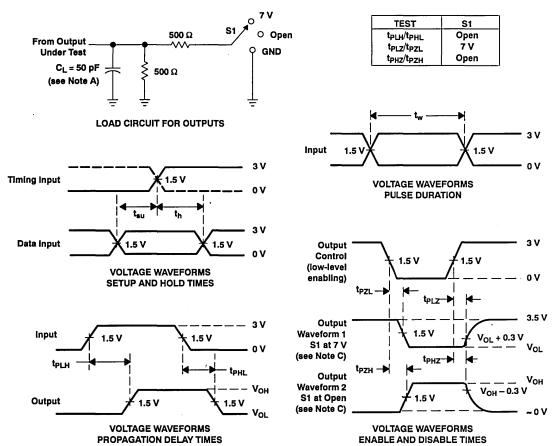
PARAMETER	FROM	FROM TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT18245		SN74ABT18245		
j	(INFO1)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	1	
f <sub>max</sub>	TCK		50	90		50		50		MHz	
tpLH	TCK1	A or B	1					3	12	ns	
t <sub>PHL</sub>	TOR	_ ^UB						3	12	115	
t <sub>РLН</sub>	TCKI	TDO						2	7		
t <sub>PHL</sub>	TCK.	TON	100						2	7	ns
t <sub>PZH</sub>	TCK.	A or B						3	14	ns	
t <sub>PZL</sub>	ICK							3	14		
t <sub>PZH</sub>	TOKI	TDO		-				2	8		
t <sub>PZL</sub>	TCK↓	100						2	8	ns	
t <sub>PHZ</sub>	TOKI	A D						3	14		
t <sub>PLZ</sub>	TCK↓	A or B						3	14	ns	
t <sub>PHZ</sub>	70//	TDO						2	8		
t <sub>PLZ</sub>	ickţ	TCKĮ TDO						2	8	ns	

NOTE 4: Preliminary specifications based on SPICE analysis

# SN54ABT18245, SN74ABT18245 SCAN TEST DEVICES

#### WITH 18-BIT BUS TRANSCEIVERS SCBS110A-AUGUST 1992-REVISED OCTOBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

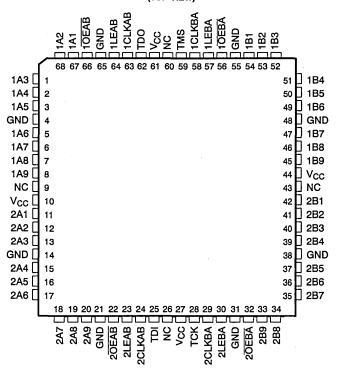
Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation

- . SCOPE ™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (HV)

# SN54ABT18502...HV PACKAGE (TOP VIEW)

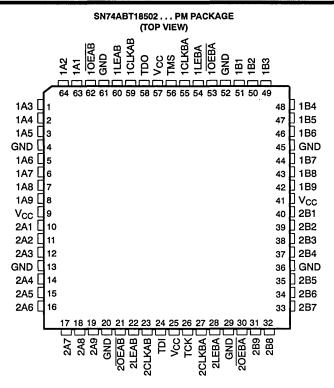


NC - No internal connection

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SCBS109A-AUGUST 1992-REVISED OCTOBER 1992



#### description

The SN54ABT18502 and SN74ABT18502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ registered bus transceivers.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When OEAB is low, the B outputs are active. When OEAB is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the OEBA, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.



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#### description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18502 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT18502 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

	INP	UTS		OUTPUT
OEAB	LEAB	CLKAB	Α	В
L	L	L	Х	B <sub>0</sub> ‡
L	L	<b>†</b>	L	L
L	L	†	Н	н
L	Н	X	L	L
L	Н	X	н	н
Н	X	X	X	Z

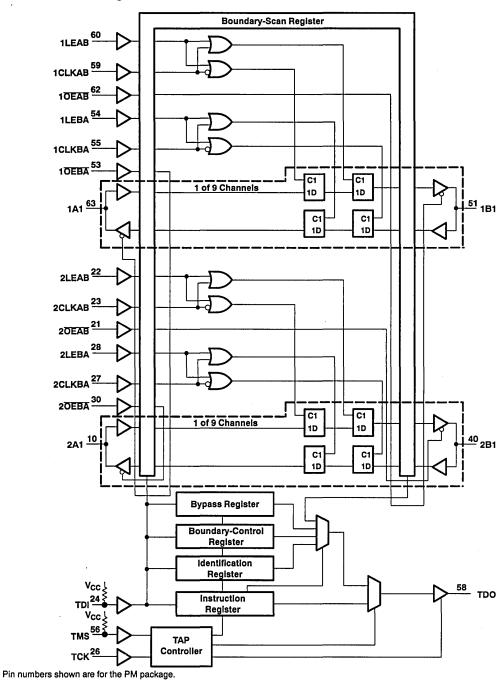
<sup>†</sup> A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

# SN54ABT18502, SN74ABT18502 **SCAN TEST DEVICES WITH** 18-BIT UNIVERSAL BUS TRANSCEIVERS SCB5109A-AUGUST 1992-REVISED OCTOBER 1992

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#### functional block diagram



INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherway)	vise noted)†
Supply voltage range, V <sub>CC</sub>	. −0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (I/O ports) (see Note 1)	−0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT18502	96 mA
SN74ABT18502	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum package power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2)	885 mW
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		SN54AB	T18502	SN74AB1	T18502	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2		2		V
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> For the SN74ABT18502 (PM package), the power derating factor for ambient temperatures greater than 55°C is -10.5 mW/°C.

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

DADAMETER	750	T CONDIT	IONO	Т	A = 25°(	2	SN54AB	T18502	SN74ABT18502		UNIT
PARAMETER	159	T CONDIT	IUNS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 m	Α			-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3	mA	2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3	mA	3			3		3		v
. V <sub>OH</sub>	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -24 \text{ mA}$			2			2				<b>V</b>
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -32 \text{ mA}$			2‡					2		
V	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 n	nA			0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	nA			0.55‡				0.55	•	
1.	V <sub>CC</sub> = 5.5 V,	CLK, LE, OE, TCK			±1		±1		±1	μА	
."	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports			±100		±100		±100	μΛ
Int	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub>		TDI,TMS			10		10		10	μА
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND TDI,TMS					-160		-160		-160	μА
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7	/			50		50		50	μА
lozL <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	$V_0 = 0.5$	/			-50		-50		-50	μА
loff	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤	: 5.5 V			±100				±100	μА
1 <sub>CEX</sub>	$V_{CC} = 5.5 \text{ V, } V_{O} =$	5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5$	/	-50	-100	-180	-50	-180	50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high			4		4		4	
Icc	I <sub>O</sub> = 0,	ports	Outputs low			80		80		80	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND	P0.10	Outputs disabled			4		4		4	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs		Control inputs		4						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 \	/	A or B ports		10						pF
C <sub>o</sub>	Vo = 2.5 V or 0.5 \	,	TDO		8						рF

NOTE 4: Preliminary specifications based on SPICE analysis

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.
 Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

1			SN54AB1	T18502	SN74ABT18502		UNIT
L			MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	. 0	100	0	100	MHz
	Pulse duration	CLKAB or CLKBA high or low			3		
tw	Fuise duration	LEAB or LEBA high			3		ns
	Setup time	A before CLKAB† or B before CLKBA†			5		
t <sub>su</sub>	Setup time	A before LEAB tor B before LEBA	<u> </u>		4		ns
+.	Hold time	A after CLKAB† or B after CLKBA†			0		
th	noid tillie	A after LEAB or B after LEBA			1		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

	•		SN54AB	Γ18502	SN74AB1	18502	
			MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
tw	Pulse duration	TCK high or low			5		ns
		A, B, CLK, LE, or OE before TCK†			5		
t <sub>su</sub>	Setup time	TDI before TCK†			6		ns
		TMS before TCK†			6		
		A, B, CLK, LE, or OE after TCK†			0		
th	Hold time	TDI after TCK†			0		ns
		TMS after TCK↑			0		
td	Delay time	Power up to TCK†			50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up			1		μs

NOTE 4: Preliminary specifications based on SPICE analysis

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

PARAMETER	FROM	(INPUT) $T_A = 25^{\circ}C$		SN74AB1	T18502	UNIT				
	( 5.)	(000.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLKAB or CLKBA		100	130		100		100		MHz
t <sub>PLH</sub>	A or B	B or A						1	6	ns
t <sub>PHL</sub>	7016	B 01 A						1	6	115
tpLH	CLKAB or CLKBA	B or A						2	6	ns
t <sub>PHL</sub>	CLIVAD UI CLIVDA	BUIA						2	6	115
t <sub>PLH</sub>	LEAB or LEBA	B or A						1.5	7.5	ns
t <sub>PHL</sub>	LEAD OF LEBA	BUIA						1.5	7.5	115
tpzH	OEAB or OEBA	B or A						2	7.5	20
t <sub>PZL</sub>	OEAB UI OEBA	BULA						2	7.5	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A						2	7.5	ns
t <sub>PLZ</sub>	OEAB UI OEBA	B UI A						2	7.5	HS

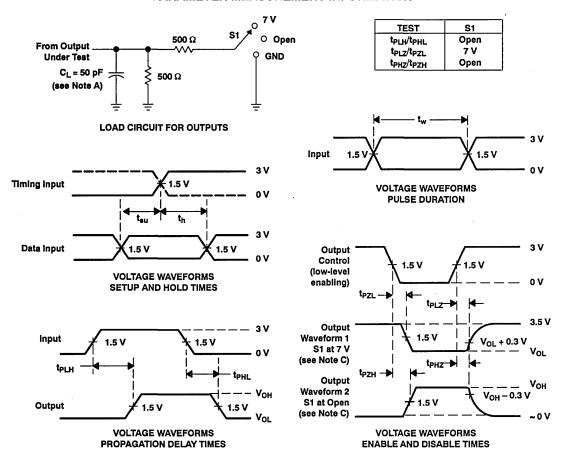
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

fmax tpLH tpHL tpHL tpHL tpHL tpHL tpHL tpHL	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 \ <sub>A</sub> = 25°C		SN54AB	T18502	SN74AB	UNIT		
	( 51)	(555.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>	TCK		50	90		50		50		MHz	
t <sub>PLH</sub>	TCK.	A or B						3	12	ns	
t <sub>PHL</sub>	ICK‡	AUIB						3	12	113	
t <sub>РLН</sub>	TCKĮ	TDO						2	7	ns	
t <sub>PHL</sub>	ICKI	100						2	7	115	
tpzH	TCKI	TCK	A or B						3	14	ns
tpZL	TOR	1 ^0'5						3	14	115	
t <sub>PZH</sub>	TCKĮ	TDO						2	8	ns	
t <sub>PZL</sub>	TOR	100						2	8	115	
t <sub>PHZ</sub>	TCKĮ	A or B		-		ĺ		3	14	ns	
t <sub>PLZ</sub>	ION	A OF B						3	14	IIIS	
t <sub>PHZ</sub>	TCVI	TDO						2	8		
t <sub>PLZ</sub>	TCK.	1 100						2	8	ns	

NOTE 4: Preliminary specifications based on SPICE analysis

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

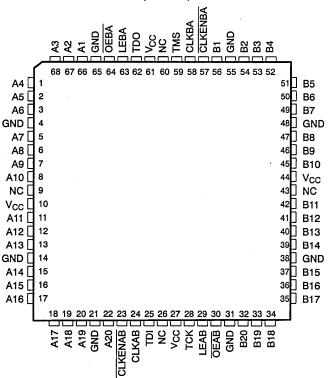
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- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
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- Two Boundary-Scan Cells per I/O for Greater Flexibility
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- SCOPE ™ instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (HV)

SN54ABT18504...HV PACKAGE (TOP VIEW)



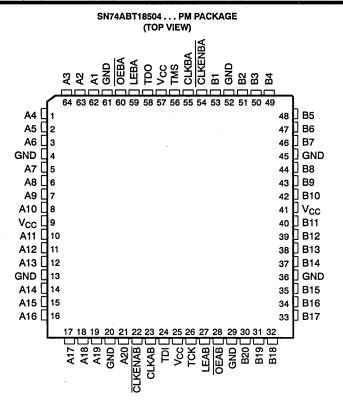
NC - No internal connection

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#### description

The SN54ABT18504 and SN74ABT18504 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ registered bus transceivers.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), clock-enable (CLKENBA) and CLKENBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKENAB is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and CLKENAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When OEAB is low, the B outputs are active. When OEAB is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the OEBA, LEBA, CLKENBA, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.



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#### description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18504 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT18504 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

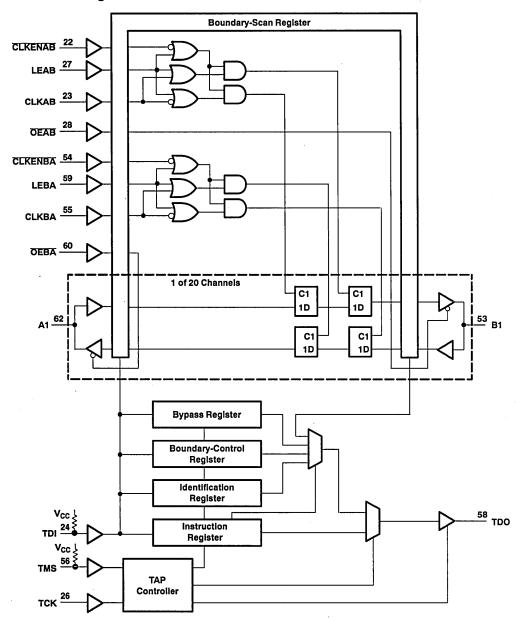
		INPUTS			OUTPUT
OEAB	LEAB	CLKENAB	CLKAB	Α	В
L	L	L	L	Х	B₀‡
L	L	L	Ť	L	L
L	L	L	<b>†</b>	Н	н
L	L	н	X	X	B₀‡
L	Н	X	X	L	L
L	Н	X	X	н	н
н	Х	X	X	X	Z

<sup>†</sup> A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, CLKENBA, and CLKBA.

Output level before the indicated steady-state input conditions were established.

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#### functional block diagram



Pin numbers shown are for the PM package.



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absolute maximum ratings over operating free-air temperature range (unless other	rwise noted)†
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	$-0.5$ V to 7 V
Input voltage range, V <sub>I</sub> (I/O ports) (see Note 1)	-0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT18504	96 mA
SN74ABT18504	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	50 mA
Maximum package power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2)	885 mW
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		18	N54ABT	18504	SN74ABT	18504	UNIT
[			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0	Vcc	0	Vcc	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate			10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> For the SN74ABT18504 (PM package), the power derating factor for ambient temperatures greater than 55°C is -10.5 mW/°C.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEC	T CONDITION	ONE	T	' <sub>A</sub> = 25°(	;	SN54AB	18504	SN74AB1	Γ18504	UNIT
PANAMEIEN	''=5	COMPILI	DNS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 m/	4			-1.2		-1.2		-1.2	٧
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ n}$	nA	2.5			2.5		2.5		
V <sub>OH</sub>	V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ m}$	nA	3			3		3		v
VOH	$V_{CC} = 4.5 \text{ V},$	l <sub>OH</sub> = -24	mA	2			2				•
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32	mA	2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 m	Α			0.55		0.55			V
VOL.	$V_{CC} = 4.5 \text{ V},$	I <sub>OL</sub> = 64 m	A			0.55‡				0.55	•
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		CLK, CLKEN, LE, OE, TCK			±1		±1		±1	μА
	At = ACC or GIAD		A or B ports			±100		±100		±100	
Iн	$V_{CC} = 5.5 \text{ V, V}_{I} = \text{V}_{CC}$	/cc	TDI,TMS			10		10		10	μΑ
l₁∟	$V_{CC} = 5.5 \text{ V, V}_{I} = 0$	SND	TDI,TMS			-160		-160		-160	μA
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$				50		50		50	μA
l <sub>ozl.</sub> §	V <sub>CC</sub> = 5.5 V,	$V_0 = 0.5 V$	1			-50		-50		-50	μA
loff	$V_{CC} = 0$ ,	V <sub>I</sub> or V <sub>O</sub> ≤	5.5 V			±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V, } V_{O} =$	5.5 V	Outputs high			50		50		50	μΑ
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 V$	,	-50	-100	-180	50	-180	-50	-180	mA
	$V_{CC} = 5.5 \text{ V},$	A or B	Outputs high			4		4		4	
Icc	I <sub>O</sub> = 0,	ports	Outputs low			88		88		88	mA
	$V_I = V_{CC}$ or GND	<b>F</b> • • • • • • • • • • • • • • • • • • •	Outputs disabled			4		4		4	
Δl <sub>CC</sub> #	$V_{CC} = 5.5 \text{ V},$ Other inputs at $V_{C}$	One input <sub>C</sub> or GND	at 3.4 V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
C <sub>io</sub>	V <sub>0</sub> = 2.5 V or 0.5 \	/	A or B ports		10						pF
C <sub>o</sub>	V <sub>0</sub> = 2.5 V or 0.5 \	/	TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT18504, SN74ABT18504 SCAN TEST DEVICES WITH 20-BIT UNIVERSAL BUS TRANSCEIVERS SCBS108A-AUGUST 1992-REVISED OCTOBER 1992

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

			SN54AB	T18504	SN74AB	T18504	
			SN54ABT18504  MIN MAX  0 100	MIN	MAX	UNIT	
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
	Dulas duration	CLKAB or CLKBA high or low			3		
t <sub>w</sub>	Pulse duration	LEAB or LEBA high			3		ns
		A before CLKAB† or B before CLKBA†			5		
t <sub>su</sub>	Setup time	A before LEAB or B before LEBA			4		ns
		CLKEN before CLK†			5		
		A after CLKAB† or B after CLKBA†			0		
th	Hold time	A after LEAB tor B after LEBA			1		ns
		CLKEN after CLK†			0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

			SN54AB1	T18504	SN74AB1	18504	UNIT
			MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
tw	Pulse duration	TCK high or low			5		ns
		A, B, CLK, CLKEN, LE, or OE before TCK†			5		
t <sub>su</sub>	Setup time	TDI before TCK†			6		ns
		TMS before TCK†			6		1
	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	A, B, CLK, CLKEN, LE, or OE after TCK↑			0		
th	Hold time	TDI after TCK†			0		ns
		TMS after TCK†			0		
t <sub>d</sub>	Delay time	Power up to TCK†			50		ns
tr	Rise time	V <sub>CC</sub> power up			1		μs

NOTE 4: Preliminary specifications based on SPICE analysis

# SN54ABT18504, SN74ABT18504 SCAN TEST DEVICES WITH 20-BIT UNIVERSAL BUS TRANSCEIVERS SCB5108A-AUGUST 1992-REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 \ <sub>A</sub> = 25°(		SN54ABT18504		SN74ABT18504		UNIT
	(	(33.1.01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
f <sub>max</sub>	CLKAB or CLKBA		100	130		100		100		MHz
t <sub>PLH</sub>	A or B	B or A						1	6	
t <sub>PHL</sub>		BOTA						1	6	ns
t <sub>PLH</sub>	CLKAB OF CLKBA	B or A						2	6	ns
<sup>t</sup> PHL	CLKAB or CLKBA	B 01 A	_					2	6	1115
t <sub>PLH</sub>	LEAB or LEBA	B or A						1.5	7.5	ns
t <sub>PHL</sub>	LEAD OF LEBA	BUIA						1.5	7.5	l ns
tpzH	OEAB or OEBA	B or A						2	7.5	
t <sub>PZL</sub>	OEAB OF OEBA	BUIA						2	7.5	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A						2	7.5	
t <sub>PLZ</sub>	OEAD OF CEDA	D UI A						2	7.5	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 1)

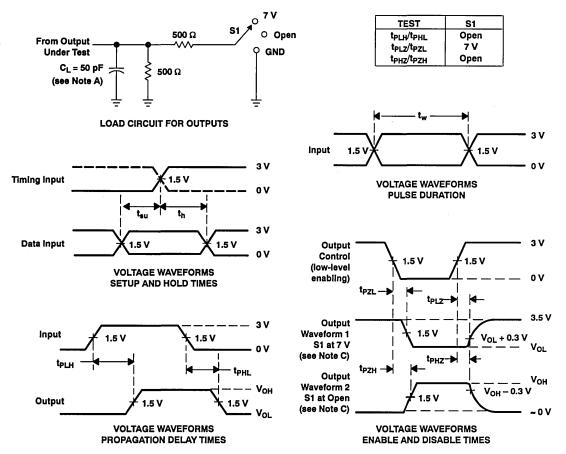
PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	T18504	SN74AB1	UNIT		
	(,	(555.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>	TCK		50	90		50		50		MHz	
t <sub>PLH</sub>	TCK.	A or B						. 3	12	ns	
t <sub>PHL</sub>	1014	7015						3	12	113	
t <sub>PLH</sub>	TCK1	тро						2	7	ns	
t <sub>PHL</sub>	ICK	100						2	7	115	
t <sub>PZH</sub>	TOVI	TCKĮ	A or B						3	14	20
t <sub>PZL</sub>	1004	A 01 B						3	14	ns	
t <sub>PZH</sub>	TCKĮ	ТДО						2	8	ns	
t <sub>PZL</sub>	TORT.	1 150						2	8	115	
t <sub>PHZ</sub>	TCKĮ	A or B						3	14		
t <sub>PLZ</sub>	ION	· Aurb						3	14	ns	
t <sub>PHZ</sub>	TCKĮ	TDO						2	8		
t <sub>PLZ</sub>	- 55						-	2	8	ns	

NOTE 4: Preliminary specifications based on SPICE analysis

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

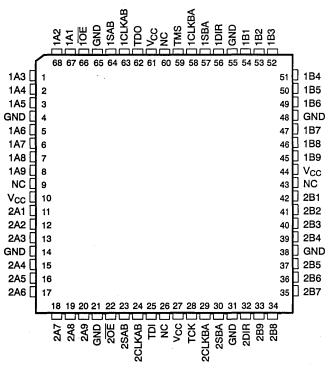
Figure 1. Load Circuit and Voltage Waveforms

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- Members of the Texas Instruments
   SCOPE ™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation

- SCOPE ™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (HV)

SN54ABT18646...HV PACKAGE (TOP VIEW)

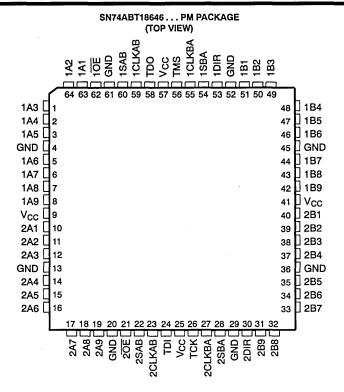


NC - No internal connection

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#### description

The SN54ABT18646 and SN74ABT18646 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable (OE) and direction (DIR) inputs. When OE is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When OE is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT18646.



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#### description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18646 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT18646 is characterized for operation from -40°C to 85°C.

# FUNCTION TABLE (normal mode, each 9-bit section)

,												
INPUTS						DAT	A I/O	ODERATION OR FUNCTION				
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	OPERATION OR FUNCTION				
X	Х	1	Х	Х	Х	Input	Unspecified <sup>†</sup>	Store A, B unspecified <sup>†</sup>				
X,	Х	X	†	X	Х	X Unspecified <sup>†</sup> Input Store		Store B, A unspecified <sup>†</sup>				
Н	Х	1	1	Х	Х	Input	Input	Store A and B data				
Н	Х	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage				
L	L	Х	Х	X	L	Output	Input	Real-time B data to A bus				
L	L	X	L	X	н	Output	Input disabled	Stored B data to A bus				
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus				
L	н	L	×	н	Х	Input disabled	Output	Stored A data to B bus				

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



### SN54ABT18646, SN74ABT18646 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS AND REGISTERS AUGUST 1992-REVISED OCTOBER 1992

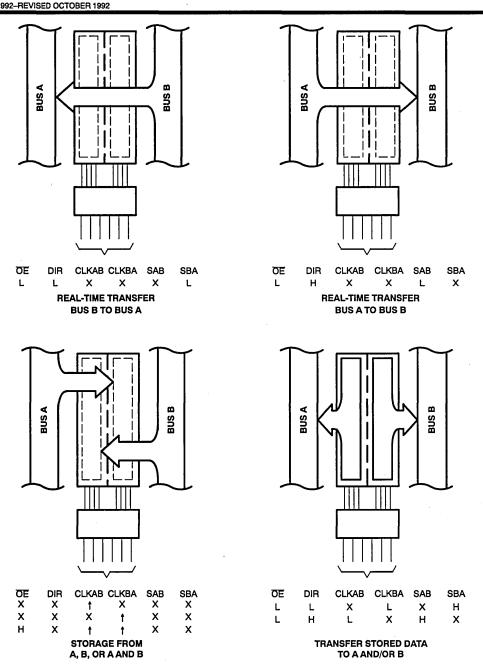
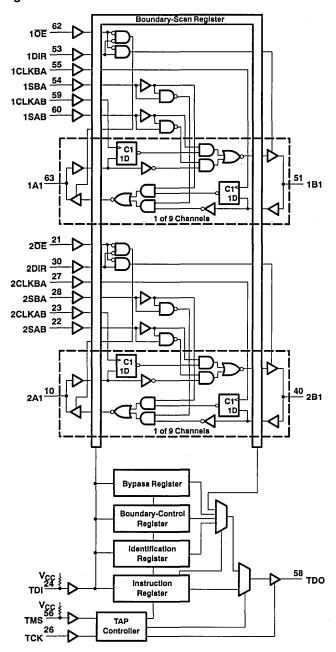


Figure 1. Bus-Management Functions



#### functional block diagram



Pin numbers shown are for the PM package.



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absolute maximum ratings over operating free-air temperature range (unless other	wise notea) '
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V

#### recommended operating conditions (see Note 3)

		SN54AB	SN54ABT18646		SN74ABT18646	
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2		2		٧
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	٧
Vı	Input voltage	0	Vcc	0	Vcc	V
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	ů

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> For the SN74ABT18646 (PM package), the power derating factor for ambient temperatures greater than 55°C is -10.5 mW/°C.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

DADAMETER	TEST COMPLETIONS			T <sub>A</sub> = 25°C			SN54ABT18646		SN74ABT18646		UNIT
PARAMETER	TEST CONDITIONS				TYP†	MAX	MIN	MAX	MIN	MAX	I UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA					-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA						2.5		2.5		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA						3		- 3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA						2				
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA								2		
V-	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA					0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55‡				0.55	, v
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		CLK, DIR, OE, S, TCK			±1		±1		±1	μА
i			A or B ports			±100		±100		±100	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub>		TDI, TMS			10		10		10	μA
l <sub>IL</sub>	$V_{CC} = 5.5 \text{ V, V}_{I} = 0$	and	TDI, TMS			-160		-160		-160	μΑ
l <sub>OZH</sub> \$	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$					50		50		50	μΑ
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V					-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	: 5.5 V			±100				±100	μΑ	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V		Outputs high			50		50		50	μA
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5	/	-50	-100	-180	-50	-180	50	-180	mA
	$V_{CC} = 5.5 \text{ V},$ $I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	A or B	Outputs high		0.9	2		2		2	
Icc		ports	Outputs low		30	38		38		38	mA
			Outputs disabled		0.9	2		2		2	
Δl <sub>CC</sub> #	$V_{CC} = 5.5 \text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND					1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		3						pF
Cio	V <sub>O</sub> = 2.5 V or 0.5 \	7	A or B ports		10						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 \	7	TDO		8						pF

NOTE 4: Preliminary specifications based on SPICE analysis

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

			SN54AB	T18646	SN74AB	Г18646	UNIT
			MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low			3		ns
t <sub>su</sub>	Setup time	A before CLKAB† or B before CLKBA†			5		ns
th	Hold time	A after CLKAB† or B after CLKBA†	]		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

			SN54AB	Г18646	SN74AB7	T18646	11117
			MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
t <sub>w</sub>	Pulse duration	TCK high or low	1		5		ns
		A, B, CLK, DIR, OE, or S before TCK†			5		
t <sub>su</sub>	Setup time	TDI before TCK†			6		ns
		TMS before TCK†			6		
		A, B, CLK, DIR, OE, or S after TCK†			0		
th	Hold time	TDI after TCK†			0		ns
		TMS after TCK†			0		
t <sub>d</sub>	Delay time	Power up to TCK†			50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up			_ 1		μs

NOTE 4: Preliminary specifications based on SPICE analysis

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

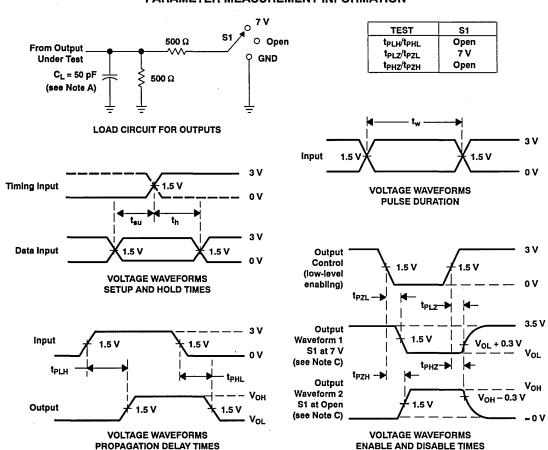
PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	CC = 5 V 4 = 25°C		SN54AB	Г18646	SN74AB1	Г18646	UNIT
	\	(55.1.51)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLKAB or CLKBA		100	130		100		100		MHz
t <sub>PLH</sub>	A or B	B or A						1	6	ns
t <sub>PHL</sub>	AOIB	2017						1	6	115
tpLH	CLKAB or CLKBA	B or A						2	6	ns
t <sub>PHL</sub>	CLIVAD OF CLIVBA	BUIA						2	6	113
t <sub>PLH</sub>	SAB or SBA	B or A						2	8	ns
t <sub>PHL</sub>	3AB 01 3BA	BULA						2	8	113
t <sub>PZH</sub>	DIR	B or A						2	7.5	ns
t <sub>PZL</sub>	DIA	B 01 A						2	7.5	113
tezh	ŌĒ	B or A		-				2	7.5	ns
t <sub>PZL</sub>	) <u> </u>	BULA						2	7.5	115
tpHZ	DIR	B or A						2	7.5	ns
t <sub>PLZ</sub>	l Din	BULA						2	7.5	118
t <sub>PHZ</sub>	OE .	B or A						2	7.5	ns
t <sub>PLZ</sub>	]	BUIA						2	7.5	113

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	ſ18646	SN74ABT	Г18646	UNIT
	( • . ,	(000.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	TCK		50	90		50		50		MHz
tрин	TCKĮ	A or B						3	12	ns
t <sub>PHL</sub>	TOR	AUIB						3	12	113
tрцн	TCKĮ	TDO						2	7	ns
t <sub>PHL</sub>	ICK	150						2	7	115
<sup>t</sup> PZH	TCKĻ	A or B						3	14	ns
t <sub>PZL</sub>	TOR	Aorb						3	14	115
t <sub>PZH</sub>	TCKI	TDO						. 2	8	ns
t <sub>PZL</sub>	TCK.	100						2	8	115
t <sub>PHZ</sub>	TOVI	A or B						3	14	
t <sub>PLZ</sub>	TCK1	\ \^\01B						3	14	ns
t <sub>PHZ</sub>	TCKĮ	2141 770						2	8	ns
t <sub>PLZ</sub>	iont	TDO						2	8	iis

NOTE 4: Preliminary specifications based on SPICE analysis

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

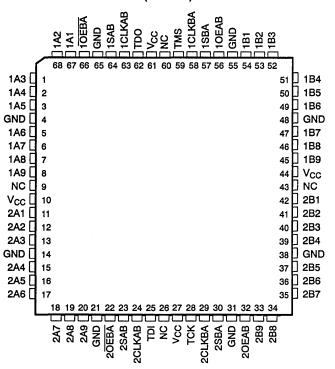
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- Members of the Texas Instruments

  SCOPE ™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation

- SCOPE ™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (HV)

# SN54ABT18652...HV PACKAGE (TOP VIEW)

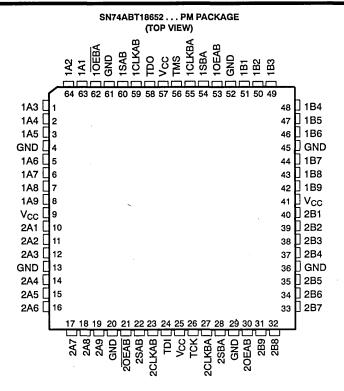


NC - No internal connection

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#### description

The SN54ABT18652 and SN74ABT18652 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and OEBA inputs. Since the OEBA input is active-low, the A outputs are active when OEBA is low and are in the high-impedance state when OEBA is high. Figure 1 illustrates the four fundamental bus-management functions that may be performed with the 'ABT18652.



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#### description (continued)

In the test mode, the normal operation of the SCOPE<sup>™</sup> bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18652 is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT18652 is characterized for operation from -40°C to 85°C.

# FUNCTION TABLE (normal mode, each 9-bit section)

		INPU	rs			DAT	A I/O	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	OPERATION OR FUNCTION
L	Н	L	L	X	Х	Input disabled	Input disabled	Isolation
L	Н	t	<b>†</b>	X	X	Input	Input	Store A and B data
X	Н	<b>†</b>	L	X	Х	Input	Unspecified <sup>†</sup>	Store A, hold B
Н	Н	<b>†</b>	<b>†</b>	X‡	Х	Input	Output	Store A in both registers
L	X	L	<b>†</b>	X	X	Unspecified <sup>†</sup>	Input	Hold A, store B
L	L	t	<b>†</b>	X	X‡	Output	Input	Store B in both registers
L	L	Х	Х	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	н	Output	Input	Stored B data to A bus
н	Н	X	X	L	X	Input	Output	Real-time A data to B bus
н	Н	L	X	н	X	Input	Output	Stored A data to B bus
н	L	L	L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

Select control = H: clocks must be staggered in order to load both registers.



<sup>\*</sup> Select control = L: clocks can occur simultaneously.

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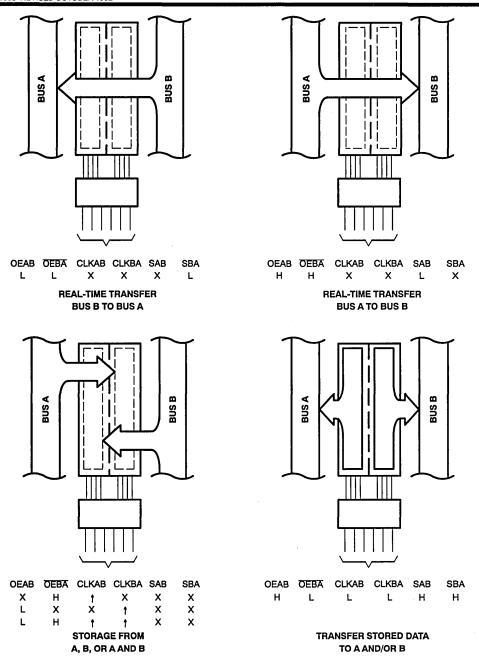
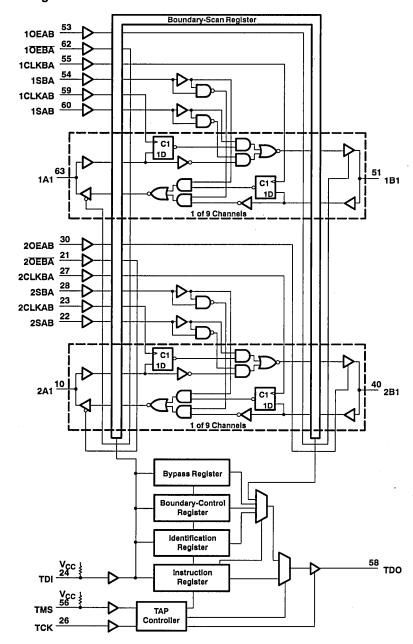


Figure 1. Bus-Management Functions



#### functional block diagram



Pin numbers shown are for the PM package.



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chaolista maximism ratings	aver energing fre	a air tamparatura rapa	e (unless otherwise noted)†
absolute maximum ratings	s over operating fre	e-air temperature rand	e (uniess otherwise notea):

Supply voltage range, V <sub>CC</sub>	_0.5 V to 7 V
Input voltage range, V <sub>1</sub> (except I/O ports) (see Note 1)	
Input voltage range, V <sub>I</sub> (I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT18652	96 mA
SN74ABT18652	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum package power dissipation at T <sub>A</sub> = 55°C (in still air) (see Note 2)	885 mW
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		SN54AB1	18652	SN74AB1	T18652	UNIT
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		8.0		0.8	V
VI	Input voltage	0	Vcc	0	Vcc	<b>V</b>
Іон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		10		10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	ů

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> For the SN74ABT18652 (PM package), the power derating factor for ambient temperatures greater than 55°C is -10.5 mW/°C.

## SN54ABT18652, SN74ABT18652 **SCAN TEST DEVICES WITH** 18-BIT BUS TRANSCEIVERS AND REGISTERS AUGUST 1992-REVISED OCTOBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

DADAMETED	750	TOONDIT	IONE	1	<sub>A</sub> = 25°0	;	SN54AB1	Γ18652	SN74AB1	18652	UNIT
PARAMETER	l ies	T CONDIT	IUNS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
Vik	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 m	ıA			-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3	mA	2.5			2.5		2.5		
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3	mA	3			3		3		v
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = 24	1 mA	2			2				<b>v</b>
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = - 32	2 mA	2‡					2		
· · ·	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 r	nA .			0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 r	nA			0.55‡				0.55	· •
l <sub>1</sub>	V <sub>CC</sub> = 5.5 V,		CLK, OEAB, OEBA, S, TCK			±1		±1		±1	μА
	$V_I = V_{CC}$ or GND		A or B ports			±100		±100		±100	
lн	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = \	/cc	TDI, TMS			10		10		10	μА
l <sub>IL</sub>	$V_{CC} = 5.5 \text{ V, V}_{I} = 0$	SND	TDI, TMS			-160		-160		-160	μA
lozh§	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7$	V			50		50		50	μА
lozL <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5	<b>V</b>			-50		-50		-50	μА
loff		V <sub>I</sub> or V <sub>O</sub> =				±100		±450		±100	μA
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> =	5.5 V	Outputs high			50		50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5	V	-50	-100	-180	-50	-180	-50	180	mA
	V <sub>CC</sub> = 5.5 V,	A or B	Outputs high			4		4		4	
lcc	l <sub>O</sub> = 0,		Outputs low			80		80		80	mA
	$V_I = V_{CC}$ or GND	POLIS	Outputs disabled			4		4		4	
Δi <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>C</sub>		at 3.4 V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		Control inputs		4						pF
C <sub>io</sub>	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$	/	A or B ports		10						pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	Outputs low   Outputs low			8						pF

NOTE 4: Preliminary specifications based on SPICE analysis

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

			SN54AB	T18652	SN74AB	T18652	UNIT
			MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	CLKAB or CLKBA	0	100	0	100	MHz
t <sub>w</sub>	Pulse duration	CLKAB or CLKBA high or low			3		ns
t <sub>su</sub>	Setup time	A before CLKAB↑ or B before CLKBA↑			5		ns
th	Hold time	A after CLKAB† or B after CLKBA†	i		0		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

			SN54AB	Г18652	SN74AB1	Γ18652	UNIT
		•	MIN	MAX	MIN	MAX	UNII
f <sub>clock</sub>	Clock frequency	тск	0	50	0	50	MHz
tw	Pulse duration	TCK high or low			5		ns
		A, B, CLK, OEAB, OEBA, or S before TCK↑			5		
t <sub>su</sub>	Setup time	TDI before TCK†			6		ns
		TMS before TCK†			6		
		A, B, CLK, OEAB, OEBA, or S after TCK†			0		
th	Hold time	TDI after TCK†			0		ns
		TMS after TCK†			0		
t <sub>d</sub>	Delay time	Power up to TCK†			50		ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> power up			1		μS

NOTE 4: Preliminary specifications based on SPICE analysis

## SN54ABT18652, SN74ABT18652 SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS AND REGISTERS AUGUST 1992—REVISED OCTOBER 1992

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

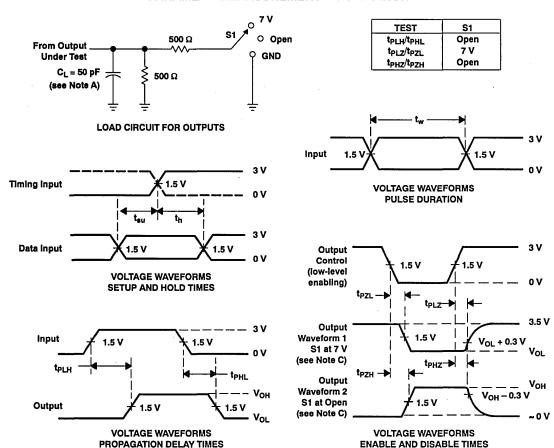
PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	Γ18652	SN74AB	T18652	UNIT
	( 0.)	(6611 61)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLKAB or CLKBA		100	130		100		100		MHz
t <sub>PLH</sub>	A or B	B or A						1	6	ns
t <sub>PHL</sub>	7015	BUIA						1	6	115
t <sub>PLH</sub>	CLKAB or CLKBA	B or A						2	6	ns
t <sub>PHL</sub>	CEIVAD OF CEIVADA	BUIA						2	6	115
t <sub>PLH</sub>	SAB or SBA	B or A						2	8	ns
t <sub>PHL</sub>	SAB OF SBA	BUIA						2	8	118
tрzн	OEAB or OEBA B or A						2	7.5		
t <sub>PZL</sub>	OEAB OF OEBA	BUIA						2	7.5	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A						2	7.5	
t <sub>PLZ</sub>	OEAD OF OEBA	D UF A						2	7.5	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		<sub>CC</sub> = 5 V <sub>A</sub> = 25°C		SN54AB	SN54ABT18652		54ABT18652 SN74ABT18652		Г18652	UNIT
	( • .)	(666.,	MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f <sub>max</sub>	TCK		50	90		50		50		MHz		
tpLH	TCK.	A or B						3	12	ns		
t <sub>PHL</sub>	TOR	AUID						3	12	ns		
t <sub>PLH</sub>	TCK.	TDO						2	7	ns		
t <sub>PHL</sub>	TOR	100						2	7	115		
t <sub>PZH</sub>	TCK!	A or B						3	14	ns		
t <sub>PZL</sub>	TOR	A 01 B						3	14	113		
tpzH	TCK.	тро						2	8	ns		
t <sub>PZL</sub>	ION	100						2	8	118		
t <sub>PHZ</sub>	TCKI	A or B						3	14			
t <sub>PLZ</sub>	10K‡	A or B						3	14	ns		
t <sub>PHZ</sub>	TCKĮ	TDO						2	8			
t <sub>PLZ</sub>	ICK\$	100				1	-	2	8	ns		

NOTE 4: Preliminary specifications based on SPICE analysis

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns.}$   $t_f \leq 2.5 \text{ ns.}$
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

	General Information
	ABT Octals 2
	ABT Widebus™
	ABT Widebus+™
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	JTAG SCOPE™ Testability Devices 8
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	LVT Widebus™
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	ABT Characterization Information 12
	Mechanical Data

#### **LVT OCTALS**

#### **Features**

- EPICIIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode circuitry
- Expanded V<sub>CC</sub> range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- SOIC and EIAJ TSSOP packaging
- TI has established an alternate source

#### **Benefits**

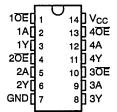
- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized, scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I<sub>CCZ</sub>) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
- Standardization that comes from a common product approach

#### SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

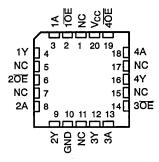
MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

SN54LVT125 . . . J PACKAGE SN74LVT125 . . . DW OR PW PACKAGE (TOP VIEW)



SN54LVT125 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

#### description

These bus buffers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (OE) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT125 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT125 is characterized for operation from -40°C to 85°C.

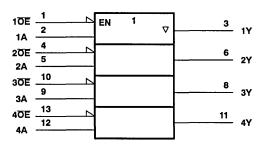
# FUNCTION TABLE (each buffer)

İ	INP	JTS	OUTPUT
	ŌĔ	Α	Y
	L	H	Н
	L	L	L
	н	Χ	z

## SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

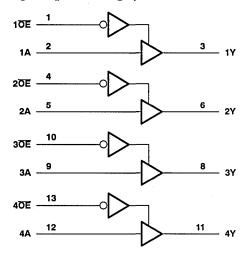
MAY 1992-REVISED NOVEMBER 1992

#### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



Pin numbers shown are for DW, J, and PW packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT125
SN74LVT125
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT125
SN74LVT125
Input clamp current, $I_{iK}$ (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package
PW package
Storage temperature range

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

# SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### recommended operating conditions

			SN54L	VT125	SN74L	√T125	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	£2.	2		V
V <sub>IL</sub>	Low-level input voltage			\$0.8		0.8	V
۷ <sub>I</sub>	Input voltage		,	< <sup>₹</sup> 5.5		5.5	V
IOH	High-level output current			-24		-32	mA
loL	Low-level output current		,3	24		32	mA
I <sub>OL</sub> †	Low-level output current		20,	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	10		10	ns/V
TA	Operating free-air temperature	-	-55	125	-40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

## SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

ADAMETED		T COMPITIONS		SN5	4LVT125	1	SN7	4LVT125		UNIT
ARAMETER	l les	T CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	i <sub>I</sub> = -18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
.,	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = – 8 mA		2.4			2.4			V
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -24 mA		2						V
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	$V_{CC} = 2.7 \text{ V},$	I <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	.,
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	٧
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA			3	,			0.55	
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V				10			10	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		<i>&amp;</i> '	±1			±1	
lį	$V_{CC} = 3.6 \text{ V},$	V <sub>I</sub> = V <sub>CC</sub>	<u> </u>		A.	1			1	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins		7	-5			-5	
loff	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V	Ô					±100	μΑ
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	<u> </u>	Q75			75			
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Data inputs	-75			-75			μΑ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V	•		-	1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high		0.12	0.19		0.12	0.19	
la-	V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0,	Outputs low		4.5	7		4.5	7	m.A
Icc	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.12	0.19		0.12	0.19	1117
ΔI <sub>CC</sub> §	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ o		- 0.6 V,			0.3			0.2	m/
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0				4			4		pF
Co	V <sub>O</sub> = 3 V or 0				8			8		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

# switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

	50011		SN54LVT125 SN74LVT1					74LVT12	25	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 3.3 V ± 0.3 V V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V	UNIT
		(661.161)	MIN	MAX	> MAX	MIN	TYP†	MAX	MAX	l
t <sub>PLH</sub>	Α	V	1	4.2	4.7	1	2.7	4	4.5	
t <sub>PHL</sub>	Α	1	1	<b>€</b> 9	5.1	1	2.9	3.9	4.9	ns
t <sub>PZH</sub>	ŌĒ	· v	. 1	<u></u> ું 34.9	6.2	1	3.4	4.7	6	
t <sub>PZL</sub>	- OE	<b>T</b>	1.1	<b>3 4.9</b>	6.7	1.1	3.4	4.7	6.5	ns
t <sub>PHZ</sub>	ŌĒ	~	1.8 🙏	5.3	5.9	1.8	3.7	5.1	5.7	
t <sub>PLZ</sub>	<u> </u>	1	1.3	4.7	4.2	1.3	2.6	4.5	4	ns

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.

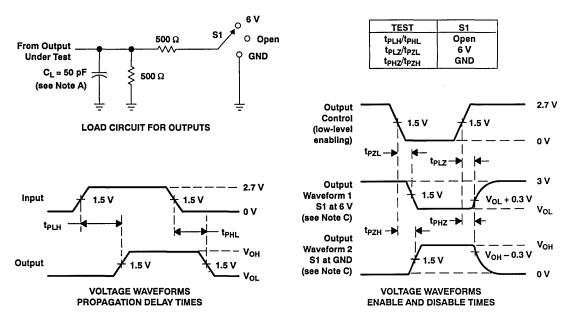


For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

MAY 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54LVT240, SN74LVT240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SEPTEMBER 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low-Static Power** Dissipation
- **Supports Mixed-Mode Signal Operation** (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- **Supports Unregulated Battery Operation** Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT240 is organized as two 4-bit buffer/line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

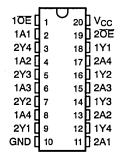
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT240 is characterized for operation from -40°C to 85°C.

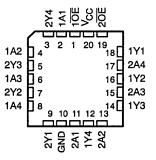
**FUNCTION TABLE** (each buffer)

	(ouon bunon)						
INP	JTS	OUTPUT					
ŌE	Α	Y					
L	Н	L					
L	L	н					
н	X	z					

SN54LVT240 ... J PACKAGE SN74LVT240 ... DW OR PW PACKAGE (TOP VIEW)



#### SN54LVT240 . . . FK PACKAGE (TOP VIEW)



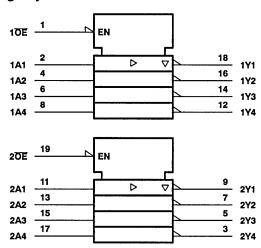
PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



#### SN54LVT240, SN74LVT240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

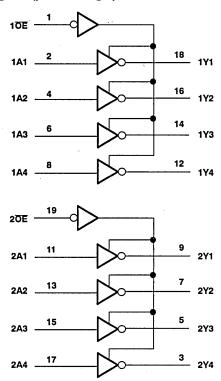
SEPTEMBER 1992-REVISED NOVEMBER 1992

#### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, $V_{CC}$	<sup>-</sup> -0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT240	
SN74LVT240	
Current into any output in the high state, IO (see Note 2): SN54LVT240	48 mA
SN74LVT240	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	0.85 W
PW package	0.5 W
Storage temperature range	65°C to 150°C

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and Vo > Vcc.



# SN54LVT240, SN74LVT240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SEPTEMBER 1992-REVISED NOVEMBER 1992

## recommended operating conditions

			SN54L	VT240	SN74L	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	V
٧ı	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
l <sub>OL</sub> †	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

## SN54LVT240, SN74LVT240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SEPTEMBER 1992—REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	54LVT24	0	SN7	4LVT240		UNIT	
PARAMETER				MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V <sub>IK</sub>	$V_{CC} = 2.7 \text{ V},$	I <sub>I</sub> = -18 mA				-1.2			-1.2	<b>V</b>
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						٧
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	l <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
.,	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	l <sub>OL</sub> = 32 mA				0.5			0.5	<b>V</b>
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10			10	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	
lį	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	Data alaa			1			1	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins			<b>-</b> 5			<b>–</b> 5	
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μΑ
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A inputs	75			75			μА
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Airiputs	-75			-75			μ.Α.
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high		0.12	0.19		0.12	0.19	
laa	V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0,	Outputs low		8.6	12		8.6	12	mA
lcc	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.12	0.19		0.12	0.19	
ΔI <sub>CC</sub> §	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ of		- 0.6 V,			0.2			0.2	mA
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0				. 4			4		pF
Co	V <sub>O</sub> = 3 V or 0				8			8		pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 3.3 V,  $T_{A}$  = 25°C.

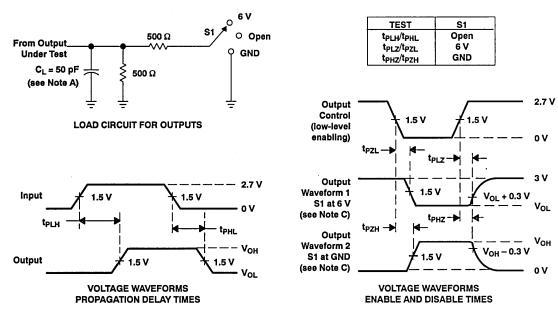
For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### SN54LVT240, SN74LVT240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SEPTEMBER 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_f \leq 2.5 \ ns$ ,  $t_f \leq 2.5 \ ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54LVT244, SN74LVT244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

AUGUST 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

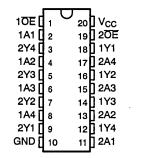
These octal buffers and line drivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT244 is organized as two 4-bit line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

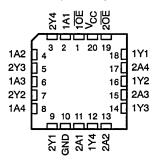
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT244 is characterized for operation from –40°C to 85°C.

#### SN54LVT244 . . . J PACKAGE SN74LVT244 . . . DW OR PW PACKAGE (TOP VIEW)



# SN54LVT244 . . . FK PACKAGE (TOP VIEW)



# FUNCTION TABLE (each buffer)

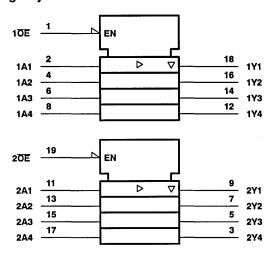
INPL	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Х	Z



#### SN54LVT244, SN74LVT244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

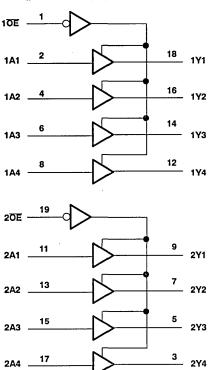
AUGUST 1992-REVISED NOVEMBER 1992

#### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	. $-0.5 \text{ V}$ to $4.6 \text{ V}$
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1) .	$\dots$ -0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT244	96 mA
SN74LVT244	128 mA
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT244	48 mA
SN74LVT244	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

<sup>\$</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_0 > V_{CC}$ .

## recommended operating conditions

			SN54L	VT244	SN74L	UNIT		
			MIN	MAX	MIN	MAX	7 5811	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V	
V <sub>IH</sub>	High-level input voltage				2		V	
V <sub>IL</sub>	Low-level input voltage			\$0.8		0.8	V	
VI	Input voltage		1 ,	<b>₹</b> 5.5		5.5	V	
ЮН	High-level output current		<i>A</i>	-24		-32	mA	
loL	Low-level output current		3	24		32	mA	
l <sub>OL</sub> †	Low-level output current		<sup>2</sup> O,	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	10		10	ns/V	
TA	Operating free-air temperature	-55	125	-40	85	°C		

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

## SN54LVT244, SN74LVT244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

AUGUST 1992-REVISED NOVEMBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS		SN54LVT244			SN74LVT244				
PARAMETER				MIN	TYP	MAX	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	l <sub>I</sub> =18 mA				-1.2			-1.2	٧
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			>
.,	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		. 2						V
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	V
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA			3	`			0.55	
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10			10	±1 1 μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		Ø.	±1			±1	
lj.	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	Bata sina			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins		3	-5			-5	
loff	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5	5 V	Q.75				•	±100	μΑ
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A :	Q75			75			^
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>i</sub> = 2 V	A inputs	-75			-75			μΑ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high		0.12	0.19		0.12	0.19	
lcc .	$V_{CC} = 3.6 V$ ,	I <sub>O</sub> = 0,	Outputs low		8.6	12		8.6	12	mA
iCC	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.12	0.19		0.12	0.19	IIIA
∆I <sub>CC</sub> §	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2			0.2	mA	
Ci	V <sub>I</sub> = 3 V or 0				4			4		pF
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0				8			8		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

			18	154LVT2	44		SN7	4LVT24	14	
PARAMETER (INPUT)	FROM	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		V <sub>CC</sub> = 2.7 V	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 2.7 \text{ V}$		V <sub>CC</sub> = 2.7 V	UNIT	
	( 0.)	(6611-617	MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t <sub>PLH</sub>	. ^	_	1	4.5	5.2	1	2.5	4.3	5	ns
t <sub>PHL</sub>	A		1	4.4	5.4	1	2.5	4.2	5.2	115
tpzH	ŌĒ	_	1	္လ5.4	6.5	1	2.7	5.2	6.3	ns
t <sub>PZL</sub>	OE .	'	1.1	္တိ 5.4	6.9	1.1	3.1	5.2	6.7	115
t <sub>PHZ</sub>	ŌĒ		2.1	5.8	6.5	2.1	3.9	5.6	6.3	ns
t <sub>PLZ</sub>	<u> </u>	<u> </u>	1.8	5.3	5.8	1.8	3.2	5.1	5.6	115

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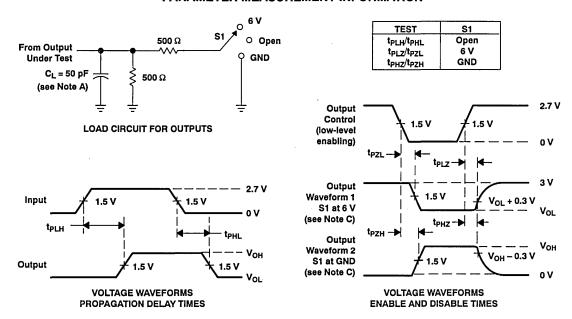


<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

AUGUST 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130A-D4504, MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- **Supports Mixed-Mode Signal Operation** (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

These octal bus transceivers are designed

specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

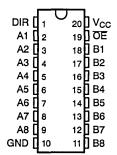
The SN54LVT245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT245 is characterized for operation from -40°C to 85°C.

The 'LVT245 is designed for asynchronous communication between data buses. The device transmits data from

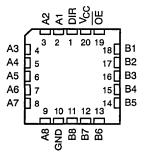
#### **FUNCTION TABLE**

INP	UTS	OPERATION				
OE	DIR					
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Х	Isolation				

SN54LVT245 . . . J PACKAGE SN74LVT245... DW OR PW PACKAGE (TOP VIEW)



SN54LVT245 . . . FK PACKAGE (TOP VIEW)



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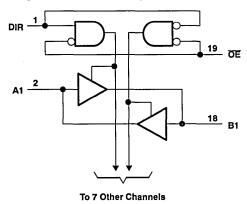
#### SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130A-D4504, MAY 1992-REVISED NOVEMBER 1992

#### logic symbol†

#### 3EN1[BA] 3EN2[AB] 18 **⊽** 1 2∇ 17 A2 **B2** 16 **B3** 15 **B4** A4 14 **A5 B**5 13 A6 **B6** 12 **B7** Α7 9 11 **B8 8**A

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub> 0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT245
SN74LVT245
Current into any output in the high state, Io (see Note 2): SN54LVT245
SN74LVT245 64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package
PW package
Storage temperature range

<sup>\*</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and  $V_Q > V_{CC}$ .

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS130A-D4504, MAY 1992-REVISED NOVEMBER 1992

#### recommended operating conditions

			SN54L	SN54LVT245		VT245		
			MIN	MAX	MIN MAX		UNIT	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧	
VIH	High-level input voltage		2	4.	2		٧	
V <sub>IL</sub>	Low-level input voltage			≲0.8		0.8	٧	
VI	Input voltage			₹ <sup>7</sup> 5.5		5.5	٧	
ЮН	High-level output current			-24		-32	mA	
loL	Low-level output current		్లక	24		32	mA	
lo <sub>L</sub> †	Low-level output current		`O,	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

#### SN54LVT245, SN74LVT245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130A-D4504, MAY 1992-REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD 414575D		T 001/DITIONS		SN5	4LVT24	5	SN7	4LVT245		
PARAMETER	TES	T CONDITIONS		MIN	TYP	MAX	MIN	TYP†	MAX	UNIT
VIK	V <sub>CC</sub> = 2.7 V <sub>i</sub>	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	1 <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = - 8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						\ \ \
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2	
	$V_{CC} = 2.7 \text{ V},$	I <sub>OL</sub> = 24 mA				0.5			0.5	
V	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
$V_{OL}$	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	v
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA			, s				0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		¥2.	±1			±1	
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V	Control pins		Ŗ.	10			10	
II	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V			<u> </u>	20			20	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§		>	1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0		,Q°		-5			-5	
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_1$ or $V_0 = 0$ to 4.5	5 V	Q.					±100	μА
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75			75			μА
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>i</sub> = 2 V	A OF B PORS	-75			-75			μΛ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μА
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				1			-1	μΑ
			Outputs high		0.13	0.19		0.13	0.19	
Icc		$I_{O}=0$ ,	Outputs low		8.8	12		8.8	12	mA
.cc	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.13	0.19		0.13	0.19	
Δlcc¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ of		- 0.6 V,			0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0				4			4		pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0				10			10		pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

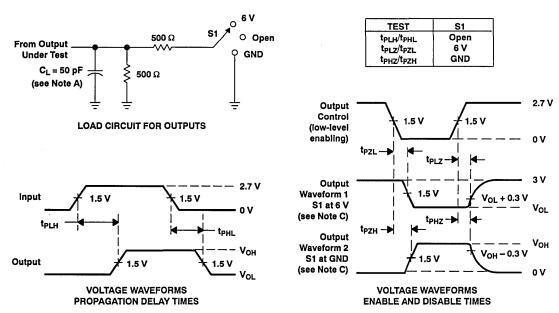
SCBS130A-D4504, MAY 1992-REVISED NOVEMBER 1992

switching characteristics over recommended operating free-air temperature range,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

l I		TO (OUTPUT)	s		SN	4LVT24	15			
PARAMETER	FROM (INPUT)		V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> =	3.3 V ±	0.3 V	V <sub>CC</sub> = 2.7 V	UNIT
	( 0.,		MIN	MAX	∰ MAX	MIN	TYP	MAX	MAX	
t <sub>PLH</sub>	A or B	B or A	1	4.2	4.9	1	2.4	4	4.7	ns
t <sub>PHL</sub>	AUIB	BUIA	1	42	4.8	1	2.4	4	4.6	115
tpzH	ŌE	A or B	1.1	్ర5.7	7.3	1.1	3.4	5.5	7.1	ns
t <sub>PZL</sub>	OE .	AOIB	1.5	స్త్రో 5.7	6.7	1.5	3.6	5.5	6.5	115
t <sub>PHZ</sub>	QE	A or B	2.2 🗸	6.1	6.7	2.2	4.3	5.9	6.5	ns
t <sub>PLZ</sub>			2	5	5	2	3.5	4.8	4.8	115

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

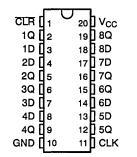
#### SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

MAY 1992-REVISED NOVEMBER 1992

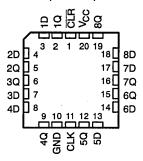
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notics.

#### SN54LVT273 . . . J PACKAGE SN74LVT273 . . . DW OR PW PACKAGE (TOP VIEW)



### SN54LVT273 . . . FK PACKAGE (TOP VIEW)



#### description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

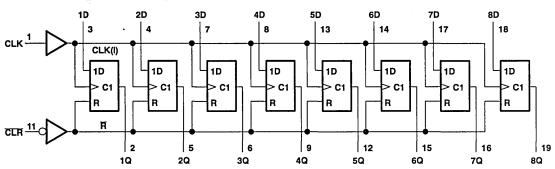
The SN54LVT273 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74LVT273 is characterized for operation from  $-40^{\circ}$ C to 85°C.

### FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
CLR	CLK	D	Q
L	X	Х	L
н	t	H	н
н	1	L	L
Н	L	Х	Qo

Texas VI

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage range, V <sub>CC</sub> –0.5 V to	o 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	′ to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)0.5 V	′ to 7 V
Current into any output in the low state, Io: SN54LVT273	96 mA
SN74LVT273	28 mA
Current into any output in the high state, IO (see Note 2): SN54LVT273	48 mA
SN74LVT273	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0) — — —	·50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	·50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	0.85 W
PW package	0.5 W
Storage temperature range –65°C to	150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .



PRODUCT PREVIEW

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR MAY 1992-REVISED NOVEMBER 1992

#### recommended operating conditions

			SN54L	VT273	SN74L	VT273	
			MIN	MAX	MIN	MAX	UNIT .
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		٧
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
Vι	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
lo <sub>L</sub> †	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

## SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR MAY 1992-REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	750	T CONDITIONS		SNS	4LVT273	3	SN7	4LVT273	1	UNIT
PARAMETER	153	T CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNII
Vik	V <sub>CC</sub> = 2.7 V,					-1.2			-1.2	V
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	l <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						· ·
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	l <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	· ·
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V				10			10	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	
II	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	Data pins			1			1	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins			-5			<b>-</b> 5	
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_1$ or $V_0 = 0$ to 4.5	5 V						±100	μΑ
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	Data innuta	75			75			
hold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Data inputs	-75			-75			μА
lozh	$V_{CC} = 3.6 \text{ V},$	V <sub>O</sub> = 3 V				1			1	μА
l <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high		0.12	0.19		0.12	0.19	
lcc	V <sub>CC</sub> = 3.6 V,	l <sub>O</sub> = 0,	Outputs low		8.6	12		8.6	12	mA
icc	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.12	0.19		0.12	0.19	, ma
Δlcc <sup>§</sup>	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ of		- 0.6 V,			0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									рF
Co	V <sub>0</sub> = 3 V or 0									pF

 $<sup>^{\</sup>dagger}$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

#### switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

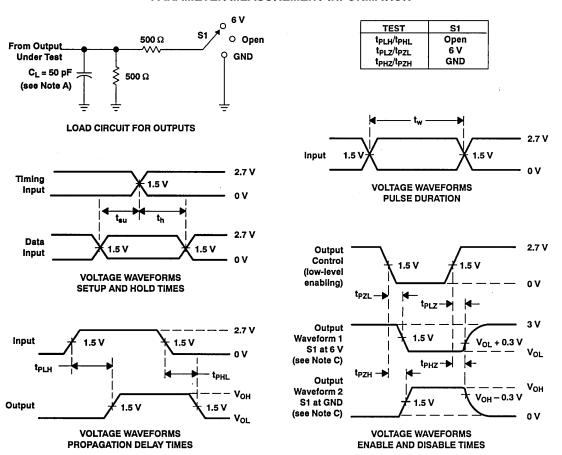
		TO (OUTPUT)	S		'3					
PARAMETER	TER FROM (INPUT)		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			V <sub>CC</sub> = 2.7 V	UNIT
	( 01)	(001.01,	MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
f <sub>max</sub>										MHz
t <sub>PLH</sub>	CLK	Any 0					3.4			
t <sub>PHL</sub>	CLK	Any Q					3.6			ns
t <sub>PHL</sub>	CLR	Any Q					3.3			ns



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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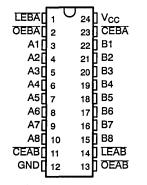
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

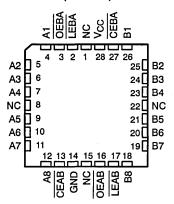
These octal transceivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

SN54LVT543...JT PACKAGE SN74LVT543...DW OR PW PACKAGE (TOP VIEW)



SN54LVT543 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT543 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74LVT543 is characterized for operation from  $-40^{\circ}$ C to 85°C.

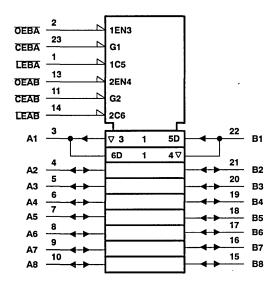
## SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPL		ОИТРИТ	
CEAB	LEAB	OEAB	Α	В
H	Х	Х	Х	Z
×	X	н	Х	z
L.	Н	L	X	B₀ <sup>‡</sup>
L	L	L	L	L
L	L	L	Н	н

<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

#### logic symbol§

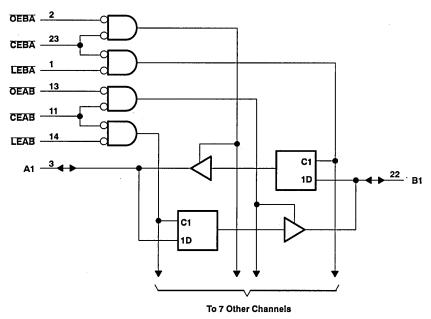


<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and PW packages.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

#### SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### logic diagram (positive logic)



Pin numbers shown are for DW, JT, and PW packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, IO: SN54LVT543	96 mA
SN74LVT543	
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT543	48 mA
SN74LVT543	64 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	0.85 W
PW package	0.5 W
Storage temperature range	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

# SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### recommended operating conditions

			SN54L	VT543	SN74LVT543		LINET
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
ViH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
l <sub>OL</sub> †	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TΑ	Operating free-air temperature		-55	125	-40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TOONDITIONS		SN5	4LVT543	}	SN7	4LVT543	3	UNIT
PARAMETER	l les	T CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP	MAX	UNII
Ýικ	V <sub>CC</sub> = 2.7 V,	l <sub>I</sub> = -18 mA				-1.2			-1.2	V
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						V
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	$V_{CC} = 2.7 \text{ V},$	I <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	•
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Caratari aire			±1			±1	
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V	Control pins			10			10	
i <sub>i</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Ì			-5			-5	
loff	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μΑ
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A on B marks	75			75			
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or B ports	-75	-		-75			μΑ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V			-	-1			1	μА
			Outputs high		0.13	0.19		0.13	0.19	
Icc		l <sub>O</sub> = 0,	Outputs low		8.8	12		8.8	12	mA
icc	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.13	0.19		0.13	0.19	
Δlcc¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ o	1.6 V, One input at V <sub>CC</sub> – 0.6 V, t V <sub>CC</sub> or GND				0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0				4.5			4.5		pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0				11			11		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				s	N54LVT5	43	8	43		
				V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V	דואט
				MIN	MAX	MIN	MIN	MAX	MIN	1
t <sub>w</sub>	Pulse durati	on	LEBA low	3.3		3.3	3.3		3.3	ns
		Data before LEAB or LEBA†	High	0		0	0		0	i
	Catua tima		Low	0.8		1.1	0.8		1.1	1
t <sub>su</sub>	Setup time	Data before	High	0		0	0		0	ns
	,	CEAB or CEBA†	Low	0.9		1.2	0.9		1.2	1
	Link dian	Data after LEAB o	LEBA†	1.7		1.7	1.7		1.7	
th	Hold time	Data after CEAB of	r CEBA†	1.8		1.8	1.8		1.8	ns

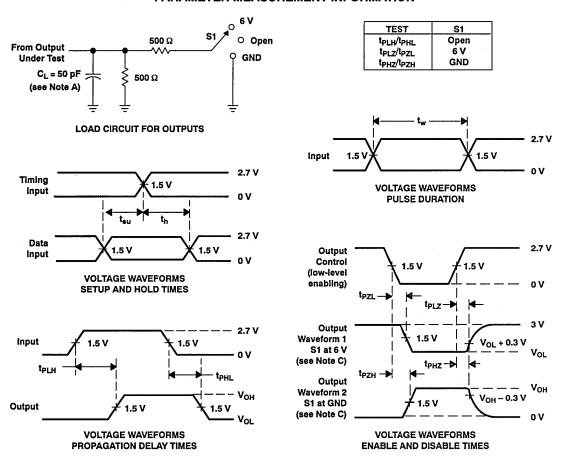
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

			S	N54LVT5	43		SN7	74LVT54	13	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		Vcc =	3.3 V ±	0.3 Y	V <sub>CC</sub> = 2.7 V	UNIT
	( 01)		MIN	MAX	MAX	MIN	TYP	MAX	MAX	
t <sub>PLH</sub>	A or B	B or A	1	4.9	5.7	1	2.9	4.7	5.5	ns
t <sub>PHL</sub>	AUIB	BUIA	1	4.8	6	1	3.3	4.6	5.8	ns
t <sub>PLH</sub>	CE.	A or B	1	6.1	7.5	1	4	5.9	7.3	ns
t <sub>PHL</sub>		70, 5	1	5.9	7.5	1	4.1	5.7	7.3	115
t <sub>PZH</sub>	ŌĒ	A or B	1	6	7.8	1	4.1	5.8	7.6	ns
t <sub>PZL</sub>	OE.	1 ^0''	1.1	6.6	8.4	1.1	4.5	6.4	8.2	115
t <sub>PHZ</sub>	ŌĒ	A or B	2.4	6.7	7.3	2.4	4.8	6.5	7.1	
t <sub>PLZ</sub>	OE	7015	2	6	6.1	2	4	5.8	5.9	ns
t <sub>PZH</sub>	CE	A or B	1	6.2	7.8	1	4.2	6	7.6	ns
t <sub>PZL</sub>	CE	^0'B	1.4	6.9	8.5	1.4	4.7	6.7	8.3	ns
t <sub>PHZ</sub>	CE	A or B	2.3	6.6	7.3	2.3	4.7	6.4	7.1	
t <sub>PLZ</sub>	Ju Ju	A or B	2	5.6	5.8	2	3.8	5.4	5.6	ns

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



#### SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

These octal latches are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

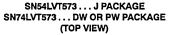
The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

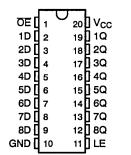
A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

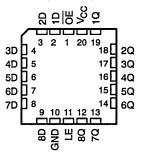
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

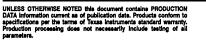
The SN54LVT573 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74LVT573 is characterized for operation from  $-40^{\circ}$ C to 85°C.

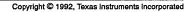




### SN54LVT573 . . . FK PACKAGE (TOP VIEW)







#### SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

### FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	н
L	н	L	L
L	L	X	Q <sub>0</sub>
н	X	×	z

#### logic symbol<sup>†</sup>

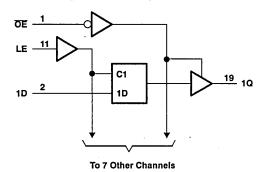
7

8

6D

#### ΕN LE C1 19 1D 1D 1Q 18 3 2D 2Q 4 17 3Q 3D 16 4D 4Q 15 6 5D 5Q

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

14

13 6Q

7Q 12

8Q

Supply voltage range, V <sub>CC</sub> –0.5 V to 4.6 V	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state, $V_0$ (see Note 1) $-0.5 \text{ V}$ to $7 \text{ V}$	
Current into any output in the low state, Io: SN54LVT573	
SN74LVT573	
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT573	
SN74LVT573 64 mA	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	
PW package	
Storage temperature range	

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

## SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### recommended operating conditions

			SN54L	VT573	SN74L	VT573	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	42.	2		V
VIL	Low-level input voltage			\$0.8		8.0	V
Vı	Input voltage		,	<b>₹</b> 5.5		5.5	٧
ІОН	High-level output current			-24		-32	mA
loL	Low-level output current		1,3	24		32	mA
l <sub>OL</sub> †	Low-level output current		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

#### SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

ADAMETER	~~~	T CONDITIONS		SN5	4LVT573		SN7	4LVT573		UNIT	
ARAMETER	l les	T CONDITIONS		MIN	TYP†	MAX	MIN	TYP	MAX	UNIT	
ViK	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧	
	V <sub>CC</sub> □ MIN to MAX‡,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
	V <sub>CC</sub> = 2.7 V,	l <sub>OH</sub> = -8 mA		2.4			2.4			v	
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	i <sub>OH</sub> = - 24 mA		2						V	
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2				
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5		
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	.,	
$V_{OL}$	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	٧	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55					
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA			· ·				0.55		
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10			10		
_	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		Q.	±1			±1		
lį	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>			<del>K</del>	1			1	μ^ 1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins		<b>}</b>	-5			-5		
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5	5 V						±100	μΑ	
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	<u> </u>	Q75			75				
hold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Data inputs	-75			-75			μΑ	
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μА	
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μА	
			Outputs high		0.13	0.19		0.13	0.19		
L	V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0,	Outputs low		8.6	12		8.6	12	-m ^	
Icc			Outputs disabled		0.13	0.19		0.13	0.19	mA	
Δlcc <sup>§</sup>	V <sub>CC</sub> = 3 V to 3.6 V, Other inputs at V <sub>CC</sub> o					0.2			0.2	mA	
Ci	V <sub>I</sub> = 3 V or 0	V <sub>I</sub> = 3 V or 0			4			4		pF	
Co	V <sub>O</sub> = 3 V or 0				8			8		pF	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			8	N54LVT5	73	9	573		
ì			V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> = 3.3 V	' ± 0.3 V	V <sub>CC</sub> = 2.7 V	UNIT
			MIN	MAX	MIN	MIN	MAX	MIN	
t <sub>w</sub>	Pulse duration, LE high		3.3	√0,%		3.3		3.3	ns
t <sub>su</sub>	Setup time, data before LE↓	High or low	0.7	\$\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	0.6	0.7		0.6	ns
t <sub>h</sub>	Hold time, data after LE↓	High or low	1.6	4	1.8	1.6		1.8	ns

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

#### SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

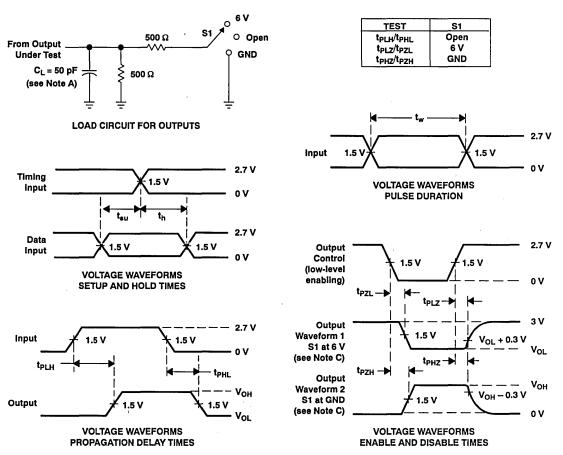
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## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54LVT573							
PARAMETER	FROM (INPUT)		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> =	3.3 V ±	0.3 V	V <sub>CC</sub> = 2.7 V	UNIT
ļ			MIN	MAX	MAX	MIN	TYP <sup>†</sup>	MAX	MAX	}
t <sub>PLH</sub>	D	Q	1	4.4	<b>4.9</b>	1	2.5	4.2	4.7	
t <sub>PHL</sub>		<u> </u>	1	4.5	5.4	1	2.7	4.3	5.2	ns
t <sub>PLH</sub>	LE	Q	1.6	5.8	6.5	1.6	3.5	5.6	6.3	
t <sub>PHL</sub>	LE	"	2.5	<i>,</i> ,,6.7	7.4	2.5	4.3	6.5	7.2	ns
t <sub>PZH</sub>	ŌĒ	Q	1	్లు 5.3	6.4	1	2.8	5.1	6.2	
t <sub>PZL</sub>	OE.	4	1.3	<u>,</u> 5.7	6.8	1.3	3.3	5.5	6.6	ns
t <sub>PHZ</sub>	Œ		2 4	5.9	6.9	2	3.7	5.7	6.7	
tPLZ	OE	_ Q	1.5	4.8	5.3	1.5	3	4.6	5.1	ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns. t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

These octal flip-flops are designed specifically for low-voltage (3.3-V)  $V_{\rm CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

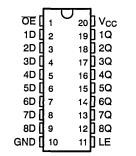
A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

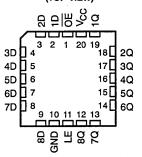
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT574 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74LVT574 is characterized for operation from  $-40^{\circ}$ C to 85°C.

#### SN54LVT574 . . . J PACKAGE SN74LVT574 . . . DW OR PW PACKAGE (TOP VIEW)



### SN54LVT574 . . . FK PACKAGE (TOP VIEW)





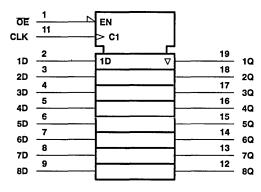
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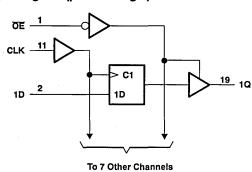
### FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
ŌĔ	CLK	Q	
L	, 1	Н	Н
L	Ť	L	L
L	L	Х	$Q_0$
Н	X	Х	z

#### logic symbol†

#### logic diagram (positive logic)





#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>	0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)	$\dots$ -0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT574	96 mA
SN74LVT574	
Current into any output in the high state, Io (see Note 2): SN54LVT574	48 mA
SN74LVT574	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package	0.85 W
PW package	0.5 W
Storage temperature range	65°C to 150°C

<sup>&</sup>lt;sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

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#### recommended operating conditions

	- 100 100		SN54L	VT574	SN74L	VT574	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	42.	2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage		٠,	<b>₹</b> 5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current		1 3	. 24		32	mA
l <sub>OL</sub> †	Low-level output current		\O,	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Q.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	750	T CONDITIONS		SNS	4LVT574	1	SN7	4LVT574		UNIT	
PAHAMETEH	IES	T CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNII	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	l <sub>j</sub> = –18 mA				-1.2			-1.2	٧	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	l <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
V	V <sub>CC</sub> = 2.7 V,	1 <sub>OH</sub> = – 8 mA		2.4			2.4			v	
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -24 mA		2						V	
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2				
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5		
.,	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v	
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	V	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55					
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA				•			0.55		
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V			Š	10			10		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		Q <sup>2</sup>	±1			±1		
11	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	Data pins		A.	1			1	μА	
	$V_{CC} = 3.6 \text{ V},$	V <sub>I</sub> = 0	Data pins		<u> </u>	-5			-5		
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V	ू ऐं <sub>75</sub>					±100	μΑ	
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	Data innuta	Q75			75				
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Data inputs	-75			-75			μΑ	
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μА	
l <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μА	
			Outputs high		0.13	0.19		0.13	0.19		
1	V <sub>CC</sub> = 3.6 V,	$I_{O}=0$ ,	Outputs low		8.7	12		8.7	12	mA	
lcc	V <sub>I</sub> = V <sub>CC</sub> or GND Outputs disabled				0.13	0.19		0.13	0.19	IIIA	
Δlcc§	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ of	One input at V <sub>CC</sub> – 0.6 V, or GND				0.2			0.2	mA	
Ci	V <sub>I</sub> = 3 V or 0	1 = 3 V or 0			4			4		рF	
Со	V <sub>O</sub> = 3 V or 0				8			8		pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVT	574						
			V <sub>CC</sub> = 3.3 \	/ ± 0.3 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	150	∠ 0	150	0	150	٥	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or	low	3.3	, j	<b>%3.3</b>		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK†	High or low	2	45°66	2.4		2		2,4		ns
t <sub>h</sub>	Hold time, data after CLK†	High or low	0.3		0		0.3		0		ns



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

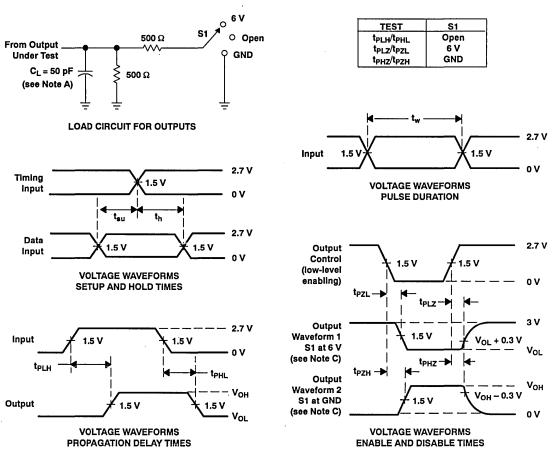
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## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

	FROM (INPUT)		SN54LVT574												
PARAMETER			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		UNIT			
	(1141-01)	(001701)	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	6.2 6.6 5.9 6.2 5.9	ı			
f <sub>max</sub>			150		150		150			150		MHz			
t <sub>PLH</sub>	CLK	a	1.7	5.6	Z,	6.4	1.7	3.6	5.4		6.2				
t <sub>PHL</sub>		CLK	<u>۱</u>	2.4	6.1	27	6.8	2.4	4.3	5.9		6.6	ns		
. t <sub>PZH</sub>	ŌĔ	OE	ਨਵ	ਨਵ	Q	1	5.		6.1	1	2.9	4.8		5.9	
t <sub>PZL</sub>			_ <u>"</u>	1.3	5.8		6.4	1.3	3.4	5.1		6.2	ns		
t <sub>PHZ</sub>	OE	_ <u> </u>	1.9	Ç5.7		6.1	1.9	4	5.5		5.9				
t <sub>PLZ</sub>		"	1.7	<b>Q`4.7</b>		4.7	1.7	3.2	4.5		4.5	ns			

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_1 \leq 2.5$  ns,  $t_1 \leq 2.5$  ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

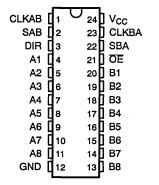
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

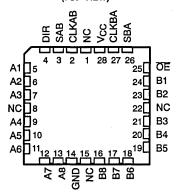
These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

SN54LVT646... JT PACKAGE SN74LVT646... DW OR PW PACKAGE (TOP VIEW)



SN54LVT646 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

#### **SN54LVT646, SN74LVT646** 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### description (continued)

The SN54LVT646 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT646 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE**

INPUTS				DAT	A I/O	OPERATION OR FUNCTION					
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION ON FONCTION			
×	Х	t	Х	×	х	Input	Unspecified <sup>†</sup>	Store A, B unspecified <sup>†</sup>			
x	X	Х	t	×	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>			
Н	х	Ť	1	×	х	Input	Input	Store A and B data			
Н	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage			
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus			
L	L	X	L	X	Н	Output	Input	Stored B data to A bus			
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus			
L	Н	L	X	н	X	Input	Output	Stored A data to B bus			

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

## SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

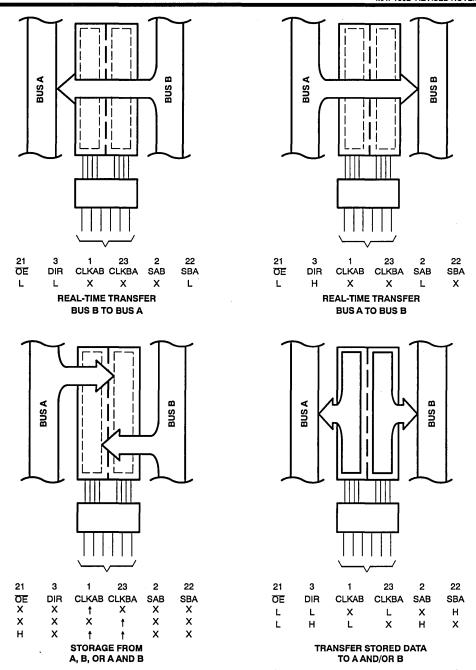
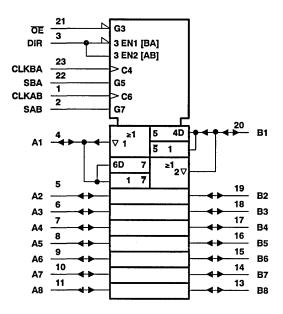


Figure 1. Bus-Management Functions



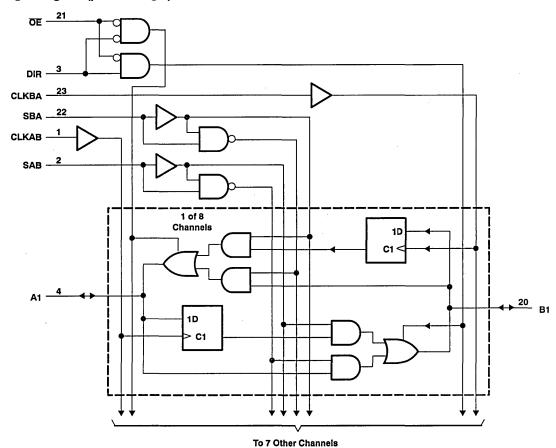
#### SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and PW packages.

#### logic diagram (positive logic)



Pin numbers shown are for DW, JT, and PW packages.

#### SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) $-0.5$ V to 7 V
Current into any output in the low state, Io: SN54LVT646
SN74LVT646
Current into any output in the high state, IO (see Note 2): SN54LVT646
SN74LVT646
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package
PW package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54L	VT646	SN74LVT646			
			MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧	
ViH	High-level input voltage		2	<u>(2)</u>	2		٧	
V <sub>IL</sub>	Low-level input voltage		1	<u>\$</u> 0.8		0.8	V	
Vι	Input voltage			<b>₹</b> 5.5		5.5	V	
ЮН	High-level output current			-24		-32	mA	
loL	Low-level output current		Ş	24		32	mA	
lOL‡	Low-level output current		Ç	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	₹,	10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	ç	

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

9-58

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and VO > VCC.

## SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	7-0	SN5	4LVT646	3	SN7					
PAHAMEIER	IES	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT		
Vik	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	V
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	l <sub>OH</sub> = -100 μA		V <sub>CC</sub> 0.2			V <sub>CC</sub> -0.2			
v	V <sub>CC</sub> = 2.7 V,		2.4			2.4			v	
∨он	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						· •
	V <sub>CC</sub> = 3 V,	$I_{OH} = -32 \text{ mA}$					2			
	V <sub>CC</sub> = 2.7 V,				0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	V <sub>CC</sub> = 2.7 V, I <sub>OL</sub> = 24 mA				0.5			0.5	
Variable   Variable			0.4			0.4	V			
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	V
	V <sub>CC</sub> = 3 V,				0.55					
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA			<u>.</u>	,			0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V			<u> </u>	10			10	
lį	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V	[		<u> </u>	20			20	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§		>	1			1	
*	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0		,oʻ		-5			-5	
1 <sub>OFF</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V			Q,					±100	μА
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A B	75			75			μА
hold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or b ports	-75			-75			
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
		I <sub>O</sub> = 0,	Outputs high		0.13	0.19		0.13	0.19	
loo	V <sub>CC</sub> = 3.6 V,		Outputs low		8.8	12		8.8	12	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND				0.13	0.19		0.13	0.19	
Δlcc <sup>¶</sup>						0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0				4.5			4.5		pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0				11			11		pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 3.3 V,  $T_{A}$  = 25°C.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

				SN54LVT	646			SN74LVT6	546		
			V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	150	2 0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or lo	w	3.3	Q	3.3		3.3		3.3		ns
	Setup time, A or B before	High	1.3	<u>,Ĉ,</u>	1.3		1.3		1.3		
<sup>τ</sup> su	CLKAB† or CLKBA†	Low	2	్టర్	2.4		2		2.4		ns
t <sub>h</sub>	Hold time, A or B after CLKAB† or CLKBA†		0.4	E.	0.4		0.4		0.4		ns

## switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 2)

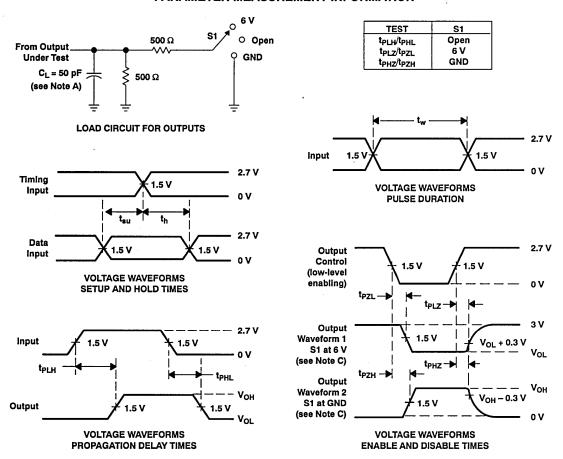
			S	N54LVT6	46		SN7	4LVT64	6	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> =	3.3 V ±	0.3 V	V <sub>CC</sub> = 2.7 V	UNIT
	( 5.,	(0011 01)	MIN	MAX	MAX	MIN	TYP <sup>†</sup>	MAX	MAX	
f <sub>max</sub>			150			150				MHz
t <sub>PLH</sub>	CLKBA or	A or B	1.8	5.9	6.9	1.8	3.8	5.7	6.7	
t <sub>PHL</sub>	CLKAB	AUID	2.1	5.9	6.6	2.1	. 3.8	5.7	6.4	ns
t <sub>РLН</sub>	A or B	D. o. A	1.3	4.9	<u>.</u> \$ 5.6	1.3	2.8	4.7	5.4	
t <sub>PHL</sub>	AOIB	B or A	1	4.8	<i>¥</i> 5.5	1	2.7	4.6	5.3	ns
t <sub>PLH</sub>	SBA or SAB‡	A au B	1.4	6:4	7.4	1.4	3.7	6.2	7.2	
t <sub>PHL</sub>	SBA OF SABT	A or B	1.4	<b>46.4</b>	7	1.4	3.8	6.2	6.8	ns
t <sub>PZH</sub>	ŌĒ	A D	1	6.4 5 6 6 6.2	7.4	1	3	5.8	7.2	
t <sub>PZL</sub>	UE .	A or B	1 ,	<b>6.2</b>	7.5	1	3.2	6	7.3	ns
t <sub>PHZ</sub>	AC.	4 P	2.3 €	6.7	7.1	2.3	4.3	6.5	6.9	
t <sub>PLZ</sub>	ŌĒ	A or B	2.2	6	6.1	2.2	3.8	5.8	5.9	ns
t <sub>PZH</sub>	DIR	A B	1	6.7	7.7	1	3.4	6.5	7.5	
t <sub>PZL</sub>	DIK	A or B	1.2	6.5	7.3	1.2	3.4	6.3	7.1	ns
t <sub>PHZ</sub>	DID	A D	1.7	7.4	8.3	1.7	4.1	7.2	8.1	
t <sub>PLZ</sub>	DIR	A or B	1.5	6	6.5	1.5	3.5	5.8	6.3	ns

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>\*</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mli DIPS

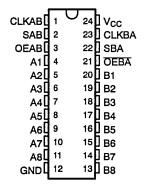
#### description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

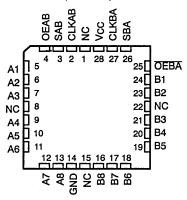
The 'LVT652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

PRODUCT PREVIEW Information concerns products in the formative or dealign phase of development. Characteristic data and other specifications are dealing opals. Texas instruments reserves the right to change or discontinue these products without notice.

SN54LVT652...JT PACKAGE SN74LVT652...DW OR PW PACKAGE (TOP VIEW)



SN54LVT652 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT652 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74LVT652 is characterized for operation from  $-40^{\circ}$ C to 85°C.



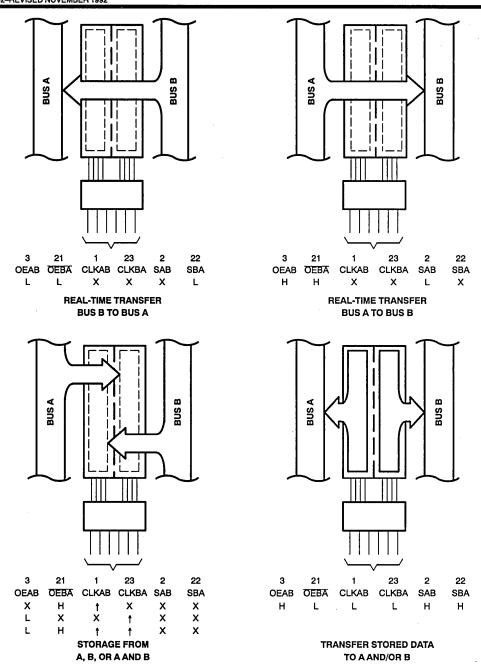


Figure 1. Bus-Management Functions



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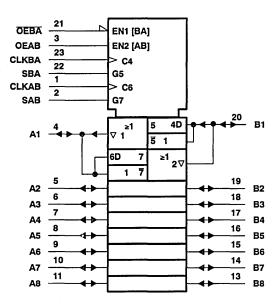
		C				

		INPU	TS			DATA	A I/O†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	L	L	X	X	Input	Input	Isolation
L	н	<b>†</b>	<b>†</b>	X	X	Input	Input	Store A and B data
×	н	†	L	×	X	Input	Unspecified <sup>‡</sup>	Store A, hold B
н	н	<b>†</b>	<b>†</b>	X‡	X	Input	Output	Store A in both registers
L	X	L	t	X	×	Unspecified <sup>‡</sup>	Input	Hold A, store B
L	L	<b>†</b>	<b>†</b>	×	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	Н	Output	Input	Stored B data to A bus
н	н	X	X	L	×	Input	Output	Real-time A data to B bus
н	Н	L	X	н	×	Input	Output	Stored A data to B bus
н	L	L	L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

Select control = L; clocks can occur simultaneously.
 Select control = H; clocks must be staggered in order to load both registers.

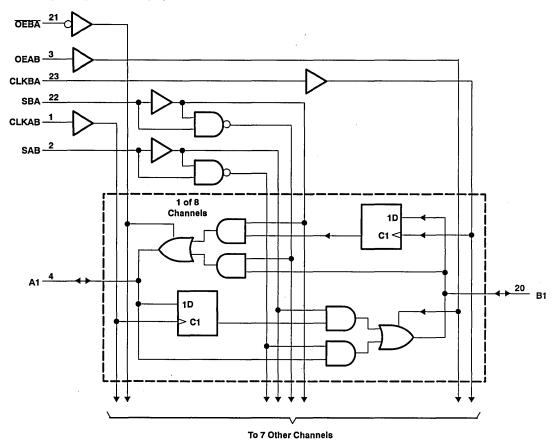
#### logic symbol§



<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and PW packages.

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### logic diagram (positive logic)



Pin numbers shown are for DW, JT, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
Supply voltage range, V <sub>CC</sub> –0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, $V_0$ (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT652
SN74LVT652
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT652
SN74LVT652
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0) –50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DW package
PW package

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54L	VT652	SN74L	VT652	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		· V
V <sub>IL</sub>	Low-level input voltage			0.8		8.0	٧
٧ı	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
lo <sub>L</sub> ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and VO > VCC.

## SN54LVT652, SN74LVT652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	750	T 0011DITIONS		SN5	4LVT652	;	SN7	4LVT652		
PARAMETER	TES	T CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNIT
VIK	V <sub>CC</sub> = 2.7 V,	l <sub>I</sub> = -18 mA				-1.2			-1.2	V
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = 24 mA		2						\ \ \
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
V	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	\ \ \
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V	Control pins			10			10	
l <sub>l</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	] .			-5			-5	
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_1$ or $V_0 = 0$ to 4.5	5 V						±100	μΑ
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75			75			μА
Ihold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or B ports	-75			-75			μΛ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1 :	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high		0.13	0.19		0.13	0.19	
lcc		$I_{O}=0$ ,	Outputs low		8.8	12		8.8	12	mA
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled		0.13	0.19		0.13	0.19	
Δlcc¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ o		- 0.6 V,			0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0									pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

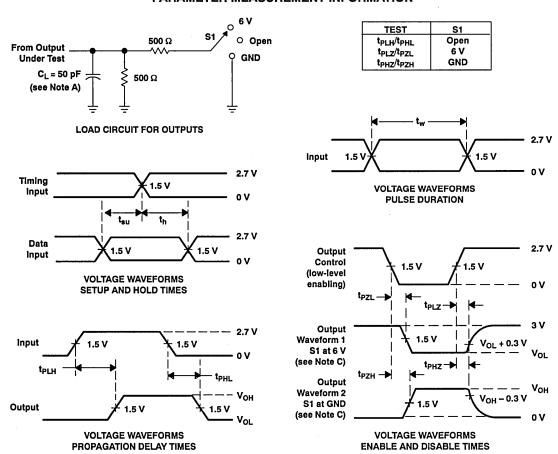
MAY 1992-REVISED NOVEMBER 1992

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)

			s	N54LVT6	52		SN	74LVT65	52	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> =	3.3 V ±	0.3 V	V <sub>CC</sub> = 2.7 V	UNIT
	(	(001101)	MIN	MAX	MAX	MIN	TYP	MAX	MAX	
f <sub>max</sub>										MHz
t <sub>PLH</sub>	CLKBA or	A or B					3.9			ns
t <sub>PHL</sub>	CLKAB	AOIB					4			ns
t <sub>PLH</sub>	A or B	B or A					3.1			ns
t <sub>PHL</sub>	AUB	BUIA					3.2			115
t <sub>PLH</sub>	SBA or SAB‡	A or B					4			ns
t <sub>PHL</sub>	SBA OF SAB	AUIB					4.6			115
t <sub>PZH</sub>	OEBA	A					3.2			ns
t <sub>PZL</sub>	OEBA						3.5			115
t <sub>PHZ</sub>	OEBA	Α					4.3			ns
t <sub>PLZ</sub>	OEBA	^					3.7			120
t <sub>PZH</sub>	OEAB	В					•			ns
t <sub>PZL</sub>	OEAB	B						·		118
t <sub>PHZ</sub>	OEAB	В								no
t <sub>PLZ</sub>	UEAB	ь								ns

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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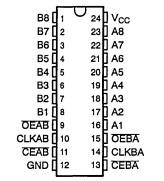
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- **Supports Mixed-Mode Signal Operation** (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF,
- Latch-Up Performance Exceeds 500 mA Per **JEDEC Standard JESD-17**
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPS

#### description

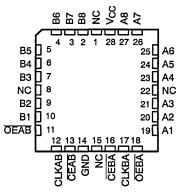
These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

SN54LVT2952...JT PACKAGE SN74LVT2952 ... DW OR PW PACKAGE (TOP VIEW)



SN54LVT2952...FK PACKAGE (TOP VIEW)



NC-No internal connection

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVT2952 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT2952 is characterized for operation from -40°C to 85°C.

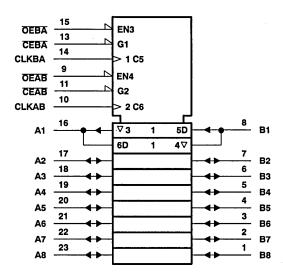
# SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992—REVISED NOVEMBER 1992

#### **FUNCTION TABLE<sup>†</sup>**

	INPU	ITS		OUTPUT
CEAB	CLKAB	OEAB	Α	В
Н	Х	L	Х	B <sub>0</sub> ‡
×	L	L	X	B <sub>0</sub> ‡
L	<b>†</b>	L	L	L
L	t	L	H	Н
х	Х	н	Х	z

<sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.

#### logic symbol§

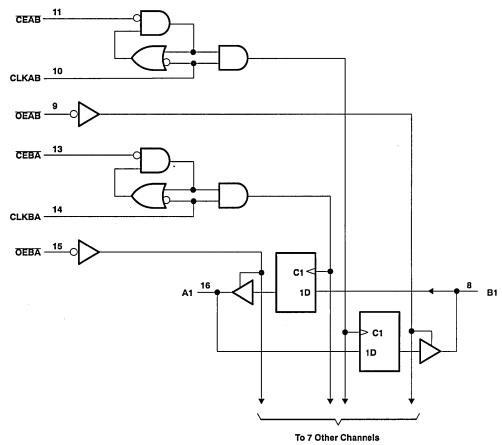


<sup>§</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and PW packages.

<sup>‡</sup> Level of B before the indicated steady-state input conditions were established.

# SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

### logic diagram (positive logic)



Pin numbers shown are for DW, JT, and PW packages.

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	are manage training of the operation of the compensation of the co
Si	upply voltage range, V <sub>CC</sub> 0.5 V to 4.6 V
	nput voltage range, V <sub>I</sub> (see Note 1)
Vo	oltage range applied to any output in the high state or power-off state, $V_0$ (see Note 1) $-0.5$ V to 7 V
C	current into any output in the low state, IO: SN54LVT2952
	SN74LVT2952
C	current into any output in the high state, IO (see Note 2): SN54LVT2952

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

#### recommended operating conditions

			SN54LV	T2952	SN74LV	T2952	UNIT
			MIN	MAX	MIN	MAX	ONLI
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	>
VI	Input voltage			5.5		5.5	<b>V</b>
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
loL‡	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ů

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		T CONDITIONS		SN54	LVT295	2	SN74	LVT295	2	UNIT
PARAMETER	l les	T CONDITIONS		MIN	TYP	MAX	MIN	TYP†	MAX	UNII
Vik	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
.,	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						·
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	$V_{CC} = 2.7 \text{ V},$	l <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
v	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	v
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control nine			±1			±1	
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V	Control pins			10			10	,
l <sub>l</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20	μΑ
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			-5	
loff	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μΑ
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75			75			 μA
Ihold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or B ports	-75			75			μΑ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
I <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high		0.13	0.19	-	0.13	0.19	
lcc	V <sub>CC</sub> = 3.6 V,	l <sub>O</sub> = 0,	Outputs low		8.8	12		8.8	12	mA
·CU	V <sub>I</sub> = V <sub>CC</sub> or GND	·	Outputs disabled		0.13	0.19		0.13	0.19	
Δlcc¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at $V_{CC}$ o		- 0.6 V,			0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0									pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>\*</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

<sup>1</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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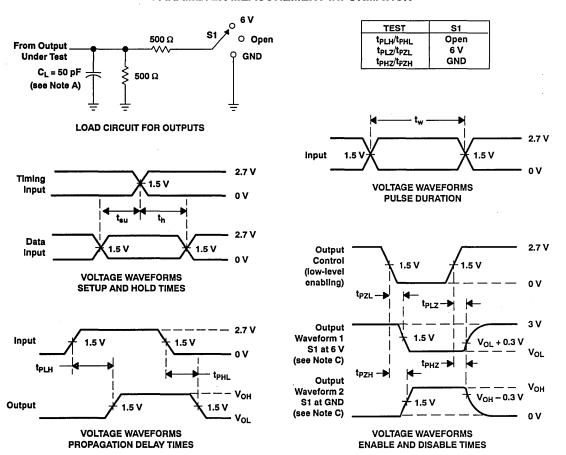
switching characteristics over recommended operating free-air temperature range,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

			s	SN54LVT2952			SN74LVT2952				
PARAMETER	FROM (INPUT)		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		V <sub>CC</sub> = 2.7 V	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		0.3 V	V <sub>CC</sub> = 2.7 V	דואט	
		(0011-01)	MIN	MAX	MAX	MIN	TYP	MAX	MAX	7	
f <sub>max</sub>										MHz	
t <sub>PLH</sub>	CLKBA or	A or B					3.5			ns	
t <sub>PHL</sub>	CLKAB	AUIB					3.6				
t <sub>PZH</sub>	OEBA or	A or B					3.2				
t <sub>PZL</sub>	OEAB	AOIB					3.5		l	ns	
t <sub>PHZ</sub>	OEBA or	A or B					4.3				
t <sub>PLZ</sub>	OEAB	AOIB					3.7			ns	

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

	General Information
	ABT Octals
	ABT Widebus™ 3
	ABT Widebus+™ 4
	ABT Memory Drivers
	ABT 25-Ω Incident-Wave Switching Drivers
	Futurebus+/BTL Transcelvers 7
-	JTAG SCOPE™ Testability Devices
	LVT Octals
	LVT Widebus™ 10
	Application Notes and Articles
	ABT Characterization Information
	Mechanical Data

#### LVT Widebus™

#### **Features**

- EPICIIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode circuitry
- Expanded V<sub>CC</sub> range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- Widebus<sup>™</sup> and UBT <sup>™</sup> architectures
- JEDEC SSOP (Widebus™) and EIAJ TSSOP (Shrink Widebus™) packaging
- TI has established an alternate source

#### **Benefits**

- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized, scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I<sub>CCZ</sub>) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- 16- and 18-bit densities for flexible integration
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
- Standardization that comes from a common product approach

#### SN54LVT16244, SN74LVT16244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged In Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### SN54LVT16244 . . . WD PACKAGE SN74LVT16244 . . . DGG OR DL PACKAGE (TOP VIEW)

		_	_	
10E[	1	U	48	20E
1Y1[	2		47	1A1
1Y2	3		46	1A2
GND	4		45	GND
1Y3[	5		44	1A3
1Y4[	6		43	] 1A4
Vcc	7		42	] v <sub>cc</sub>
2Y1[	8		41	] 2A1
2Y2[	9		40	2A2
GND[	10		39	GND
2Y3[]	11		38	] 2A3
2Y4[	12		37	] 2A4
3Y1[	13		36	] 3A1
3Y2[	14		35	] 3A2
GND[	15		34	] GND
3Y3[]	16		33	] 3A3
3Y4[]	17		32	] 3A4
Vcc[	18		31	] v <sub>cc</sub>
4Y1[	19		30	] 4A1
4Y2[]	20		29	] 4A2
GND[	21		28	GND
4Y3[]	22		27	4A3
4Y4[]	23		26	] 4A4
40E[	24		25	30E

#### description

The 'LVT16244 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical  $\overline{\text{OE}}$  (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16244 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16244 is characterized for operation from –40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

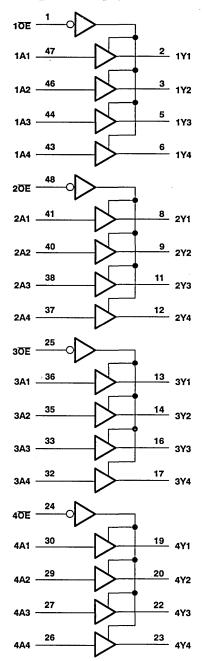
## SN54LVT16244, SN74LVT16244 3.3-V ABT 16-BÍT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### logic symbol<sup>†</sup>

10E 30E 40E	1 48 25 24	EN1 EN2 EN3 EN4			
1A1			1	1 ▽	2
1A2	46				3
1A3	44	┌			5
1A4	43				6
2A1	41		1	2 ▽	8
2A2	40				9
2A3	38	┢			11
A4	37	┢			12
	36	$\vdash$	1	3 ▽	13
A1	35	├		3 🗸	14
A2	33	<u> </u>			16
A3	32	<b> </b>			17
A4	30				19
A1	29	<u> </u>	1	4 ▽	20
A2	27	<u> </u>			22
A3	26	<b> </b>			23

<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



### SN54LVT16244, SN74LVT16244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

## FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	н
н	Х	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> –0.5 V	′ to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_0$ (see Note 1)0.5	V to 7 V
Current into any output in the low state, IO: SN54LVT16244	. 96 mA
SN74LVT16244	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16244	. 48 mA
SN74LVT16244	. 64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	-50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	-50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DGG package	0.6 W
DL package	. 0.85 W
Storage temperature range –65°C	to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

#### recommended operating conditions

	_		SN54LV	T16244	SN74LV		
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
ViH	High-level input voltage	2		2		٧	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	٧	
۷ <sub>I</sub>	Input voltage		5.5		5.5	V	
ЮН	High-level output current		-24		-32	mA	
lOL	Low-level output current			24		32	mA
loL‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

### SN54LVT16244, SN74LVT16244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	RAMETER TEST CONDITIONS			SN54	SN54LVT16244			SN74LVT16244			
PAHAMETER			MIN	TYP	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT		
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	l <sub>I</sub> = -18 mA				-1.2			-1.2	V	
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = 8 mA		2.4			2.4			V	
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						\ <b>V</b>	
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2				
	$V_{CC} = 2.7 \text{ V},$	I <sub>OL</sub> = 100 μA				0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5		
v	V <sub>CC</sub> = 3 V,	l <sub>OL</sub> = 16 mA				0.4			0.4	v	
$V_{OL}$	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	<b>,</b>	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA			0.55						
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55		
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V				10			10		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1		
l <sub>l</sub>	$V_{CC} = 3.6 \text{ V},$	V <sub>I</sub> = V <sub>CC</sub>	Data sina			1			1	μΑ	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins			<b>-</b> 5			<b>-</b> 5		
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_1 \text{ or } V_0 = 0 \text{ to 4.5}$	5 V						±100	μА	
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A inputs	75			75			^	
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Ainpuis	<b>–</b> 75			<b>-</b> 75			μΑ	
l <sub>ozh</sub>	$V_{CC} = 3.6 \text{ V},$	V <sub>O</sub> = 3 V				1			1	μА	
I <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			1	μΑ	
			Outputs high			0.1			0.1		
Icc	$V_{CC} = 3.6 \text{ V},$	l <sub>O</sub> = 0,	Outputs low			5			5	mA	
icc			Outputs disabled			0.1			0.1	111/4	
Δl <sub>CC</sub> §	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2			0.2	mA		
Ci	V <sub>1</sub> = 3 V or 0									pF	
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0	_								pF	

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

# switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

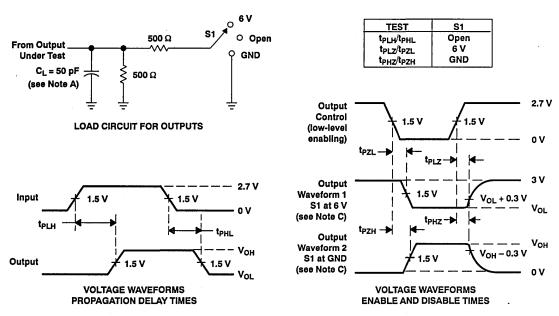
			NS .	SN54LVT16244			SN74LVT16244					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V	± 0.3 V	V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> =	3.3 V ±	0.3 V	V <sub>CC</sub> = 2.7 V	UNIT		
	(1111 01)	( 01)	(100176	(0011 01)	MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t <sub>PLH</sub>	^	v					2.5			20		
t <sub>PHL</sub>	A	T					2.6			ns		
t <sub>PZH</sub>	QE	V					2.8			ns		
t <sub>PZL</sub>	OE .	T					3.3			115		
t <sub>PHZ</sub>	ŌĒ	· v					3.8			20		
t <sub>PLZ</sub>	QE	T					2.9			ns		



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>1</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\pm}$  10 MHz,  $Z_{o}$  = 50  $\Omega$ ,  $t_{f}$   $_{z}$  2.5 ns,  $t_{f}$   $_{z}$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments
   Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink
   Small-Outline (DL) and Thin Shrink
   Small-Outline (DGG) Packages and 380-mil
   Fine-Pitch Ceramic Flat Packages (WD)
   Using 25-mil Center-to-Center Spacings

SN54LVT16245... WD PACKAGE SN74LVT16245... DGG OR DL PACKAGE (TOP VIEW)

1DIR	1	U	48	10E
1B1 [			47	1A1
1B2				1A2
GND [				GND
1B3 [				1A3
1B4 [	6			1A4
V <sub>CC</sub> [	7		42	] v <sub>cc</sub>
1B5 [	8		41	1A5
1B6 [				1A6
GND [	10			GND
1B7 🛚	11		38	1A7
1B8 🛚			37	1A8
2B1 [	13		36	2A1
2B2 [	14		35	] 2A2
GND [	15			GND
2B3 [	16		33	2A3
2B4 [			32	2A4
v <sub>cc</sub> [	18		31	] v <sub>cc</sub>
2B5 [				2A5
2B6 [			29	] 2A6
GND [				gnd
2B7 🛚				2A7
2B8 🛚				2A8
2DIR [	24		25	20E
				ı

#### description

The 'LVT16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16245 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16245 is characterized for operation from -40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

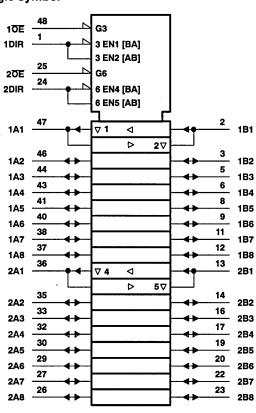


## FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION			
ŌĒ	DIR				
L	L	B data to A bus			
L	н	A data to B bus			
Н	х	Isolation			

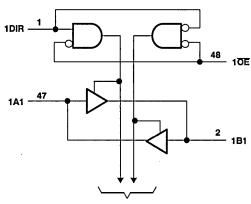
#### logic symbol<sup>†</sup>

**PRODUCT PREVIEW** 

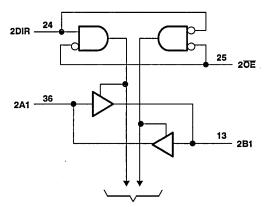


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



To 7 Other Channels



To 7 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16245
SN74LVT16245
Current into any output in the high state, IO (see Note 2): SN54LVT16245
SN74LVT16245
Input clamp current, I <sub>IK</sub> (V <sub>1</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DGG package
DL package
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54LV	SN54LVT16245		SN74LVT16245	
			MIN	MAX	MIN	MAX	UNIT
Vcc	V <sub>CC</sub> Supply voltage		2.7	3.6	2.7	3.6	V
٧ <sub>IH</sub>	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
٧ <sub>I</sub>	Input voltage			5.5		5.5	V
10H	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
lo <sub>L</sub> ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and VO > VCC.

MAY 1992-REVISED NOVEMBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16245			SN74LVT16245			UNIT		
PAHAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	TYP	MAX	UNII	
$V_{IK}$ $V_{CC} = 2.7 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2			-1.2	٧			
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v	
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						] `	
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2				
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA	OL = 100 μA			0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5		
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	<u> </u>	
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5		
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55					
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control mino			±1		•	±1		
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V	Control pins			10			10	μА	
i <sub>i</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§			1			1		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			-5	5	
loff	$V_{CC} = 0$ , $V_{I}$ or $V_{O} = 0$ to 4.5 V							±100	μΑ		
	V <sub>CC</sub> = 3 V,	V <sub>1</sub> = 0.8 V	A or B ports	75			75				
Ihold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or B ports	-75	- 1		-75			μΑ	
l <sub>ozh</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μA	
lozL	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V					-1			-1	μΑ	
			Outputs high	puts high 0.1		0.1					
lcc	$V_{CC} = 3.6 \text{ V}, \qquad I_{O} = 0,$	l <sub>O</sub> = 0,	Outputs low			. 5			5	mA	
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			0.1			0.1		
Δlcc¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2			0.2	mA		
Ci	V <sub>I</sub> = 3 V or 0									pF	
Cio	V <sub>O</sub> = 3 V or 0								pF		

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

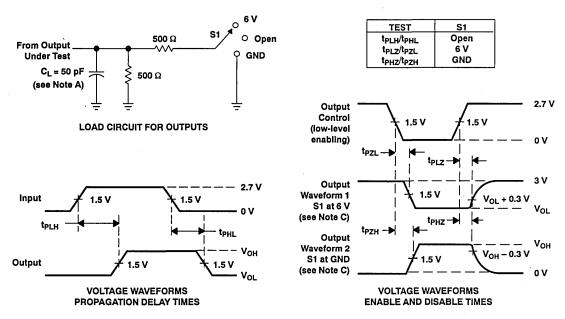
<sup>&</sup>lt;sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

MAY 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments
   Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### SN54LVT16373... WD PACKAGE SN74LVT16373... DGG OR DL PACKAGE (TOP VIEW)

		<del></del>
10E [	1, U	48 1LE
1Q1 [	2	47 D1
1Q2 [	3	46 1D2
GND [	4	45 GND
1Q3 [	5	44 D3
1Q4 [	6	43 D4
v <sub>cc</sub> [	7	42 V <sub>CC</sub>
1Q5 [		41 2 1D5
1Q6 [		40 D6
GND [		39 GND
107		38 🛚 1D7
1Q8 [		37 D8
2Q1 [		36 2D1
2Q2 [		35 2D2
GND [		34 [] GND
2Q3 [		33 2D3
2Q4 [		32 2D4
v <sub>cc</sub> [	18	31 V <sub>CC</sub>
2Q5 [		30 2D5
2Q6 [		29 2D6
GND [		28 GND
2Q7 [		27 2D7
2Q8 [		26 2D8
20E [	24	25 2LE

#### description

The 'LVT16373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.



#### SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

#### description (continued)

The SN74LVT16373 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16373 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16373 is characterized for operation from -40°C to 85°C.

## FUNCTION TABLE (each 8-bit section)

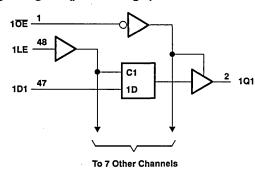
	INPUTS	OUTPUT	
OE LE D			Q
L	Н	Н	Н
L	Н	L	L
L	L	X	$Q_0$
н	X	X	z

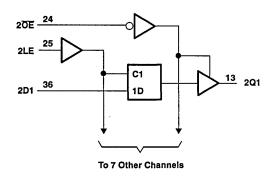
### logic symbol<sup>†</sup>

#### 10E 1EN 48 СЗ 1LE 24 20E 2EN 25 2LE C4 47 1D1 3D 1 ▽ 1Q1 46 3 1D2 1Q2 44 5 1D3 **1Q3** 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 **1Q7** 37 12 1Q8 1D8 36 13 2D1 4D 2 ▽ 2Q1 35 14 2D2 2Q2 33 16 2D3 2Q3 32 17 2Q4 2D4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 207 26 23 2D8 2Q8

## <sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)





## SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

absolute maximum	ratings ove	r operating free-air	temperature range	(unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> −0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1) −0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16373
SN74LVT16373
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT16373
SN74LVT16373
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, $I_{OK}$ ( $V_O < 0$ )
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package 0.6 W
DL package
Storage temperature range — 65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. This current will only flow when the output is in the high state and VO > VCC.

#### recommended operating conditions

1			SN54LV	SN54LVT16373		SN74LVT16373	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
lo <sub>L</sub> ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

# SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16373			SN74	UNIT		
PARAMETER	153	CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	l <sub>I</sub> = -18 mA				-1.2			-1.2	٧.
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = – 8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						· •
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
<b>V</b> OL	V <sub>CC</sub> = 3 V,	i <sub>OL</sub> = 32 mA				0.5			0.5	V
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA			0.55					
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	ı
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V				10			10	
1.	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	μΑ
lı	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	Data pins			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins			-5			-5	
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_1$ or $V_0 = 0$ to 4.5	5 V						±100	μΑ
h	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V		75			75			μА
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Data inputs	75			-75			
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
l <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			1	μА
			Outputs high			0.1			0.1	
1 <sub>CC</sub>	V <sub>CC</sub> = 3.6 V,	$I_{O} = 0$ ,	Outputs low			5			5	mA
'CC	V <sub>I</sub> = V <sub>CC</sub> or GND Outputs disabled				0.1			0.1	mA	
ΔI <sub>CC</sub> §	$V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND					0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									pF
Co	V <sub>O</sub> = 3 V or 0									pF

 $<sup>^{\</sup>dagger}$  All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

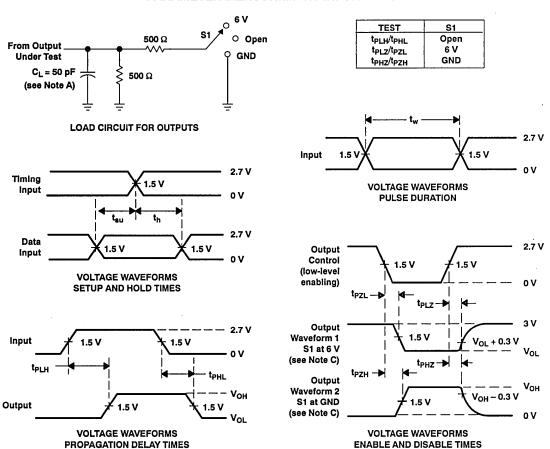
<sup>&</sup>lt;sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

## SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

MAY 1992-REVISED NOVEMBER 1992

•	State-of-the-Art Advanced BiCMOS
	Technology (ABT) Design for 3.3-V
	Operation and Low-Static Power
	Dissipation

- Member of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### SN54LVT16374... WD PACKAGE SN74LVT16374... DGG OR DL PACKAGE (TOP VIEW)

10E [	, U	40	] 1CLK
101			1D1
1Q2 [			] 1D2
GND [			GND
1Q3 [		44	] 1D3
1Q4 [		43	] 1D4
Vcc [	7	42	] v <sub>cc</sub>
1Q5 [	8	41	1D5
1Q6 [	9	40	1D6
GND [	10	20	CND
1Q7 [	11	38	1D7 1D8
1Q8 [	12	37	1D8
2Q1 [		36	J 2D1
2Q2 [			2D2
GND [	15	34	GND
2Q3 [	16	33	2D3
2Q4 [	17	32	] 2D4
Vcc [	18	31	] v <sub>cc</sub>
2Q5 [	19	30	2D5
2Q6 [	20	29	2D6
GND [		28	GND
2Q7 [		27	2D7
2Q8 [	23		2D8
20E [	24	25	2CLK

#### description

The 'LVT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16374 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus is a trademark of Texas Instruments Incorporated.



# MAY 1992-REVISED NOVEMBER 1992 description (continued)

The SN54LVT16374 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16374 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE** (each flip-flop)

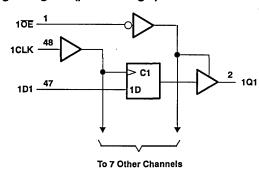
(									
	INPUTS	OUTPUT							
ŌĒ	CLK	D	Q						
L	Ť	Н	Н						
L	. 1	L	L						
L	L	Χ.	Qo						
н	Х	X	ž						

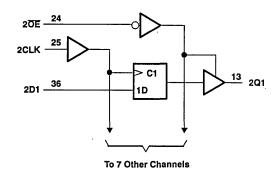
#### logic symbol†

PRODUCT PREVIEW

#### 10E 1EN 48 1CLK C1 24 20E 2EN 25 2CLK C2 47 2 1D1 1D 1 ▽ 1Q1 46 3 1D2 1Q2 5 44 1D3 1Q3 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 **1Q6** 38 11 1D7 1Q7 37 12 1D8 1Q8 36 13 2D 2D1 2 ▽ 2Q1 35 14 2D2 2Q2 33 16 2D3 2Q3 32 17 2D4 2Q4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 2D8 2Q8

#### logic diagram (positive logic)





<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MAY 1992-REVISED NOVEMBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub>
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16374
SN74LVT16374
Current into any output in the high state, IO (see Note 2): SN54LVT16374
SN74LVT16374
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package
DL package
Storage temperature range65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

#### recommended operating conditions

			SN54LV	SN54LVT16374		Γ16374	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
ViH	High-level input voltage		2		2		V
V <sub>I</sub> L	Low-level input voltage			0.8		0.8	V
٧Į	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
loL‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	40	85	ŝ

<sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

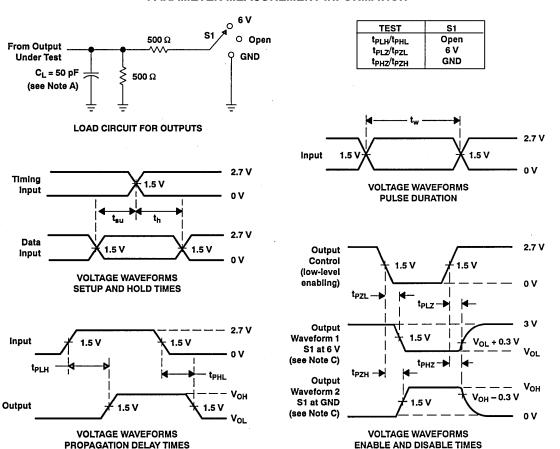
PARAMETER	TEST CONDITIONS -			SN54LVT16374			SN74	LVT1637	4	UNIT	
PAHAMETER				MIN	TYP	MAX	MIN	TYP	MAX	UNII	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧	
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	$V_{CC} = MIN \text{ to MAX}^{\ddagger},  I_{OH} = -100 \mu\text{A}$					V <sub>CC</sub> -0.2				
\ <u>'</u>	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v	
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						V	
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2				
	V <sub>CC</sub> = 2.7 V,	i <sub>OL</sub> = 100 μA				0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5		
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	.,	
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	٧	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				i	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	ĺ	
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10			10		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	μΑ	
lı	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>				1			1		
,	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0	Data pins			-5			<b>-</b> 5		
loff	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5	5 V						±100	μΑ	
	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V		75			75			μА	
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	Data inputs	-75			-75				
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ	
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ	
			Outputs high			0.1			0.1		
laa	V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0,	Outputs low			5			5	m A	
lcc	V <sub>I</sub> = V <sub>CC</sub> or GND Outputs disabled					0.1			0.1	mA	
Δlcc <sup>§</sup>	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND					0.2			0.2	mA	
Ci	V <sub>I</sub> = 3 V or 0									рF	
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0									pF	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

MAY 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\leq}$  10 MHz,  $Z_{0}$  = 50  $\Omega$ ,  $t_{f}$   $_{\leq}$  2.5 ns,  $t_{f}$   $_{\leq}$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

SN54LVT16500 . . . WD PACKAGE SN74LVT16500 . . . DGG OR DL PACKAGE (TOP VIEW)

ОЕАВ[	<sub>1</sub> U	56 GND
LEAB[		55 CLKAB
A1 [		54 🛭 B1
GND[		53 GND
A2[		52 B2
А3[		51 B3
V <sub>CC</sub> [	7	50 V <sub>CC</sub>
A4[	8	49 ] B4
A5[	9	48 🛮 B5
A6[	10	47 🛮 B6
GND	11	46] GND
A7[		45 B7
A8[		44 🕽 B8
A9[		43 🛮 B9
A10[		42 B10
A11 [		41 D B11
A12[		40 B12
GND		39 GND
A13[		38 B13
A14[		37 B14
A15		36 B15
v <sub>cc</sub> [		35 🛚 V <sub>CC</sub>
A16[		34 B16
A17		33 D B17
GND		32 ] GND
A18		31 B18
OEBAL		30 CLKBA
LEBA[	28	29 GND

#### description

The 'LVT16500 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{CLKAB}$  is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of  $\overline{CLKAB}$ . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{\text{OEBA}}$ , LEBA, and  $\overline{\text{CLKBA}}$ . The output enables are complementary (OEAB is active high, and  $\overline{\text{OEBA}}$  is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus and UBT are trademarks of Texas Instruments Incorporated.



MAY 1992-REVISED NOVEMBER 1992

#### description (continued)

The SN74LVT16500 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16500 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

	ОИТРИТ			
OEAB	LEAB	CLKAB	Α	В
L	Х	Х	Х	Z
н	н	X	L	L
н	н	X	Н	н
н	L	<b>↓</b>	L	L
н	L	<b>↓</b>	Н	н
н	L	Н	Х	B <sub>0</sub> ‡ ·
Н	L	L	Х	B <sub>0</sub> ‡ · B <sub>0</sub> §

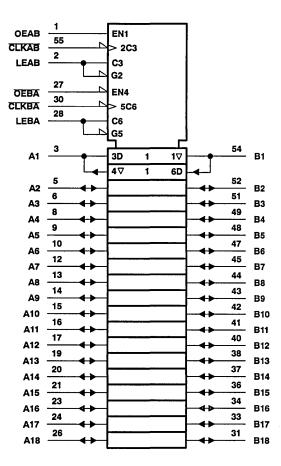
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

<sup>&</sup>lt;sup>‡</sup> Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

MAY 1992-REVISED NOVEMBER 1992

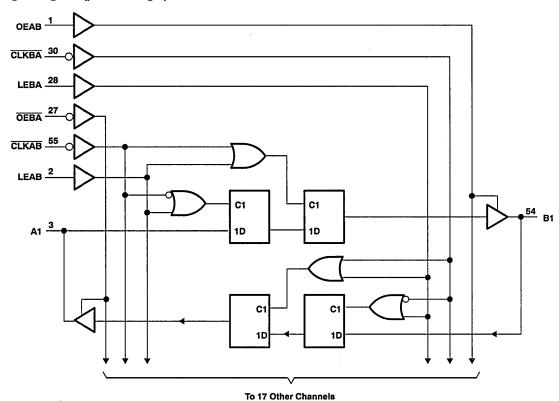
# logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MAY 1992-REVISED NOVEMBER 1992

#### logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> –0.5 V	' to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high state or power-off state, $V_0$ (see Note 1)0.5	V to 7 V
Current into any output in the low state, Io: SN54LVT16500	. 96 mA
SN74LVT16500	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16500	. 48 mA
SN74LVT16500	. 64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	-50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	-50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.



# SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

## recommended operating conditions

			SN54LV	SN54LVT16500		SN74LVT16500		
			MIN	MAX	MIN MAX		UNIT	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V	
VIH	High-level input voltage		2		2		V	
VIL	Low-level input voltage			0.8		0.8	V	
Vı	Input voltage			5.5		5.5		
Іон	High-level output current			-24		-32	mA	
loL	Low-level output current			24		32	mA	
I <sub>OL</sub> †	Low-level output current			48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	ç	

<sup>&</sup>lt;sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

# SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BÍT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SN54LVT16500			SN74	LVT1650	0	UNIT
PARAMETER				MIN	TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	l <sub>i</sub> = -18 mA				-1.2			-1.2	V
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	l <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						•
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA			,		2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2	
	$V_{CC} = 2.7 \text{ V},$	I <sub>OL</sub> = 24 mA				0.5			0.5	
V	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	· •
·	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	μΑ
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V				10			10	
l <sub>l</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			<b>-</b> 5	
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μΑ
L	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75			75			μΑ
l <sub>hoid</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A of B ports	-75			<b>–7</b> 5			
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high			0.1			0.1	
lcc		$I_O = 0$ ,	Outputs low			5			5	mA
'CC			Outputs disabled			0.1			0.1	
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND				-	0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0									pF

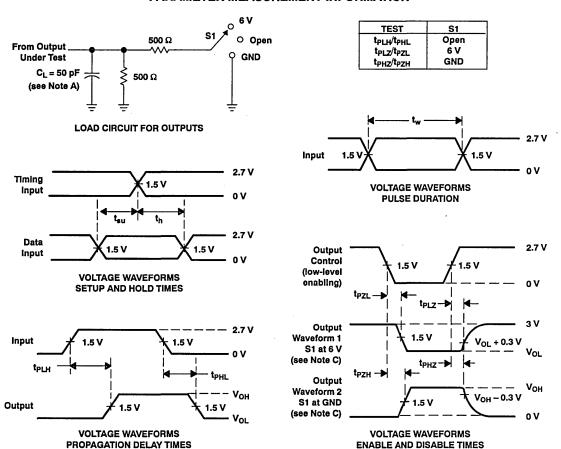
<sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

MAY 1992-REVISED NOVEMBER 1992

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low-Static Power** Dissipation
- **Member of the Texas Instruments** Widebus™ Family
- **Supports Mixed-Mode Signal Operation** (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- UBT ™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Filp-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V<sub>OLP</sub> (Output Ground Bounce)  $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Lavout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) **Using 25-mil Center-to-Center Spacings**

SN54LVT16501 . . . WD PACKAGE SN74LVT16501 . . . DGG OR DL PACKAGE (TOP VIEW)

OEAB[	70	56	GND
LEAB[			CLKAB
A1[		54 F	B1
GND[			GND
A2[			B2
A3[			B3
Vcc		50	Vcc
A4[		49	B4
A5[			B5
A6[			В6
GND[			GND
A7[		45	B7
		44	В8
A9[			В9
A10			B10
A11			B11
A12			B12
GND[			GND
A13[			B13
A14[	20		B14
A15[	21		B15
v <sub>cc</sub> [	22	35	l v <sub>cc</sub>
A16[		34	B16
A17[	24	33	B17
GND[		32	GND
A18[		31	B18
OEBA[	27	30	CLKBA
LEBA[	28	29	GND

#### description

The 'LVT16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA). and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



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#### description (continued)

The SN74LVT16501 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16501 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

	OUTPUT			
OEAB	LEAB	CLKAB	Α	В
L	X	X	Х	Z
н	Н	X	L	L
н	Н	X	Н	н
H-	L	†	L	L
н	L	†	Н	Н
Н	L	Н	Х	B₀‡
Н	L	L	Х	В <sub>0</sub> ‡ В <sub>0</sub> §

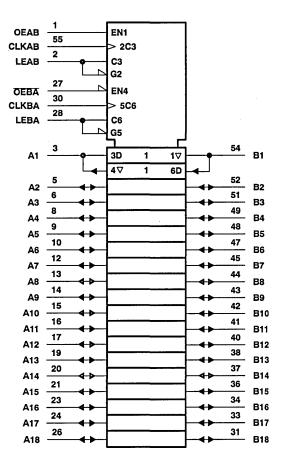
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

<sup>§</sup> Output level before the indicated steady-state input conditions were established.

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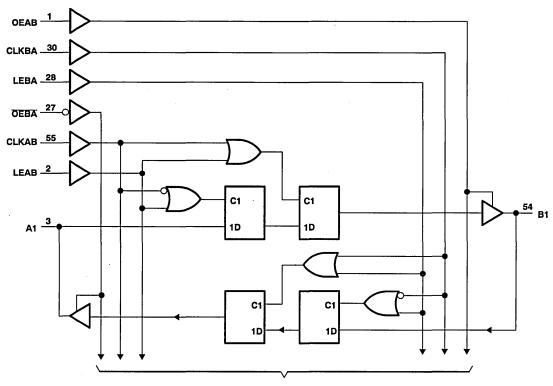
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

MAY 1992-REVISED NOVEMBER 1992

#### logic diagram (positive logic)



To 17 Other Channels

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	-0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, IO: SN54LVT16501	96 mA
SN74LVT16501	
Current into any output in the high state, Io (see Note 2): SN54LVT16501	48 mA
SN74LVT16501	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and  $V_0 > V_{CC}$ .



# SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

## recommended operating conditions

			SN54LV	SN54LVT16501		SN74LVT16501	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	•	2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage			5.5		5.5	V
Іон	High-level output current			-24		-32	mA
I <sub>OL</sub>	Low-level output current			24		32	mA
I <sub>OL</sub> †	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>†</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

MAY 1992-REVISED NOVEMBER 1992

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16501			SN74LVT16501			UNIT		
FARAMETER	TEST CONSTITIONS			MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
V	V <sub>CC</sub> = 2.7 V,	$I_{OH} = -8 \text{ mA}$		2.4			2.4			v	
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						\	
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2				
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5		
V	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v	
$V_{OL}$	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	v	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				7	
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	μА	
	V <sub>CC</sub> = 0 or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10	ĺ		10		
li	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V	A or B ports§			20			20		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>				1		-	1		
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			-5		
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μА	
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B norto	75			75				
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or B ports	-75			-75			μА	
l <sub>ozh</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ	
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ	
			Outputs high			0.1			0.1		
Icc	V <sub>CC</sub> = 3.6 V,	l <sub>O</sub> = 0,	Outputs low			5			5	mA	
'CC	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			0.1	,		0.1	III/A	
Δl <sub>CC</sub> ¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2			0.2	mA		
Ci	V <sub>I</sub> = 3 V or 0									pF	
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0									pF	

 $<sup>^{\</sup>dagger}$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

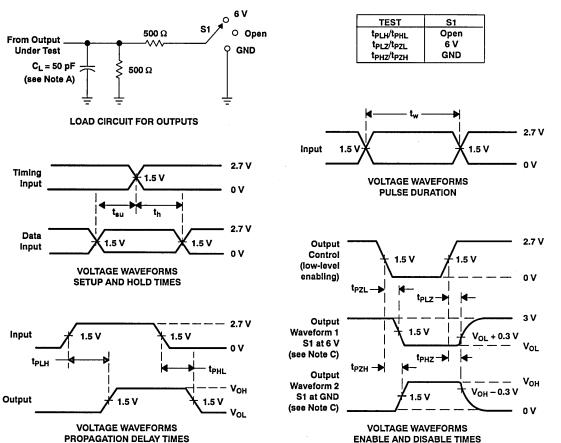
For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

•	State-of-the-Art Advanced BiCMOS
	Technology (ABT) Design for 3.3-V
	Operation and Low-Static Power
	Dissipation
•	Member of the Texas Instruments

- Member of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

#### SN54LVT16543... WD PACKAGE SN74LVT16543... DGG OR DL PACKAGE (TOP VIEW)

10EAB[	1 U	56	] 10EBA
1LEAB	1		1LEBA
1CEAB			1CEBA
GND[			[] GND
1A1 [	5	52	] 1B1
1A2[	6	51	] 1B2
V <sub>CC</sub> [	7	50	] v <sub>cc</sub>
1A3[		49	] 1B3
1A4[	9		] 1B4
1A5[	10		] 1B5
GND[	11	46	] GND
1A6[]			] 1B6
1A7[			] 1B7
1A8[]			] 1B8
2A1 🛭			] 2B1
2A2[]			2B2
2A3[			] 2B3
GND[]			] GND
2A4[]			] 2B4
2A5	20		2B5
2A6[]	21		] 2B6
Vcc			] v <sub>cc</sub>
2A7			] 2B7
2A8[]			] 2B8
GND ]			] GND
2CEAB [			2CEBA
2LEAB	i e		2LEBA
20EAB[	28	29	] 20EBA

#### description

The 'LVT16543 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16543 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16543 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16543 is characterized for operation from -40°C to 85°C.

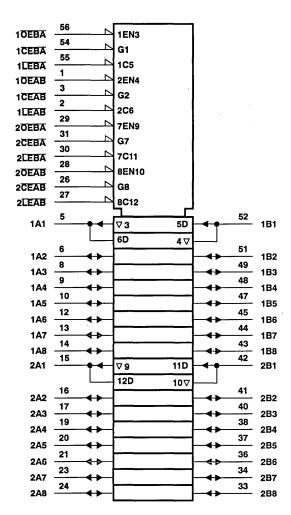
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#### SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

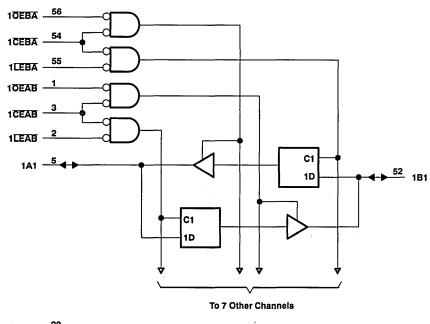
MAY 1992-REVISED NOVEMBER 1992

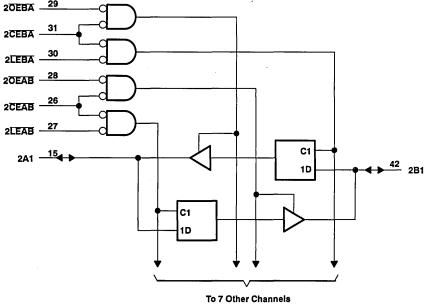
#### logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)





## SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

#### FUNCTION TABLE† (each 8-bit section)

	INPL	JTS		ОПТРИТ
CEAB	LEAB	OEAB	Α	В
н	X	×	Х	Z
×	X	Н	Х	z
L	Н	L	Х	В <sub>0</sub> ‡
L	L	L	L	L
L	L	L	Н	н

<sup>&</sup>lt;sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, vCC0.5 v to 4.6 v
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16543
SN74LVT16543
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT16543
SN74LVT16543
Input clamp current, $I_{iK}(V_i < 0)$
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package
DL package
Storage temperature range

<sup>§</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

			SN54LVT16543		SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage			5.5		5.5	٧
Гон	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
I <sub>OL</sub> ¶	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	. –40	85	°C

<sup>¶</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz



Output level before the indicated steady-state input conditions were established.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_0 > V_{CC}$ .

## SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS		SN54LVT16543			SN74LVT16543			UNIT	
PARAMETER	163	CONDITIONS		MIN	TYP†	MAX	MIN	TYP	MAX	UNII
VIK	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧
	V <sub>CC</sub> = MIN to MAX <sup>‡</sup> ,	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			1 ,
Voн	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						V
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	i <sub>OL</sub> = 100 μA		l		0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
VOL	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	٧
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	μΑ
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10			10	
lį	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V	A or B ports§			20			20	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>				1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			<b>–</b> 5	
I <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V		_				±100	μА
t	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75			75			μА
l <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A OI B POILS	-75			<b>–75</b>			μΛ
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high			0.1			0.1	
lcc	V <sub>CC</sub> = 3.6 V,	$I_0 = 0$ ,	Outputs low			5			5	mA
.00			Outputs disabled			0.1			0.1	
Δlcc¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2			0.2	mA	
Ci	V <sub>i</sub> = 3 V or 0									pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0									pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

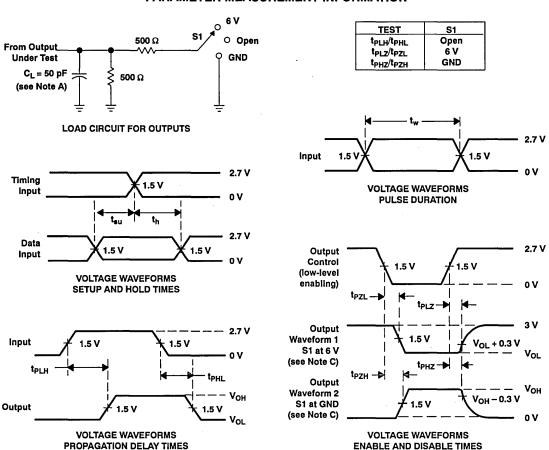
For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_1 \leq 2.5 \text{ ns}$ ,  $t_1 \leq 2.5 \text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

#### SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

<ul> <li>State-of-the-Art Advanced BiCMOS         Technology (ABT) Design for 3.3-V         Operation and Low-Static Power     </li> </ul>	SN74LVT16646	SN54LVT16646 WD PACKAGE N74LVT16646 DGG OR DL PACKAGE (TOP VIEW)				
Dissipation	1DIR [		] 10E			
Member of the Texas Instruments	1CLKAB	1 56	1 1CLKBA			
<i>Widebus</i> ™ Family	1SAB		1SBA			
Supports Mixed-Mode Signal Operation	GND		GND			
(5-V Input and Output Voltages With	1A1 [		1B1			
3.3-V V <sub>CC</sub> )	1A2		1B2			
Supports Unregulated Battery Operation	Vcc		Vcc			
Down to 2.7 V	1A3 [		л 183			
· · · · · · · · · · · · · · · · · ·	1A4 [		П 1B4			
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> <li>0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C</li> </ul>	1A5 [		1B5			
	GND		GND			
ESD Protection Exceeds 2000 V Per     STR 9820 Method 2015: Exceeds	1A6		∏ 1B6			
MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF.	1A7	13 44	П 1B7			
R = 0)	1A8 [	14 43	1B8			
•	2A1 [	15 42	D 2B1			
Latch-Up Performance Exceeds 500 mA Per     LEDEO Object   LEDEO 17	2A2 [	16 41	] 2B2			
JEDEC Standard JESD-17	2A3 [	17 40	2B3			
Bus-Hold Data Inputs Eliminate the Need	GND [	18 39	] GND			
for External Pullup Resistors	2A4 [	19 38	] 2B4			
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> </ul>	2A5 [	20 37	] 2B5			
Minimizes High-Speed Switching Noise	2A6 [		] 2B6			
<ul> <li>Flow-Through Architecture Optimizes PCB</li> </ul>	V <sub>cc</sub> [		] v <sub>cc</sub>			
Layout	2A7 [		] 2B7			
Packaged in Plastic 300-mil Shrink	2A8 [		] 2B8			
Small-Outline (DL) and Thin Shrink	GND [		] GND			
Small-Outline (DGG) Packages and 380-mil	2SAB [		2SBA			
Fine-Pitch Ceramic Flat Packages (WD)	2CLKAB	27 30	2CLKBA			
the contract of the contract o		וחס חחו				

#### description

The 'LVT16646 is a 16-bit bus transceiver designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

2DIR 28

29 20E

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

Using 25-mil Center-to-Center Spacings



#### SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

#### description (continued)

The SN74LVT16646 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16646 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16646 is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE**

INPUTS						DATA I/O		OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Х	Х	t	Х	Х	Х	Input	Unspecified <sup>†</sup>	Store A, B unspecified†
Х	x	Х	<b>†</b>	X	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>
Н	X	<b>†</b>	†	×	х	Input	Input	Store A and B data
Н	X	L	L	X	х	Input disabled	Input disabled	Isolation, hold storage
L	L	X	Х	X	L	Output	Input	Real-time B data to A bus
L	L	Х	L	X	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	L	X	Н	X	Input	Output	Stored A data to B bus

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



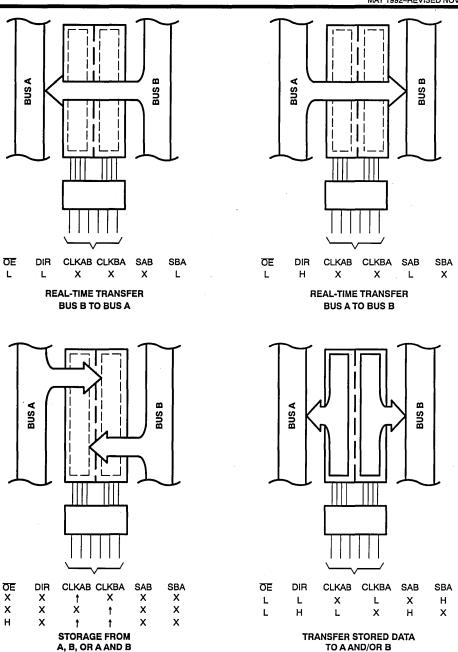


Figure 1. Bus-Management Functions

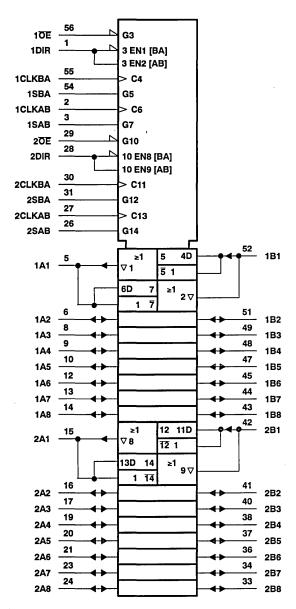


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## SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

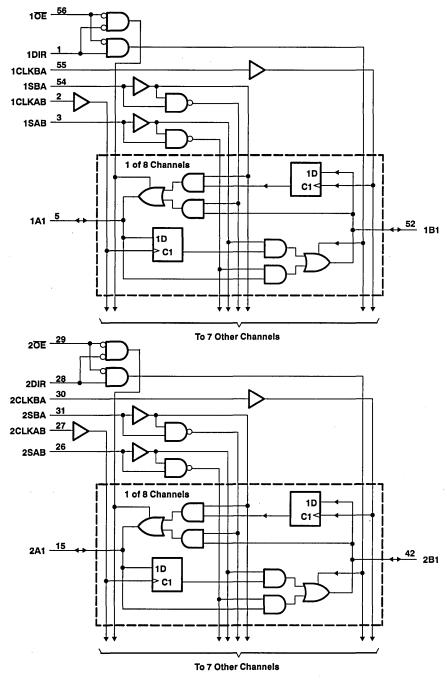
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#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



## SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) $-0.5$ V to 7 V
Current into any output in the low state, Io: SN54LVT16646
SN74LVT16646
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT16646
SN74LVT16646
Input clamp current, $I_{iK}$ ( $V_i < 0$ ) —50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package 0.7 W
DL package 1 W
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

#### recommended operating conditions

			SN54LV	SN54LVT16646		SN74LVT16646	
		•	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage			0.8		8.0	٧
Vı	Input voltage			5.5		5.5	٧
loh	High-level output current			-24		-32	mA
I <sub>OL</sub>	Low-level output current			24		32	mA
l <sub>OL</sub> ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ů

<sup>&</sup>lt;sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz



#### SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

MAY 1992-REVISED NOVEMBER 1992

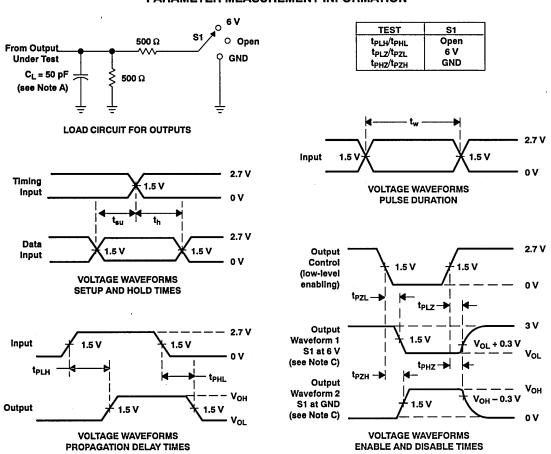
#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SN54	LVT1664	16	SN74LVT16646			UNIT
PARAMETER	le:	T CONDITIONS		MIN	TYP†	MAX	MIN	TYP	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	l <sub>j</sub> = -18 mA				-1.2			-1.2	V
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2				
V	$V_{CC} = 2.7 \text{ V},$	I <sub>OH</sub> = – 8 mA		2.4			2.4			1
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA		2						V
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA					2			
	V <sub>CC</sub> = 2.7 V,	l <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
V	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	<b>V</b>
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	
	V <sub>CC</sub> = 3.6 V,	$V_I = V_{CC}$ or GND	Control pins			±1			±1	μΑ
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V	Control pins			10			10	
l <sub>l</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§			1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>1</sub> = 0				-5			<b>-</b> 5	
l <sub>OFF</sub>	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μA
1	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75		,	. 75			μА
I <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A of B poils	-75			-75			
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μA
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high			0.1			0.1	
lcc	V <sub>CC</sub> = 3.6 V,	$I_{O}=0$ ,	Outputs low			5			5	mA
100			Outputs disabled			0.1			0.1	
Δlcc¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND					0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									pF
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0									pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Lavout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

SN54LVT16652 ... WD PACKAGE SN74LVT16652 ... DGG OR DL PACKAGE (TOP VIEW)

₁ ∪	56	10EBA
2	55	1CLKBA
3	54	1SBA
4	53	GND
5	52	] 1B1
6	51	] 1B2
7	50	] v <sub>cc</sub>
8	49	] 1B3
9		] 1B4
10	47	] 1B5
11		] GND
		] 1B6
		~
		1B8
15		] 2B1
		2B2
		] 2B3
	39	GND
	38	] 2B4
		2B5
		] 2B6
		] v <sub>cc</sub>
		2B7
		2B8
		GND
		2SBA
		2CLKBA
28	29	] 2 <mark>OE</mark> BA
	2 3 4 5 6 7 8 9 10 11 12 13 14	2 555 3 544 4 533 5 522 6 51 7 50 8 49 9 48 10 47 11 46 12 45 13 44 14 43 15 42 16 41 17 40 18 39 19 38 20 37 21 36 22 35 23 34 24 33 25 32 26 31 27 30

#### description

The 'LVT16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

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#### description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16652 is characterized for operation from –40°C to 85°C.

#### **FUNCTION TABLE**

		INPU	rs			DATA	4 I/O†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR PUNCTION
L	Н	L	L	X	Х	Input	Input	Isolation
L	Н	Ť	<b>↑</b> `	X	X	Input	Input	Store A and B data
х	Н	†	L	X	X	Input	Unspecified <sup>‡</sup>	Store A, hold B
н	н	†	<b>†</b>	X <sup>‡</sup>	×	Input	Output	Store A in both registers
L	X	L	1	x	×	Unspecified <sup>‡</sup>	Input	Hold A, store B
L	L	<b>†</b>	. 1	X	X‡	Output	Input	Store B in both registers
L	L	х	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	x	Н	Output	Input	Stored B data to A bus
н	н	X	X	L	×	Input	Output	Real-time A data to B bus
н	н	L	X	н	X	Input	Output	Stored A data to B bus
н	L	L	L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

Select control = H; clocks must be staggered in order to load both registers.

<sup>&</sup>lt;sup>‡</sup> Select control = L; clocks can occur simultaneously.

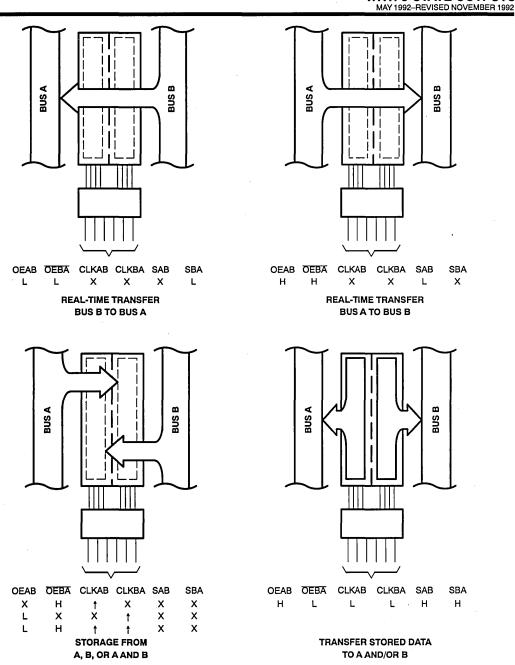
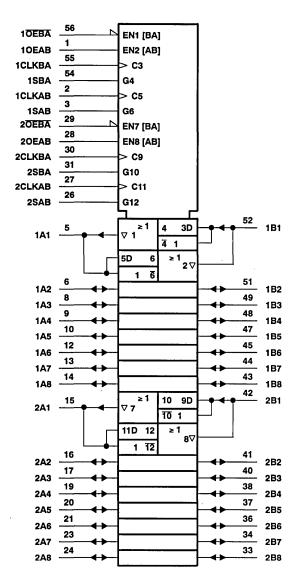


Figure 1. Bus-Management Functions



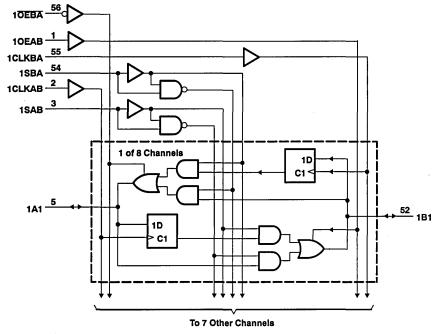
#### SN54LVT16652, SN74LVT16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

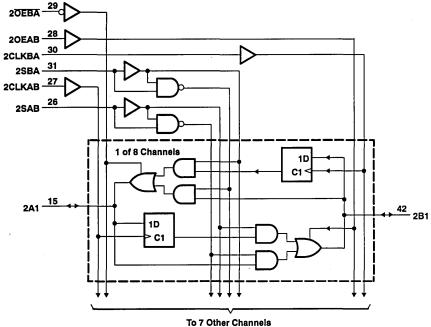
logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted) <sup>†</sup>
Supply voltage range, V <sub>CC</sub> –0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16652
SN74LVT16652
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT16652 48 mA
SN74LVT16652
Input clamp current, $I_{iK}(V_i < 0)$ —50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package 0.7 W
DL package 1 W
Storage temperature range

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		4	SN54LVT16652		SN74LVT16652		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		8.0	٧
Vı	Input voltage			5.5		5.5	٧
I <sub>OH</sub>	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
lo <sub>L</sub> ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	င့

<sup>&</sup>lt;sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

#### SN54LVT16652, SN74LVT16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS MAY 1992-REVISED NOVEMBER 1992

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

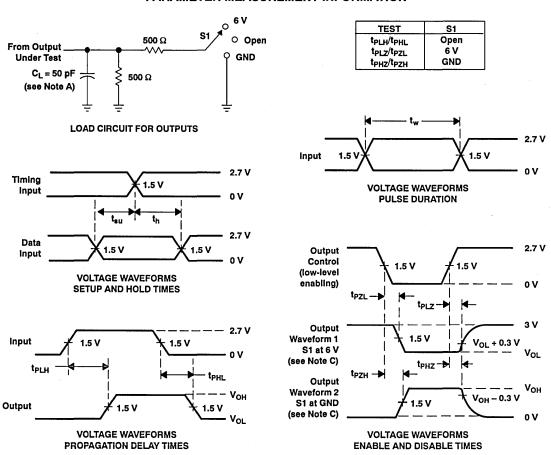
DADAMETER	TEST CONDITIONS			SN54	LVT1665	2	SN74	UNIT		
PARAMETER	TES	CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	V
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},  I_{OH} = -100  \mu A$			V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			
	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA		2.4			2.4			v
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -24 mA		2						V
	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = -32 mA		1			2			
	$V_{CC} = 2.7 \text{ V},$	I <sub>OL</sub> = 100 μA				0.2			0.2	
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5	
V.	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	v
V <sub>OL</sub>	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 32 mA				0.5			0.5	v
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55				
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55	_
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins			±1			±1	μА
	$V_{CC} = 0$ or $MAX^{\ddagger}$ ,	V <sub>I</sub> = 5.5 V				10			10	
1 <sub>1</sub>	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V				20			20	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>	A or B ports§	1		1			1	
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			-5	
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	$V_I$ or $V_O = 0$ to 4.5	5 V						±100	μА
		V <sub>I</sub> = 0.8 V	A or B ports	75			75			μА
hold	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A of B ports	-75			-75			
lozh	V <sub>CC</sub> = 3.6 V <sub>i</sub>	V <sub>O</sub> = 3 V		<u> </u>		1			1	μΑ
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μΑ
			Outputs high			0.1			0.1	
Icc		$I_0 = 0,$	Outputs low			5			5	mA
100	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			0.1			0.1	
Δlcc¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND					0.2			0.2	mA
Ci	V <sub>I</sub> = 3 V or 0									pF
Cio	V <sub>O</sub> = 3 V or 0									pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_f \leq$  2.5 ns.  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

MAY 1992-REVISED NOVEMBER 1992

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Member of the Texas Instruments
   Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

SN54LVT16952 WD PACKAGE						
SN74LVT16952 DGG OR DL PACKAGE						
(TOP VIEW)						

		_	
10EAB[	1	56	10EBA
1CLKAB	2	55 ]	1CLKBA
1CEAB[	3	54	1CEBA
GND[	4	53	GND
1A1 [			1B1
1A2[]		51	1B2
v <sub>cc</sub> []	7	50	
1A3[]		49 🛚	1B3
1A4[]		48 🛚	1B4
1A5[]			1B5
GND			GND
1A6			1B6
1A7		44 []	1B7
1A8]			1B8
2A1 🛚			2B1
2A2[]			2B2
2A3[]			2B3
GND			GND
2A4[]			2B4
2A5[]			2B5
2A6			2B6
Vcc			Vcc
2A7		34	2B7
2A8			2B8
GND			GND
2CEAB[		31	2CEBA
	27		2CLKBA
2OEAB[	28	29]	20EBA

#### description

The 'LVT16952 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT16952 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

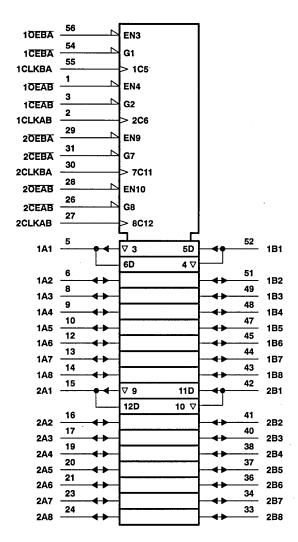
The SN54LVT16952 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16952 is characterized for operation from -40°C to 85°C.

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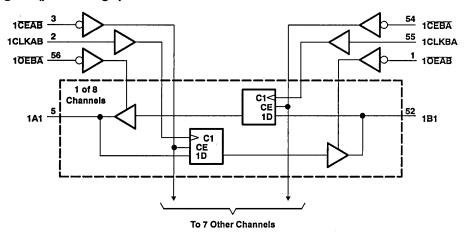
#### logic symbol<sup>†</sup>

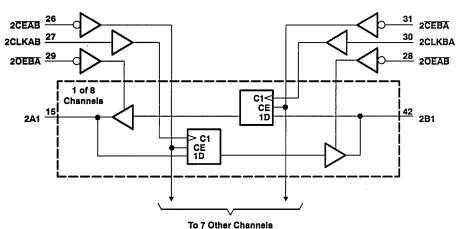


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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#### logic diagram (positive logic)





#### **FUNCTION TABLE<sup>†</sup>**

	OUTPUT			
CEAB	CLKAB	OEAB	Α	В
Н	Х	L	Х	B <sub>0</sub> ‡
×	L	L	Х	B <sub>o</sub> ‡ B <sub>o</sub> ‡
L	t	L	L	L
L	1	L	Н	н
х	X	н	Х	z

<sup>&</sup>lt;sup>†</sup> A-to-B data flow is shown; B-to-A data flow is similar but uses CEBA, CLKBA, and OEBA.



<sup>&</sup>lt;sup>‡</sup> Level of B before the indicated steady-state input conditions were established.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16952	96 mA
SN74LVT16952	128 mA
Current into any output in the high state, I <sub>O</sub> (see Note 2): SN54LVT16952	48 mA
SN74LVT16952	64 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package	0.7 W
DL package	1 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

#### recommended operating conditions

	•			SN54LVT16952		SN74LVT16952	
	•		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	٧
l <sub>он</sub>	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
l <sub>OL</sub> ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

<sup>&</sup>lt;sup>‡</sup> Current duty cycle ≤ 50%, f ≥ 1 kHz

<sup>2.</sup> This current will only flow when the output is in the high state and  $V_O > V_{CC}$ .

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16952			SN74LVT16952			UNIT		
PARAMETER				MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	UNII		
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V,	I <sub>I</sub> = -18 mA				-1.2			-1.2	٧		
	$V_{CC} = MIN \text{ to } MAX^{\ddagger}$ ,	l <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2					
V	V <sub>CC</sub> = 2.7 V,	I <sub>OH</sub> = -8 mA	- 8 mA				2.4			v		
V <sub>OH</sub>	V <sub>CC</sub> = 3 V,	I <sub>OH</sub> = - 24 mA	2									
	V <sub>CC</sub> = 3 V,	$I_{OH} = -32 \text{ mA}$					2					
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 100 μA				0.2			0.2	_		
	V <sub>CC</sub> = 2.7 V,	I <sub>OL</sub> = 24 mA				0.5			0.5			
VoL	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 16 mA				0.4			0.4	V		
<b>VOL</b>	V <sub>CC</sub> = 3 V,	l <sub>OL</sub> = 32 mA		İ		0.5			0.5			
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 48 mA				0.55						
	V <sub>CC</sub> = 3 V,	I <sub>OL</sub> = 64 mA							0.55			
	V <sub>CC</sub> = 3.6 V,	$V_I = V_{CC}$ or GND	Control pins			±1			±1	μΑ		
	$V_{CC} = 0$ or MAX <sup>‡</sup> ,	V <sub>I</sub> = 5.5 V				10			10			
11	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 5.5 V	A or B ports§			20			20			
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub>				1			1			
	V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = 0				-5			-5			
l <sub>OFF</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V							±100	μΑ		
, L	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 0.8 V	A or B ports	75			75			μА		
l <sub>hold</sub>	V <sub>CC</sub> = 3 V,	V <sub>I</sub> = 2 V	A or B ports	-75			-75					
lozh	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 3 V				1			1	μΑ		
lozL	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0.5 V				-1			-1	μA		
		I <sub>O</sub> = 0,	Outputs high			0.1			0.1			
lcc			Outputs low			5			5	mA		
	V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs disabled			0.1			0.1			
Δlcc¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND				0.2			0.2	mA			
Ci	V <sub>I</sub> = 3 V or 0								pF			
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0								pF			

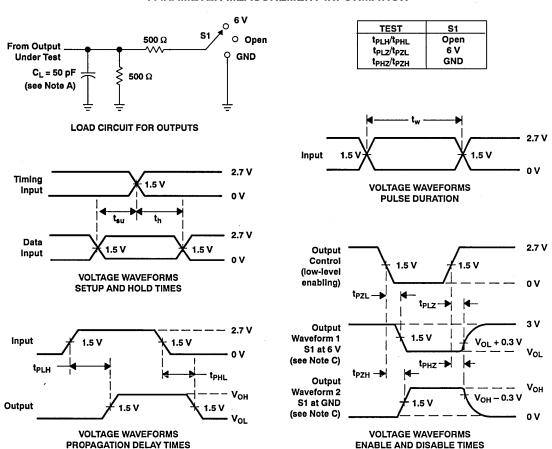
<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>\*</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> Unused pins at V<sub>CC</sub> or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $_{\leq}$  10 MHz,  $Z_0 = 50~\Omega$ ,  $t_f \leq 2.5~ns$ ,  $t_f \leq 2.5~ns$ .
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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# The Bypass Capacitor in High-Speed Environments

Advanced BiCMOS Technology

Ramzi Ammar General Purpose Logic – Semiconductor Group Texas Instruments Incorporated

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#### Introduction

High-speed switching environments generate noise on power lines (or planes) due to the charging and discharging of internal and external capacitors of an integrated circuit. The instantaneous current generated with the rising and falling edges of the outputs causes the power line (or plane) to ring. This behavior can violate the V<sub>CC</sub> recommended operating conditions or generate false signals, creating serious problems. A simple and easy solution must be considered to prevent such a problem from occurring. This solution is the bypass capacitor.

#### **Bypass Definition**

A bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low impedance supply, thereby minimizing the noise generated by the switching outputs of the device.

#### **Bypassing Considerations**

A system without bypassing techniques can create severe power disturbance and cause circuit failures. Figure 1 shows the  $V_{CC}$  line of the ABT541 ringing while all outputs are switching. Note that there is no bypass capacitor at the  $V_{CC}$  pin. There are a few issues that should be considered when bypassing power lines (or planes).

- The capacitor type
- The capacitor placement
- The output load effect
- The capacitor size

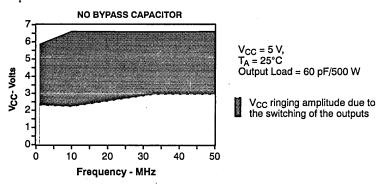


Figure 1. V<sub>CC</sub> Line Disturbance vs Frequency

#### **Capacitor Type**

In a high-speed environment the lead inductances of a bypass capacitor become very critical. High-speed switching of a part's outputs generates high frequency noise (> 100 MHz) on the power line (or plane). These harmonics cause the capacitor with high lead inductance to act as an open circuit, preventing it from supplying the power line (or plane) with the current needed to maintain a stable level, and resulting in functional failure of the circuit. Therefore, bypassing a power line (or plane) from the device internal noise requires capacitors with very small inductances. That is why the multilayer ceramic chip capacitors (MLC) are more favorable than others for bypassing power lines (or planes). They exhibit negligible internal inductance, thereby allowing the charge to flow easily, when needed, without degradation.

#### **Capacitor Placement**

Most of the printed circuit boards are designed to maintain a short distance between power and ground. This is done by laminating the power line (or plane) with the ground plane and can be electrically approximated with lumped capacitances as shown in Figure 2. However, this is not enough to have a reliable system, and another technique must be considered to provide a low-impedance path for the transient current to be grounded. This can be done by placing the bypass capacitor close to the power pin of the device.

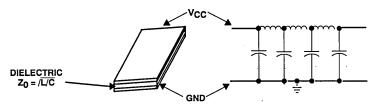


Figure 2. Typical Power Layout

#### Why This Location Is Very Important

Consider a device driving a line from low to high having an impedance ( $Z = 100 \Omega$ ) and a supply voltage ( $V_{CC} = 5 V$ ) (see Figure 3). In order for the device to change state, an output current (I = 50 mA) is needed instantaneously. Note that for eight outputs switching  $I = 50 \times 8 = 400 \text{ mA}$ . This current is provided by the power line (or plane) in a period  $\leq$  the rise time of the output (approximately 3 ns for ABT). The bypass capacitor must supply the charge in that same period of time to avoid  $V_{CC}$  drop, therefore distance becomes an important issue. Line inductances can block the charge from flowing, leaving the power line (or plane) disturbed.

Using the formula for paralleled wires:

$$L = 1 \frac{\mu_0}{\pi} \operatorname{Ln} \frac{d}{r} \tag{1}$$

where d is the distance between the wires, r is the radius of the wires, l is the length of the wires and  $\mu_0$  is the permeability of medium between wires, one can note that the inductance (L) is directly proportional to the distance between the lines as well as the length of the lines. Therefore, by reducing the loop ABCD in Figure 3, we can minimize the inductance and allow the capacitor to do its function more efficiently, and hence keep the noise off the power line (or plane).

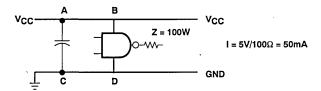
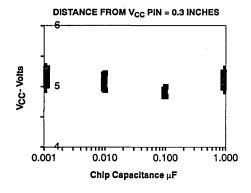
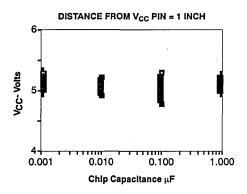
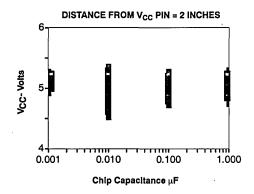


Figure 3. Capacitive Storage (Bypass Capacitor)

Several tests were done on an 'ABT541 device to study the behavior of its power line (or plane) as the outputs switch simultaneously. This data is taken at different distances from the power pin (0.3, 1, and 2 inches) using four chip capacitors  $(0.001, 0.01, 0.1, \text{ and } 1 \mu\text{F})$ , with an input frequency of 33 MHz and all eight outputs switching (worst case). Figure 4 shows the line disturbance increases as the capacitor is moved away from the power pin.







 $V_{CC}$  = 5 V,  $T_A$  = 25°C, Frequency = 33 MHz, Output Load = 500  $\Omega$ 

 $V_{CC}$  ringing amplitude due to the switching of the device outputs

Figure 4.  $V_{CC}$  Line Disturbance vs Cap Size at Different Distances

#### **Output Load Effect**

Capacitive loads combined with increased frequency result in higher transient current and possible  $V_{CC}$  oscillation. If the output load is purely resistive, the increase in frequency does not affect the rising and falling edge of the outputs, therefore not increasing the  $V_{CC}$  line disturbance. Figure 5 shows the power line behavior across frequency while driving a resistive load only, and Figure 6 shows the same plot with an additional 60-pF capacitive load.

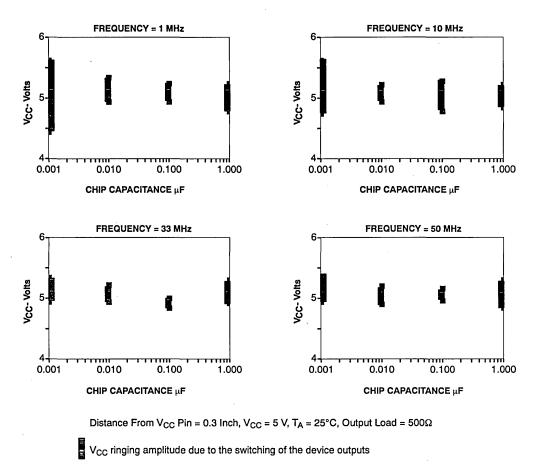


Figure 5.  $V_{CC}$  Line Disturbance vs Cap Size With Resistive Load at Different Frequencies

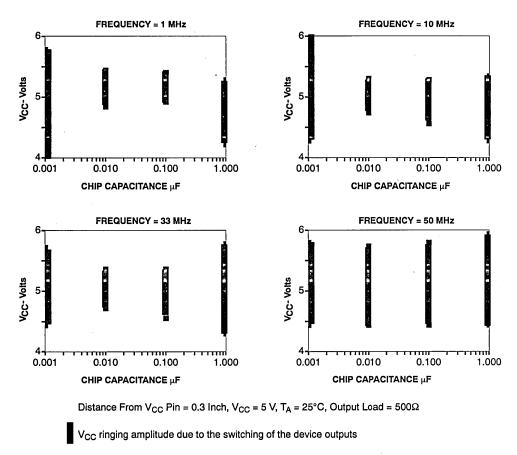


Figure 6. V<sub>CC</sub> Line Disturbance vs Cap Size With 60-pF Load at Different Frequencies

When driving large capacitive loads, more charge will need to be supplied to the output load, resulting in a slower rising or falling edge. However, if the bypass capacitor is not capable of providing the needed charge, power lines (or planes) start to ring and eventually oscillate causing failures across the board. These oscillations can be of a great amplitude, 2 to 3 V p-to-p. Figure 7 shows these oscillations at four different loads (0, 60, 115 and 200 pF) using four different bypass capacitors (0.001, 0.01, 0.1, and 1  $\mu$ F).

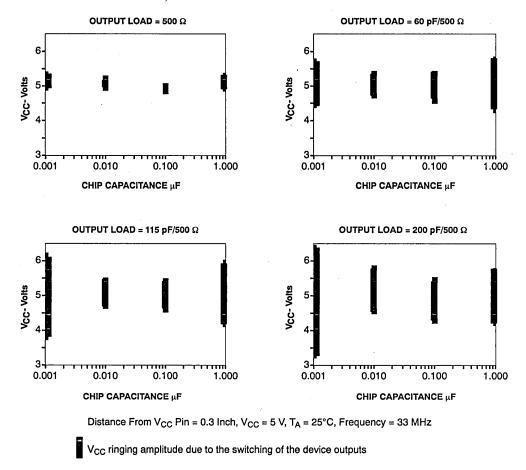


Figure 7.  $V_{CC}$  Line Disturbance vs Cap Size at Different Capacitive Loads

#### **Capacitor Size**

How can we choose the right bypass capacitor? The most important parameter is the capability of supplying instantaneous current when it is needed.

There are two ways for calculating the bypass capacitor size for a device:

 One must know the amount of current needed to switch one output from low to high (I), the number of outputs switching (N), the time required for the capacitor to charge the line (ΔT), and the drop in V<sub>CC</sub> that can be tolerated (ΔV).

The following equation can be used:

$$C = \frac{I \times N \times \Delta T}{\Delta V} \tag{2}$$

where  $\Delta T$  and  $\Delta V$  can be assumed.

For example, say one has the following parameters:  $\Delta V = 0.1 \text{ V}$ ,  $\Delta T = 3 \text{ ns}$ , N = 8, and I can be obtained from either Figure 3, for rough estimate or from the plot in Figure 8, assuming 50-MHz frequency. We are going to use the latter parameter for our example, I = 44 mA.

Then the equation is as follows:

$$C = \frac{44 \times 10^{-3} \times 8 \times 3 \times 10^{-9}}{0.1} = 10080 \times 10^{-12} = 0.01 \,\mu\text{F}$$
 (3)

Several of the capacitor manufacturers specify the maximum pulse slew rate. This allows the capacitor's maximum current to be calculated. For example, a 0.1-μF capacitor rated at 50 V/μs can supply: i = cdv/dt = 0.1 × 50 = 5 A. This current is greater than the maximum current (I × N = 44 mA × 8 outputs switching = 352 mA) required by the device used in the previous example.

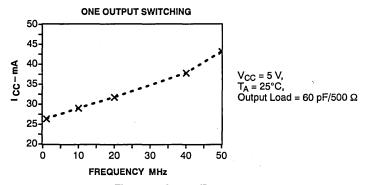


Figure 8. I<sub>CC</sub> vs Frequency

#### Conclusion

From what was mentioned previously, one can see how important is the bypassing technique. Bypass capacitors play a major role in achieving reliable systems. The absence of the bypass capacitor can generate false signals and create major problems across the entire board. Figure 1 shows the undesired ringing caused by simultaneously switching the outputs of the 'ABT541. Also, choosing a capacitor with negligible lead inductance can avoid unpredictable behavior at high frequencies. Locating the capacitor closer to the  $V_{CC}$  pin of a device can avoid further complications and eliminate the ringing entirely. Figure 6 shows the  $V_{CC}$  line behavior with the bypass capacitor placed 0.3 inches away from the  $V_{CC}$  pin, whereas Figure 9 shows the same plot with the same load, but the bypass capacitor is located at the pin, one can see the dramatic improvement achieved in the latter case. This technique can also be applied to Texas Instruments  $Widebus^{TM}$  family by bypassing all  $V_{CC}$  pins. This was proven to be the most effective method for eliminating the  $V_{CC}$  line ringing. It is always important to minimize the loop between the  $V_{CC}$  pin, the ground, and the bypass capacitor. Finally, choosing the capacitor size by using either method mentioned earlier is highly recommended. If one considers all these issues, a good bypass technique can be achieved.

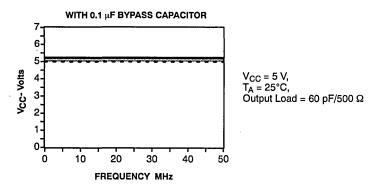


Figure 9. V<sub>CC</sub> Line Disturbance vs Frequency

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- [1] Texas Instruments, Advanced Schottky Family (ALS/AS) Applications
- [2] Walton, D., P.C.B. Layout for High-Speed Schottky TTL

# Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices

Advanced BiCMOS Technology

Jim Tuckwell General Purpose Logic – Semiconductor Group Texas Instruments Incorporated

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#### Introduction

The data in this application note demonstrates the skew between the outputs of a sample of Texas Instruments Advanced BiCMOS (ABT) devices. This paper will explain which output skew is being examined, where the data for these curves comes from, and how the data is analyzed. Also, some of the errors that may be present in the data will be discussed.

#### Skews

Skew is a term that is used to define the difference, in time, between two different signal edges. There are several different types of skew currently being used, they are defined in JEDEC 99 clause 2.3.5:

<u>Output Skew</u>  $(t_{sk(o)})$  – The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminating at different outputs.

 $\underline{Input \, Skew} (t_{sk(i)})$  – The difference between two propagation delay times that originate at different inputs and terminate at a single output.

<u>Pulse Skew</u>  $(t_{sk(p)})$  – The difference between the propagation delay times  $t_{PLH}$  and  $t_{PHL}$  when a single switching input causes one or more outputs to switch.

 $\underline{Process\ Skew}$  ( $t_{sk(pr)}$ ) – The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions.

<u>Limit Skew</u>  $(t_{sk(l)})$  – The difference between: 1. The greater of the maximum specified values of  $t_{PLH}$  and  $t_{PHL}$  and 2. The lesser of the minimum specified values of  $t_{PLH}$  and  $t_{PHL}$ .

The skew discussed here is the skew of propagation delays across the outputs of a device. More specifically, it is the difference between the largest value obtained for a propagation delay and the smallest value across all of the outputs. For example, if output 3 has the largest propagation delay  $t_{PLH}$  and output 14 has the smallest, then the output skew for this device would be the difference between the propagation delays for output 3 and output 14 (see Figure 1).

The majority of the curves presented in this paper consist of data taken on devices that have one output switching at a time. This produces a skew that should not be confused with the defined data sheet skew  $t_{sk(o)}$ . The data sheet value for  $t_{sk(o)}$  is found by switching all of the outputs simultaneously. Two of the devices examined in this paper ('ABT16240, 'ABT16500A) include curves which present  $t_{sk(o)}$  data.

#### Source of Data

The data used to produce the curves presented in this paper was extracted from the characterization data bases used to set the data sheets for the devices presented. The sample size of the data base is approximately thirty devices for each characterization lot (wafer) used.

The data was sorted so that the maximum skew for each device at a particular  $V_{CC}$  and temperature combination could be determined. Next, the maximum skew values were averaged to produce a data point for each transition. Further statistical analysis of this data was performed to calculate a standard deviation of the maximum skew across the devices. This value was then used to produce a three standard deviations data point for each  $V_{CC}$  and temperature combination. The data is presented as a family of curves across  $V_{CC}$  with each member of the family being an output skew versus temperature curve. The curves for each device are broken out by output transition (i.e.  $t_{PLH}$ ,  $t_{PHL}$ ). Each transition is further separated into a set of curves depicting the average skew across the devices and a set representing the average skew plus three standard deviations.

For those devices ('ABT16952 and 'ABT16500A) which have registers, the data path chosen for each device was the path which put the device in a transparent mode. Also, for the bidirectional devices ('ABT16245, 'ABT16952, and 'ABT16500A) the A-to-B direction was used.

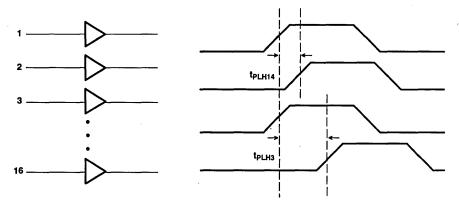


Figure 1. Skew = |tpLH14 - tpLH3|

#### Sources of Error in Data

The data in this paper was taken on an IMPACT tester, which is a piece of automatic test equipment used to characterize integrated circuits. The tester is offset using a golden unit which has had data taken on a lab bench setup. It is this process of offsetting which is the main source of error in the data.

Briefly the tester is offset in the following manner: First the golden unit has its propagation delay measurements taken at 25°C and 85°C using a pulse generator as the source and an oscilloscope as the measurement unit. The golden unit is then placed on the IMPACT and the data is again taken. The difference between the two values is the offset. The 25°C offsets are used for the data taken at -55°C, -40°C and 25°C while the 85°C offsets are used at 85°C and 125°C.

Great care is taken during this process to ensure that the induced error is kept to a minimum. For example, the boards are checked before use to ensure the output loads are correct, the oscilloscope is calibrated each day and the input signals are closely monitored to ensure that the intended signal is delivered to the golden unit.

This reduction in error is quite important in this application due to the fact that the average skews for the devices are about 200 ps. A 20-ps error in offsets translates into an approximate error of 10% in the output skew data.

However, it can be seen in the curves presented here that the error has been kept to a minimum and that the curves are fairly well behaved.

#### Conclusion

The family of curves presented in this paper demonstrates that the Texas Instruments Advanced BiCMOS family of devices can be expected to produce an average skew between outputs that will remain below 400 ps for devices with single switching outputs. Also, when a device has its outputs switching simultaneously, the average skew across the outputs can be expected to remain below 700 ps.

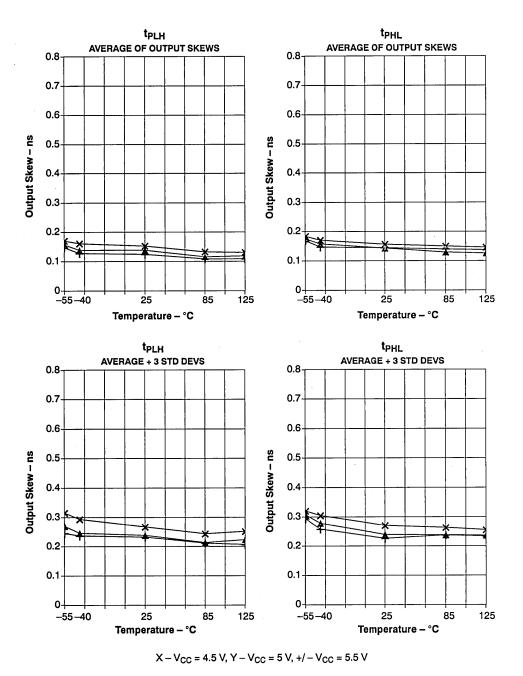


Figure 2. 'ABT16240 - Single Switching

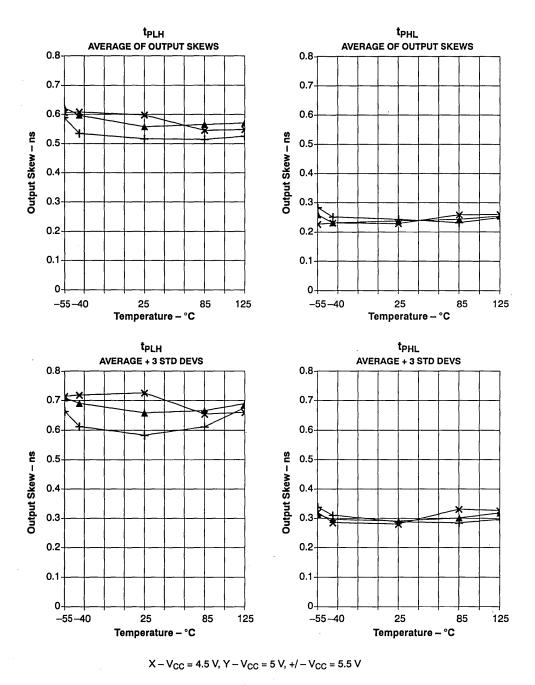
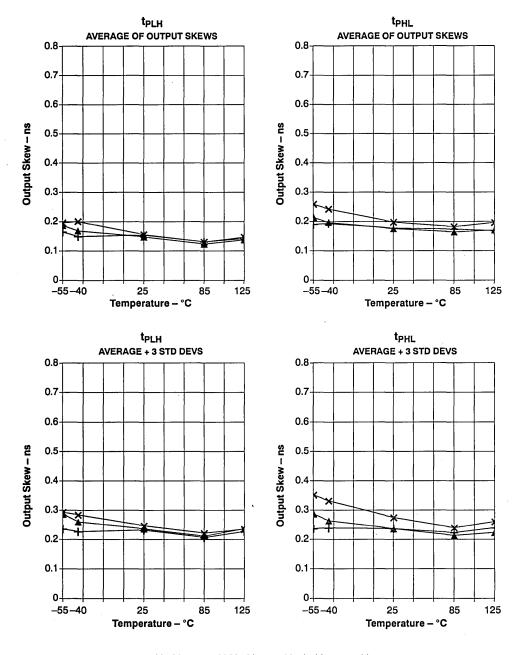


Figure 3. 'ABT16240 - Simultaneous Switching



 $X - V_{CC} = 4.5 \text{ V}, Y - V_{CC} = 5 \text{ V}, +/-V_{CC} = 5.5 \text{ V}$ 

Figure 4. 'ABT16245 - Single Switching

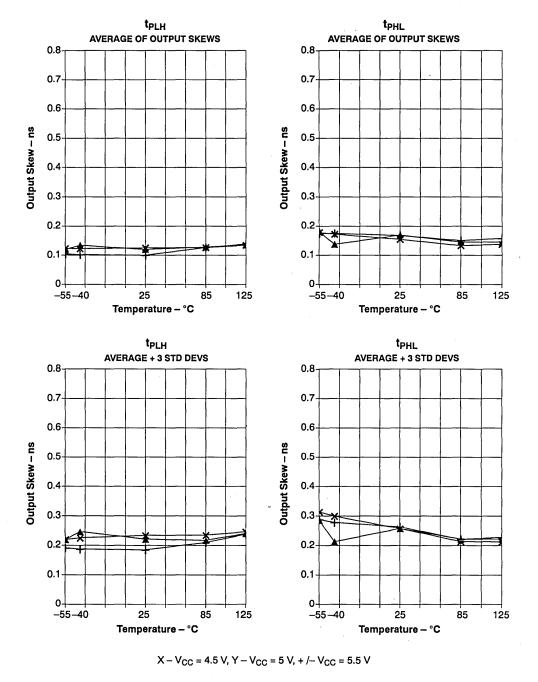


Figure 5. 'ABT16952 - Single Switching

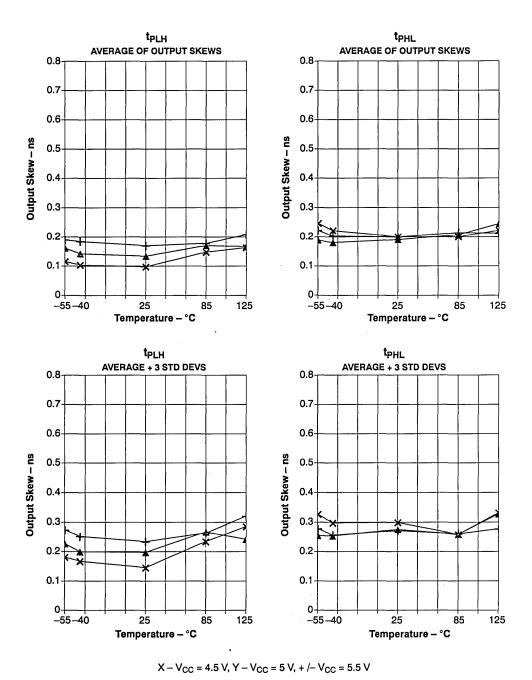


Figure 6. 'ABT16500A - Single Switching

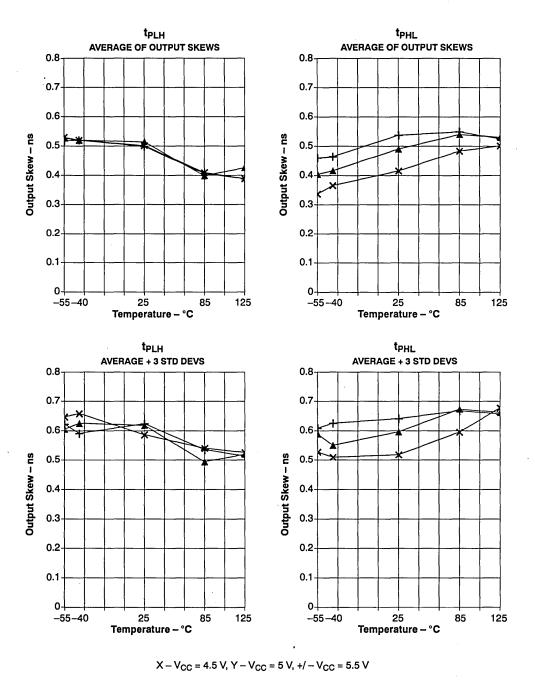


Figure 7. 'ABT16500A - Simultaneous Switching

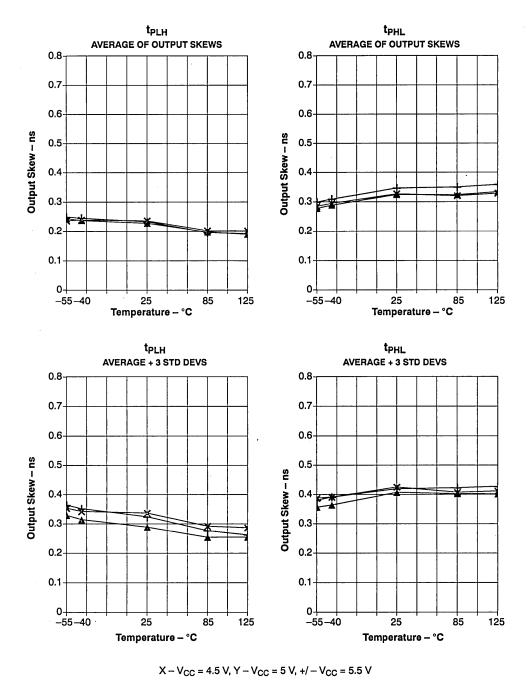


Figure 8. 'ABT244 - Single Switching

## Mixing It Up With 3.3 Volts

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## Mixing It Up With 3.3 Volts

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#### Introduction

The evolution to 3.3-volt supply is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes, or geometries, are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M versions will be developed for operation from a supply voltage of 3.3 +/- 0.3 volts. For 16M DRAM product there is no such rule-of-thumb as certain vendors expect to operate from 3.3 volts, while others will offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-volt power operation externally with internal step-down conversion to 3.3 volts. For static memories random access (SRAMs). manufacturers have announced that most versions of the 16M will operate at 3.3 volts or lower (with some down to 2.7 volts).

Typical 1M DRAM geometries are on the order of 1.2 microns, and it is not a problem to apply a 5-volt power supply to these type of products. However, as the feature sizes of DRAMs shrink, the stresses of 5-volt operation can preclude their

reliable operation due to high field effect failures. One such effect is hot carrier injection which over time increases the transistor's threshold, leading to eventual non-operation. Another field effect concern is the breakdown of the transistor's gate oxide, causing internal shorts. Therefore, reducing the supply voltage is one way to insure reliable operation of devices fabricated in state-of-the-art processes.

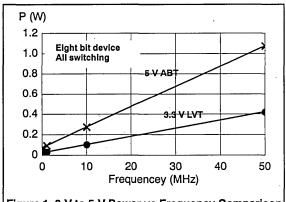


Figure 1. 3-V to 5-V Power vs Frequency Comparison

The reduction of Vcc from 5 volts to 3.3 volts also reduces the power consumed by the device, increasing system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this

square relationship a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3 volt operation.

#### The Market for Low Voltage

User demand for low voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments mutli-user such servers, engineering workstations, high-end desktop PCs, and other high performance motherboards favor high performance over low power but are interested in 3.3-volt products to reduce or eliminate bulky. noisy cooling fans in the never ending attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery powered notebook and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as laptop computers, automotive and air/space products.

The universal benefits to users of low voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-volt solutions and results from lower stress gradients on device junctions and oxides, lower build-up of heat due to lower power consumption and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users an added benefit of the lower power consumption of low voltage products is one of increased battery lifetime.

Of all the end equipment groups which can benefit from the use of low voltage products, it appears that demand will be initially driven by battery operated computers. This market segment is defined by notebook and palmtop computers, as well as, point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on board transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-volt supply when charged, decreasing to about 2.7 volts after use. Three NiCad batteries provide for a baseline 3.6 volt supply fully charged but the spread actually runs from about 3.3 volts up to 3.9 volts. For now the unregulated battery market demands low voltage products which are optimized to run from 2.7 volts up as high as 3.9 volts. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 volts since this is where devices will slow down appreciably.

There are some barriers for low voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3 volt devices can be a problem. Generally DRAM memories are leading the way into 3.3-volt operation with SRAM memories close behind. Coupled with the low voltage microprocessors now available systems are being implemented with the core components operating at 3.3 volts, with volume requirements not beginning until the '94—'95 time frame. Hindering the migration to a full 3.3-volt system is the availability of support products such as: disk drives, LCDs, A/D, RF transmitters and EPROMS.

#### Migration to 3.3 Volts

The need to migrate to power supplies less than 3.3 volts has been an issue since 1984 when, through various JEDEC committees, two standards were adopted. Standard 8.0 was intended to address both regulated (3.0 V to

3.6 V) and unregulated (2.0 V to 3.6 V) battery applications. Standard 8.1 was intended to address higher performance applications operating from a regulated power supply which could interface to a standard 5-volt TTL device as well as a low voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low voltage battery operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the more critical one being reviewed now. When ratified the new LVTTL standard will present methods for interfacing with 5-volt systems, as well as, contain a provision for battery operated systems. Until this point however, a generic lack of compatibility will exist between the various 3.3-volt and 5-volt interfaces.

Existing solutions for 3.3-volt operation have historically been 5-volt products and processes characterized for 3.3 volt operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-volt and 3.3-volt operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-volt operation. A limitation of many of these devices is their inability to directly interface to a 5-volt system when running off a 3.3-volt supply, due to diodes from the input and input/output (I/O) pins to Vcc. This limits input voltages to Vcc+0.5 volts and limits direct connection to a 5-volt system.

#### **Mixed Mode Operation**

This dilemma of device compatibility between the large installed base of 5-volt systems with the newly emerging 3.3-volt systems is a pressing industry concern. Mixed mode operation allows for direct communication between the two systems. Devices which support this mode must

be designed for maximum input voltages of 5.5-volt without any long term reliability issues. Another concern is that the output drive must be capable of driving a standard TTL backplane, while still providing for rail-to-rail switching for compatibility with 3 volt CMOS system.

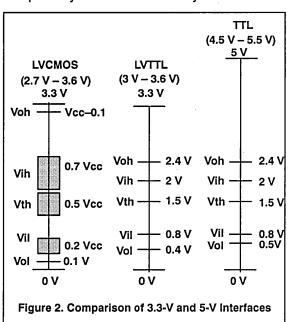


Figure 2 compares the standard TTL DC interface levels with two of the emerging low voltage standards. Low voltage CMOS (LVCMOS) is a pure CMOS specification which specifies low current rail-to-rail output drive, along with input voltage level, Vih and Vil, which are ratios of Vcc. Low-voltage TTL (LVTTL) utilizes the standard TTL input levels of 0.8 and 2.0 volts, as well as specifying a higher DC output drive than (LVCMOS). To insure interoperability between these three varied standards, a multi-purposed low-voltage interface device must meet all of the requirements of the three different specifications.

## **LVT Family Characteristics**

To address the need for a complete low voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed mode operation. The LVT series of parts

rely on a state of the art sub-micron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-volt maximum input voltage.

Specified 2.7- to 3.6-volt supply voltage.

I/O structures which support live insertion.

Standard TTL output drives of:

 $V_{OH} = 2 V \text{ at } I_{OH} = -32 \text{ mA}$ 

 $V_{OI} = 0.55 \text{ V at } I_{OI} = 64 \text{ mA}$ 

Rail-to-rail switching for driving CMOS

Maximum supply currents of:

 $I_{CC(L)} = 15 \text{ mA}$ 

 $I_{CC(H)} = 250 \,\mu A$ 

 $I_{CC(Z)} = 250 \mu A$ 

Propagation delays of:

 $t_{pd} < 4.6 \text{ ns}$ 

 $t_{pd}$  (LE to Q) < 5.1 ns

 $t_{pd}$  (CLK to Q) < 6.3 ns

Surface mount packaging support including flne-pitch packages:

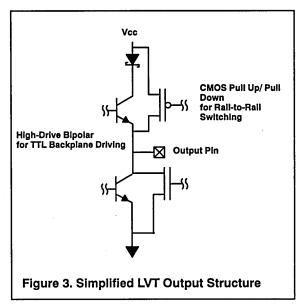
48- and 56-pin SSOP for LVT

Widebus™

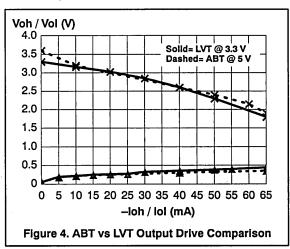
20- and 24-pin TSOP for standard LVT

#### LVT Input/Output Characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-volt ABT devices, Figure 4, providing the DC drive needed for existing 5-volt backplanes, thus, allowing for a simple solution to reduce system power, via the migration to 3.3-volt operation.



Not only can LVT devices operate as 3 V to 5 V level translators by supporting input or I/O voltages of 5.5 volts with Vcc= 2.7 to 3.6 volts, the inputs can withstand 5.5 volts even when Vcc= 0 volts. This allows for the devices to be used under partial system power down applications or those which require live insertion.



#### **Bus Hold**

Many times devices are used in applications that do not provide a pull-up or down voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or non-bused lines. To prevent application problems or oscillations a large pull-up resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, +/ $-100 \mu A$ , that is sufficient enough to overcome any 'CMOS'-type leakages. Since this is an active circuit is does take current, approximately +/ $-500 \mu A$ , to toggle the state of the

input. This current is trivial when compared to the tens of mA of current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

#### Conclusion

LVT devices solve the system need for a transparent seam between the low voltage and 5-volt sections, by providing for mixed signal operation. The devices support live insertion or partial power applications, while providing for low input leakage currents. The outputs are capable of driving today's 5-volt backplanes, with a considerable reduction in the device's power consumption, as well as, being packaged in state of the art fine pitch surface mount packages.

Widebus is a trademark of Texas Instruments Incorporated.

## **Package Thermal Considerations**

Darla Wellheuser General Purpose Logic – Semiconductor Group Texas Instruments Incorporated

### **Package Thermal Considerations**

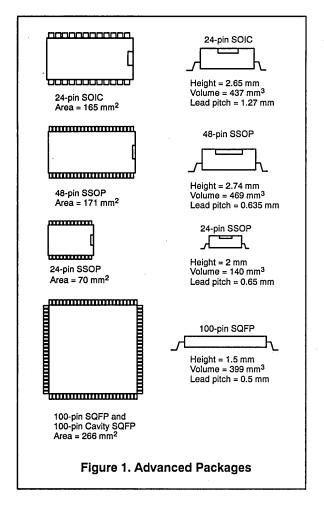
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#### **Abstract**

In order to meet current and future system requirements of increasing speed and decreasing size, integrated circuit manufacturers are pushing the edge on existing packaging technology. No longer is a component's performance determined by process technology alone but also by the thermal limitations of its package. As a leader in package technology, Texas Instruments has introduced a number of fine pitch packages and is acutely aware of the thermal considerations which must be examined by systems designers. This paper is intended to create awareness and understanding of thermal issues and to explore factors which influence thermal performance.

#### Introduction

Thermal awareness became an industry concern when surface mount (SMT) packages began replacing through hole (DIP) packages in PCB designs. Circuits operating at the same power enclosed in a smaller package meant higher power. To add to the issue, systems were requiring increased through-put which resulted in higher frequencies, increasing the power density even further. Not only are these same concerns still haunting designers today, they are progressively getting more severe.



A glance at Figure 1 will explain part of the reason for increased attention to thermal issues. As a baseline for comparison the 24-pin SOIC is pictured along with several fine-pitch packages supplied by TI, including the 24-pin SSOP (shrink small-outline), 48-pin SSOP and the 100-pin SQFP (shrink quad flat pack). The 24-pin SSOP (8, 9, 10 bits) allows for the same circuit functionality of the 24-pin SOIC to be packaged in less than half the area, while the 48-pin SSOP (16, 18, 20 bits) occupies just slightly more area but has twice the functionality of the 24-pin SOIC. This same phenomena is expanded even further with the 100-pin SQFP (32 and 36 bits) which is the functional equivalent of four 24-pin or two 48-pin devices with additional board savings over that of the SSOP packages. As the trend in packaging technology continues to give way to smaller packages, attention must be focused on the thermal issues this creates.

## Reliability

The overriding effect of increased power densities in integrated curcuits is a decrease in overall system reliability. A direct relationship exists between junction temperature and reliability which can be shown using the Arrhenius equation.

$$AF = Exp [Ea/k(1/T1 - 1/T2)]$$
 (1)

Where:

AF = acceleration factor Ea = activation energy (eV)

k = Boltzmann's constant  $(8.617 \times 10^{-5} \text{ eV/K})$ 

T1 = use junction temperature (K)
T2 = stress junction temperature (K)

The acceleration factor can be used to determine the failure rate of a given component.

FR (failure rate) = 
$$1/AF$$
 (2)

Table 1 provides an example of a device with an initial junction temperature of 100°C and the calculated failure rate decrease as the in use junction temperature is lowered. The data given in

Table 1 indicates that lower junction temperature will result in increased system reliability.

Table 1

Temp C	AF	FR	% FR Decrease
100	1.00	1.00	0
90	1.54	0.65	35
80	2.41	0.41	59
70	3.90	0.26	74
60	6.48	0.15	85

Ea = 0.5eV % FR Decrease = 1 – FR

A better understanding of the factors which contribute to junction temperature (Tj) will provide a system designer with more flexibility when attempting to solve thermal issues. Device junction temperature is determined by the following:

$$Tj = Ta + [\Theta_{JA} \times P_T]$$
(3)

Where:

Tj = junction (die) temperature (°C)

Ta = ambient temperature (°C)

Θ<sub>JA</sub> = thermal resistance of the package from the junction to the ambient (°C/W)

 $P_T$  = total power of the device (W)

Among the things that can alter junction temperature are lower chip power consumption, longer trace length, heat sinks, forced airflow, package mold compound, lead frame size and material, surface area, and die size. Some of these are mechanically inherent to a particular package while others are controlled by the designer and are application specific. To understand which variables can be influenced by practicing good thermal design techniques requires a more detailed investigation of power considerations as well as thermal resistance measurements.

## Power Consumption

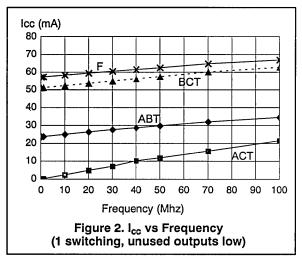
One way to lower the junction temperature (Tj) of a device, thus improving reliability, is to lower the power consumption. A variety of options are available to help achieve this, such as, low power process technologies, reduced output swing, and reduced power supply voltage. A close look at the power performance and advantages of several popular logic families will assist the designer when choosing what best fits his/her needs.

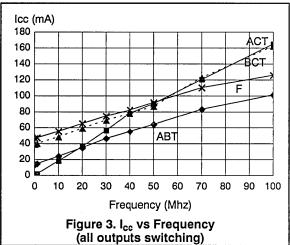
The choices available from Texas Instruments for high speed bus-interface ranges from standard bipolar (F) to advanced CMOS (ACL/ACT) to state-of-the-art BiCMOS (BCT) and advanced BiCMOS (ABT). Figures 2-4 show current consumption comparisons of 244 functions for these technologies across frequency. As expected, the bipolar device consumes more current than the CMOS device at lower frequency, but as frequency increases this relationship no longer holds true. In fact, there exists a region in the frequency range where the CMOS device will consume more current than the bipolar device. The point at which they are equal is referred to as the cross-over frequency. Notice the low frequency where the cross-over point for ABT and ACT occurs.

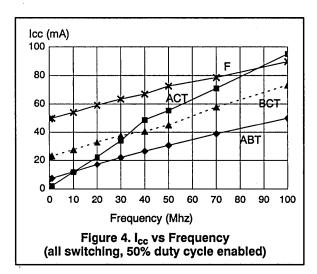
Typical applications for bus-interface devices require them to be disabled or in the *stand-by* mode during certain periods of time, for instance, while other devices access the bus. This can result in a large decrease in current consumption for ABT, BCT, and ACT devices which have low stand-by current. These values are given in the datasheets as  $I_{CC}$  for ACT and  $I_{ccz}$  for ABT (250  $\mu$ A) and BCT ( $\cong$  10 mA). Current consumption data versus percent duty cycle enabled is shown in Figure 5.

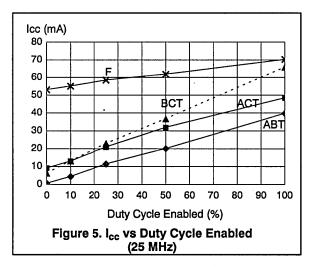
The frequency of the data is held constant at 25 MHz and all outputs are switching.

The power consumption data provided is limited to a small range of variations, however, using this data along with standard formulas power consumption can be calculated for specific applications.









#### **Power Calculations**

When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account.

Both bipolar and BiCMOS devices have varying static current levels depending on the state of the output (I<sub>CCL</sub>, I<sub>CCH</sub>, I<sub>CCZ</sub>), while a CMOS device has a single value for I<sub>CC</sub>. (These values can be found in the individual datasheets.) ACT and ABT inputs when driven at TTL levels will also consume

additional current because they may not be driven all the way to Vcc or GND, therefore the input transistors are not completely turned off. This value is known as  $\Delta l_{CC}$  and is also provided in the datasheet.

Dynamic power consumption results from the charging and discharging of both internal parasitic capacitances as well as external load capacitance. The parameter for ACT and AC and devices which accounts for the parasitic capacitances is known as  $C_{pd}$  and is obtained using the following formula, and is found in the datasheet.

$$C_{pd} = [I_{CC} (dynamic)/(V_{CC} - Fi)] - C_L$$
(4)

Where:

Fi = input frequency (Hz)
V<sub>CC</sub> = supply voltage (V)
C<sub>I</sub> = load capacitance (F)

I<sub>CC</sub> = measured value of current into the device

Although a  $C_{pd}$  value is not provided for ABT, BCT, or F devices,  $I_{CC}$  versus frequency curves display essentially the same information. The slope of the curve provides a value in the form of mA/(Mhzxbit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device (without the load current).

The following equations can be used to calculate total power for CMOS, Bipolar, and BiCMOS devices.

$$P_{T} = P_{S(tatic)} + P_{D(ynamic)}$$
 (5)

**CMOS** 

AC (CMOS-level inputs)

$$P_{S} = V_{CC} \times I_{CC}$$

$$P_{D} = [(C_{pd} + C_{L}) \times V_{CC}^{2} \times f_{1}] N_{sw}$$
(6)

**ACT** (TTL-level inputs)

$$P_{S} = V_{CC} [I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)]$$

$$P_{D} = [(C_{pd} + C_L) \times V_{CC}^2 \times f_1] N_{sw}$$
(7)

#### **BiCMOS/Bipolar**

 $P_S = V_{CC} \left[ DC_{en} (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) \right]$ (8) +  $(1-DC_{en})Iccz$ ] +  $(N_{TTL} \times \Delta Icc \times DC_d)$ 

Note:  $\Delta I_{CC} = 0$  for bipolar devices

 $P_D = [DC_{en} \times N_{sw} \times V_{CC} \times f_1 \times (V_{OH} - V_{OL}) \times C_L]_{(9)}$ +  $[DC_{en} \times N_{sw} \times V_{cc} f_2 \times (mA/MHz \times bit)] \times 10^{-1}$ 

#### Where:

Vcc = supply voltage (V)

lcc = power supply current (A) (from the datasheet)

power supply current when outputs are in ICCL = the low state (A) (from the datasheet)

power supply current when outputs are in Icch = the high state (A) (from the datasheet)

power supply current when outputs are in lccz = the high-impedance state (A) (from the

datasheet)

power supply current when inputs are at a  $\Delta I_{CC} =$ 

TTL level (A) (from the datasheet)

DC<sub>en</sub> = % duty cycle enabled (50% = 0.5) $DC_d =$ % duty cycle of the data (50% = 0.5) $N_H =$ number of outputs in the high state number of outputs in the low state  $N_L$ total number of outputs switching  $N_{sw} =$ 

Nτ total number of outputs operating frequency (Hz) f<sub>1</sub> operating frequency (MHz) f<sub>2</sub>

output voltage in the high state (V) V<sub>OH</sub> =  $V_{OL} =$ output voltage in the low state (V)

external load capacitance (F)

mA/(Mhzxbit) = slope of the I<sub>CC</sub> vs frequency curve

### Thermal Resistance Values

Design trends requiring board size reduction have made way for circuit manufacturers to produce fine-pitch packages which appear to threaten the reliability of systems due to further thermal constraints. As a leader in packaging technology, Instruments has done considerable research into the validity of traditional thermal measurements and data provided by circuit manufacturers.

Unlike datasheet parameters, where the industry has adopted a standard load for measurement (50 pf, 500  $\Omega$ ), the measurement of  $\Theta_{JA}$  has no standard to which all manufacturers comply. The

problem facing the designer wishing to make comparisons of thermal data from several manufacturers is that this could be an apples to oranges type comparison. As a result, a software package has been developed at TI to allow designers to obtain thermal data based on their specific application.

The validity and usefulness of the traditional approach to presenting  $\Theta_{JA}$  values became a pressing issue when TI and another manufacturer measured an identical package and obtained results which varied by 40%. Extensive research led to the conclusion that the methodology used to measure  $\Theta_{JA}$  did not cause the discrepancy but the physical aspects such as trace length, trace width, number of devices per board, and proximity of the other devices did.

To demonstrate the extreme impact of trace length alone, Figure 6 shows graphs of the  $\Theta_{JA}$  values for Texas Instruments 48-pin shrink small-outline package (SSOP) at 0 lfm and 250 lfm with varying trace lengths. (The 48-pin SSOP is pictured in Figure 1 for a side by side comparison with the standard 24-pin SOIC, the 24-pin SSOP and the 100-pin SQFP). The data in Figure 6 clearly shows the need for more complete thermal data, not simply a single data point.

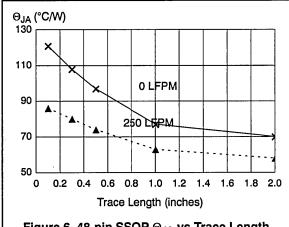
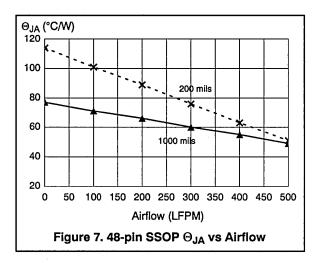


Figure 6. 48-pin SSOP ⊖<sub>JA</sub> vs Trace Length

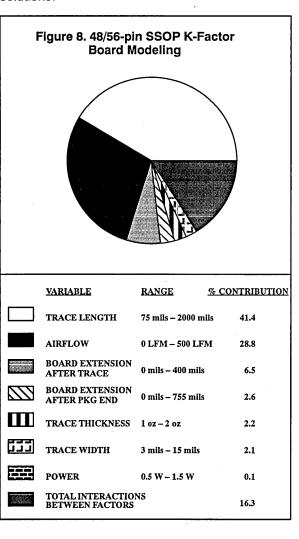
There are, of course, other methods to lower the  $\Theta_{JA}$  of a device. Using heat sinks or blowing air across a device will certainly improve the ability to remove heat from its surface. Figure 7 provides  $\Theta_{JA}$  data for the 48-pin SSOP with trace lengths of 200 mils and 1 inch while varying the amount of airflow. Although many applications tend to limit the amount of airflow allowed, it provides excellent benefits when possible.



A comparison was made of several variables which have a direct effect on  $\Theta_{JA}$  values. This data is shown in Figure 8. Surprisingly, the major contributing factor is trace length not airflow. Once again, this validates the need for improvement not necessarily in the test methodology used to calculate  $\Theta_{JA}$  values, but certainly in the way they are provided.

Texas Instruments has taken the step of providing  $\Theta_{JA}$  values for a variety of packages (including the SOIC, SSOP and QSOP) in a user-friendly

software package. The program allows the designer to specify his/her own conditions such as trace length, airflow, proximity of other devices, and trace width in order to obtain realistic thermal solutions.



#### Conclusion

How can a system avoid being a reliability nightmare in today's world where:

- Eight-bit devices are being replaced by 16 and 32 bits in a single package, increasing the power.
- Higher operating frequencies add to the increase in power.
- Fine-pitch packages are reducing the amount of available surface area to remove heat from a device.

Semiconductor manufacturers must take the first step and provide realistic and useful thermal information which will provide designers key variables to focus on for thermal management.

## **For Further Information**

#### **Thermal Software**

Contact the factory - (903) 868-7682

#### **Power Dissipation**

Advanced CMOS Logic Designer's Handbook, Texas Instruments, 1988.

SSOP Designer's Handbook, Texas Instruments, 1991.

# Recent Advancements in Bus-Interface Packaging and Processing

Ken Ristow
General Purpose Logic – Semiconductor Group
Texas Instruments Incorporated

## Recent Advancements in Bus-Interface Packaging and Processing

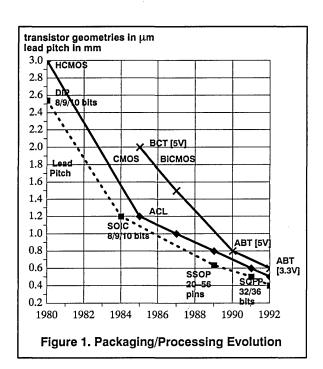
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#### Introduction

Over the past several years the advancements in semiconductor processing have been combined with advanced surface mount packages to offer solutions to board area concerns, as well as, providing for increased system performance. Figure 1 compares the reduction of the package's lead pitch to that of both CMOS and BiCMOS transistor geometries. This paper will explore the different types of fine pitch logic packages and the bus interface solutions provided when they are combined with sub-micron semiconductor processes.

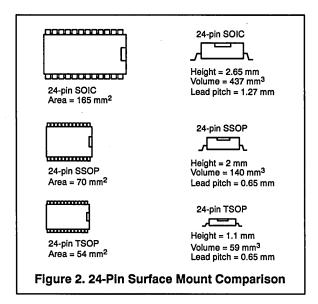
## **Evolutions in Device Packaging**

With the need for increased functionality in less board area has come the consolidation of much of the board's logic into higher complexity devices. In many cases the discrete logic parts that remain, primarily interface/bus drivers, must occupy the board area leftover after the higher level chips, i.e., microprocessor, ASICs, memory, etc., have been laid out. To meet this task the standard small-outline Integrated circuit (SOIC) has evolved in two distinct paths. One path reduces the package's area and volume (see Figure 2), and the other increases the bit density of the device (see Figure 3).



One method to increase bit density is to keep the number of pins constant while reducing both the lead pitch and package area. The 20/24 pin SSOPs utilize a 0.65-mm lead pitch to achieve over a 50% reduction in area, compared to their standard SOIC counterparts. The package height is also reduced from 2.65 mm for the SOIC to 2 mm for the 20/24-pin SSOPs. This reduction in volume

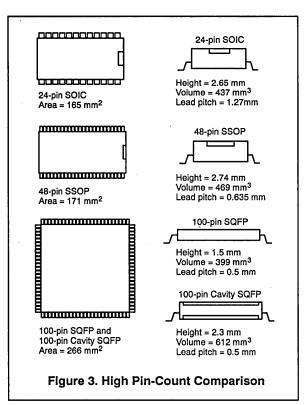
translates into tighter board to board spacing, allowing for denser memory arrays.



The advent of the Personal Computer Memory Card International Association (PCMCIA) standard has required that the package height be reduced even further, thus spawning the thin small-outline package (TSOP). This package utilizes 0.65-mm lead pitch and has a maximum device height of 1.1 mm. With an area of 59 mm², this package utilizes 86% less volume than the standard 24-pin SOIC, facilitating the use of logic functions on these cards.

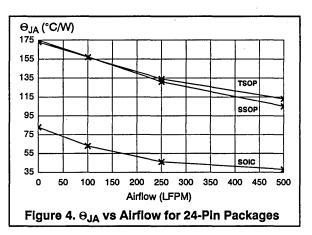
Another way to increase bit density is to reduce the lead pitch of the package. The 48/56-pin shrink small-outline package (SSOP) halves the lead pitch of the SOIC package from 1.27 mm to 0.635 mm, allowing for twice the number of I/0 pins in the same board area. Eight-, nine-, and ten-bit functions now become 16-, 18-, and 20-bit parts. The 100-pin shrink quad flat package (SQFP), along with the high-power cavity-SQFP, further reduce the lead pitch to 0.5 mm. These packages

double the bit density over the 48-pin SSOP with only a 50% increase in area. Both of these high pin count packages allow for 32- and 36-bit logic functions, providing for efficient buffering of today's 32- and 64-bit bus widths.

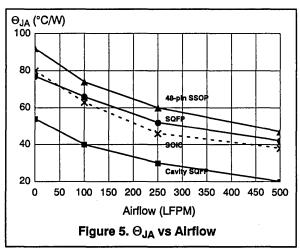


# Thermal Impedances of Fine-Pitch Packages

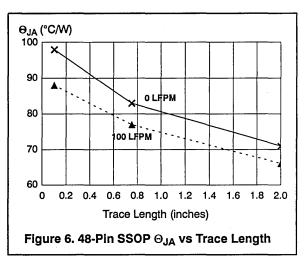
As package area decreases, which is the case for the 20- and 24-pin SSOP and TSOP, the thermal impedance of the package to the ambient environment ( $\Theta_{JA}$ ) increases. Figure 4 illustrates the fact that this relationship is almost linear, and for a 50% reduction in area,  $\Theta_{JA}$  doubles for the 24-pin SSOP and TSOP. Because of the higher  $\Theta_{JA}$ , additional attention must be given to the power dissipation of the device to insure proper operation.



A similar power consideration occurs with the high pin count packages due to the increased number of bits causing higher power dissipation per package. Figure 5 compares  $\Theta_{JA}$  for the 24-pin SOIC, 48-pin SSOP, 100-pin SQFP, and cavity SQFP. The cavity package mounts the lead frame directly to one of the metal lids of the package. This mounting provides a direct path for the heat to flow from the die to the ambient environment. This package accommodates both cavity up or down assembly allowing for both conduction, into the board, or convection, into the ambient, cooling.



One factor influencing  $\Theta_{JA}$  is the trace length that is connected to the package lead finger. This is because some of the heat is taken out of the package through the lead and dissipated into the board as well as through the package top and into the ambient air. Non-standard trace length factors have been identified as a major contributing factor in differences between different manufacturer's published thermal values. Figure 6 shows the effect that trace length has on the 48-pin SSOP's  $\Theta_{JA}$ .



## **Evolutions in Device Processing**

With the improvements to microprocessor clock rates and memory access times, bus-interface devices have become a larger percentage of the total bus cycle time. To keep pace with the need for faster logic many semiconductor manufactures are utilizing sub-micron BiCMOS processes, utilizing shorter gate lengths and thinner gate oxide for device speed improvements. The reductions in transistor area result in less intrinsic capacitance allowing faster internal gate delays, as well as lowering the output capacitance (Ci/o). With a lower Ci/o, ABT devices minimize their impact to system loading.

In a transmission line environment, when the driver's edge rate is less than twice the line's propagation delay, distributed output loading has the effect of reducing the characteristic impedance (Zo) of the transmission line. The higher the distributed capacitive load, the lower the apparent impedance, making it harder for the driver to switch the line on the incident wave. This well known transmission line loading equations is:

$$Z'_{o} = \frac{Z_{o}}{\sqrt{1 + \frac{C_{d}}{C_{o}}}} \tag{1}$$

where  $Z_{o}$  is the line's unloaded characteristic impedance,  $C_{o}$  is its intrinsic capacitance per unit length, and  $C_{d}$  is the distributed capacitive load per unit length.

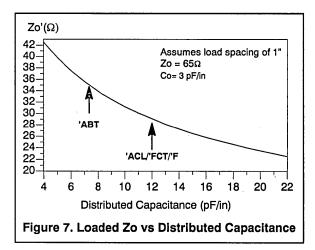


Figure 7 shows how the a device's output capacitance can lower a line's impedance, as in the case of a backplane. If the effects of the other board capacitance contributors — connectors, vias, and trace stubs, are assumed to be constant regardless

of the device used, and thus ignored, a comparison of transmission line loading between different technologies can be made.

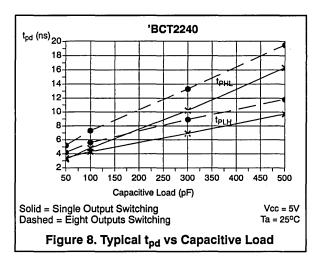
#### 3.3-V Operation

As process geometries move towards gate lengths of 0.5  $\mu$  and below, coupled with the desire for lower power consumption, 3.3-V operation becomes necessary. Because the migration to 3.3 V will be gradual, gated by the availability of semiconductor functions, the need for mixed signal level operation will be critical for bus interface devices. That is the input and I/O pins will be able to have input voltage levels up to 5.5 V without any conduction paths to  $V_{CC}$ . The outputs should also be capable of driving a standard 5-V backplane, which would translate into drive currents of at least -15 mA of  $I_{OH}$  and 64 mA of  $I_{OI}$  .

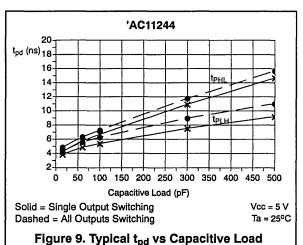
## Advance Bus Interface Solutions

### Memory Driver Usages for the SSOPs

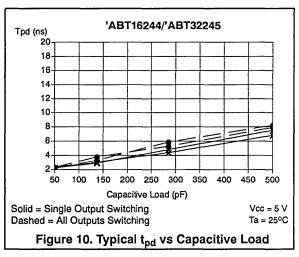
As pointed out above, any of the SSOPs can be utilized as buffers in high-density memory arrays. In many instances, series-dampening termination is chosen, due to its ease of implementation and power savings. Numerous logic devices are available that incorporate the series-dampening resistor on chip, as in the BCT2XXX series of products, simplifying this type of termination. When these parts are packaged in the 20-pin SSOP, as in the 'BCT2240DB, a tremendous board real estate savings is realized over a discrete approach using external resisters and SOIC devices. For PCMCIA cards the driver must also offer low-power consumption, necessary for battery operation. The 'AC11244PW (TSOP package) can be used in these applications due to its low static power CMOS characteristics.



Many times when an output switches a large memory array the capacitive load is localized in close proximity to the driver and can be treated as a simple lumped load. In these instances it is useful to know how the propagation delay  $(t_{pd})$  of the driver changes with the additional capacitive load. The change in the driver's  $t_{pd}$  is due to the interaction of its source impedance,  $R_{on}$ , with the capacitive load,  $C_{l}$ . Figures 8, 9, and 10 show this phenomena for the 'AC11244, 'BCT2240, 'ABT16244, and 'ABT32245 for both single and multiple outputs switching.



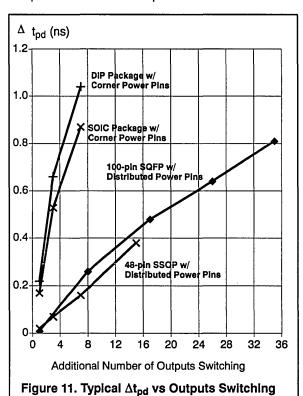
These three figures illustrate the effect that the output impedance of the driver has over tod degradation. Figure 8 shows that even though the 'AC11244 has symmetrical high and low output drive current ratings of 24 mA, tpHI show more degradation versus capacitive loading due to the graded turn-on of the output to minimize simultaneous switching noise [ground bounce]. Many advanced CMOS logic devices utilize this graded turn-on, but not without the penalty of slower propagation delays at higher capacitive loads. Figure 7 shows a similar asymmetrical tell performance, but now it is due to the inclusion of a 33- $\Omega$  series output resistor. Contrasting the previous two graphs is Figure 10 which highlights the high-drive capability of the ABT16XXX and ABT32XXX devices, along with the symmetrical t<sub>nd</sub> performance that the -32/64 mA outputs deliver.



#### **Bus-Interface Usages for the SSOP**

The gains made by utilizing devices with faster propagation delays can be lost if the propagation delay degrades when multiple outputs on a package are switched simultaneously. This effect is greatly reduced when a device is packaged in the 48/56-pin SSOP, because this package allows the signal-to-ground ratio of a standard 8-bit function to be improved from 8:1 to 2:1, and the signal-to-V<sub>CC</sub>

ratio improves from 8:1 to 4:1. This multiple power pin system translates into a quieter on-chip power system when multiple outputs switch, resulting in less propagation delay degradation compared to a standard 8-bit function. The same can be said of the 100-pin SQFP and cavity SQFP which utilizes a 3:1 signal-to-ground ratio. Figure 11 compares the change in t<sub>pd</sub> vs number of outputs switching (in phase) of a typical 244, buffer-type function when packaged in a 48-pin SSOP and 100-pin SQFP to the performance in a 20-pin DIP and SOIC.



#### Conclusion

The various fine pitch surface-mount packages give the designer a wide range of solutions to today's system area and volume constraints. The high pin count SSOP and SQFP packages allow bus-interface devices to track the trend of wider data bus widths, while providing superior electrical performance when compared to the standard end-pin product. The cavity SQFP allows for higher power dissipation applications, allowing the interface device to operate at higher frequencies. The low pin count SSOPs occupy less volume than other surface mount devices, facilitating their use in height critical applications.

#### For Further Information

#### **Transmission Lines**

Advanced Schottky Family Applications, Texas Instruments Advanced Schottky Data Book, 1986.

Advanced CMOS Logic Designer's Handbook, Texas Instruments, 1988.

#### **Power Dissipation**

SSOP Designer's Handbook, Texas Instruments, 1991.

## **ABT Enables Optimal System Design**

Steve Perna General Purpose Logic – Semiconductor Group Texas Instruments Incorporated

#### ABT ENABLES OPTIMAL SYSTEM DESIGN

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As the operating frequencies microprocessors increase, the period of time allotted for memory access, arithmetic computation or similar operation decreases. With this in mind, a new series of Advanced Bus Interface Logic (ABIL) products developed with Instruments' Texas sub-micron Advanced BiCMOS (ABT) process technology assume a prominent role as the key high performance logic needed in today's workstation, personal and portable computer, and telecom systems. The goal of this family of products is to provide system designers a bus interface solution combining high drive capability, low power consumption, signal integrity and propagation delays fast enough to appear transparent with respect to overall system performance. Fine pitch package options simplify layout, reduce required board space and decrease overall system costs. Novel circuit design techniques add value over competitive solutions.

## TRENDS IMPORTANT FOR TODAY'S SYSTEM DESIGNER

Modern system designers face many complex challenges in meeting their design goals. The trends toward (need for) faster cycle times, lower power consumption, smaller footprints, greater reliability and lower total system cost combine to put ever increasing pressure on today's system designer.

The need for faster cycle time has traditionally been addressed by the microprocessor manufacturer. Clock and microprocessor

frequencies have increased steadily with each succeeding product generation. The most advanced RISC processors in development are touting frequencies in the area of 200 MHz. For production systems it is not unusual for processors to run on the order of 50 MHz and above. Increasing clock and microprocessor frequencies are now beginning to put pressure on surrounding memory and logic to make greater contributions in reducing overall system cycle times and improving overall system performance.

Higher performance systems require the designer to focus on total system power requirements. Faster systems traditionally require more power which often means more costly solutions. Power costs money to supply and heat buildup due to this power costs money to remove. Also, excess power consumption adversely affects reliability due to the increase in the junction temperature of the silicon components. Lower power devices reduce requirements for larger power supplies and high cost cooling techniques, and could lead to smaller system packaging.

Occurring in parallel with demands for increased system performance and reduced system power consumption is demand to house systems in smaller cases, boxes, chassis and cabinets. This miniaturization requires that each system component be optimally laid out in silicon, packaged and mounted on the PCB board.

Speed, power, size, cost and reliability are all parameters by which system and end

equipment success are measured. Semiconductor technologies thrived because they were cheap and manufacturers must be sensitive to these readily available. parameters and be able to provide well-defined and designed products to meet these needs.

#### ADVANCED BUS INTERFACE LOGIC (ABIL) AS THE SYSTEM BUS INTERFACE

Semiconductor vendors are required by system design houses to provide new products which are faster, consume less power, exist in smaller packages and present a lower relative cost than their predecessors. Since the early 1970s many different logic product technologies have attempted to meet these demands.

Early logic product technologies often forced the system designer to make tradeoffs. As Figure 1 details, speed and power were the most typical design goals traded off. Solutions such as Schottky or HCMOS respectively offered high

Prop Delay (ns) 1970s Mature Logic 1980s TTL Advanced 30 Logic 25 1990s ABIL 20 15 10 ⊗s 50 100 150 Supply Current (mA) FIGURE 1. ABT ASSUMES OPTIMAL POSITION

speed at the expense of low power or low power at the expense of high speed. In a typical system delay. application this logic sat between only a few interface logic to meet these budget needs because system blocks such as a simple 8 MHz processor, a it is typically much less expensive for the designer slow 256K DRAM, and a local TTL bus. Their to use than higher performance memories or functional role was little more than small-scale processors. integration (SSI) or medium-scale integration (MSI). Despite these shortcomings, early logic

The cycle time requirements for interface logic vary as a function of microprocessor and clock speed. In an 8 MHz system, the total system cycle available for completion of all operations is 250 nanoseconds. This can be roughly budgeted into 160 nanoseconds for the memory access, 45 nanoseconds for processor set-up and 45 nanoseconds for the interface logic (including signal propagation across printed circuit board With 45 nanoseconds available for traces). low-performance interface. forgiving, a technology such as Low-power Schottky or HCMOS can be utilized.

The situation changes dramatically when system speeds increase to 45 or 50 MHz. At 45 MHz only 44 nanoseconds of total cycle time is available to complete all operations. Now, more expensive memories are needed with access times down in the 20 nanosecond range. Microprocessor

> can only be 8 set-ups nanoseconds. This leaves only 16 nanoseconds for interface and signal trace propagation delay. The interface cycle time is a much higher percentage of the total system cycle time at 45 MHz than at 8 MHz.

> As cycle time requirements shrink. each nanosecond becomes critical in meeting the total system 'budget'. The system designer has the option of using higher performance memories. processors or interface logic in additional squeezing

nanoseconds out of the system There is great demand for in using In light of decreasing total system cycle time requirements, the early logic technologies gave way to faster technologies. Significant gains made since the Schottky and HCMOS days result in products which no longer force the system designer into a tradeoff box. New product development in the area of complex memories, processors and ASIC's has led the way for an equal, if not greater, acceleration in new product development for advanced digital logic products.

This development has propelled logic up from the ranks of "glue" status, used to fill in design gaps around the other major system blocks, to its new position as the system "bus interface". Advanced Bus Interface Logic (ABIL) products are now responsible for controlling the signals between the backplane busses and the other major system design blocks. They have become a major system design block in their own right exerting significant influence over the performance of the final design.

In a modern-day system ABIL products are likely to connect many major system design blocks including application specific parallel processors, 4M DRAM's, fast cache SRAM's and complex ASIC gate arrays/standard cells. The task of this new breed of advanced logic is to effectively transceive the address, data and control signals of these IC elements to and from heavily loaded TTL/CMOS/BTL system backplanes.

A wide variety of industry standard and proprietary backplane specs add to the difficulty of the task. At the low-end of the scale, exhibiting data transfer rates in the range of 10-20 MByte/sec, are the PC AT and EISA type busses. For mid-range server and graphics workstation applications, the 50-100 MByte/sec data transfer rate range of Multibus II and Microchannel type busses is typical. High-end server and mainframe computer applications require the greater than 100 MByte/sec data transfer rates of Futurebus + type busses. Transceivers connecting to each of these backplanes need to provide very high drive current capability to effectively and reliably migrate ABIL products from Texas signals across. Instruments uniquely address this need.

### ENABLERS TO CONTINUOUS NEW PRODUCT DEVELOPMENT

Reduction in minimum process dimension, enhanced value-added circuit design techniques, utilization of fine-pitch packaging and incorporation of lower power supply voltages are the most important enablers to continuous new development for logic products.

The minimum process dimension represents the width of the transistor gate region and gives an indication of the switching speed of the transistor. In general, the smaller the minimum process dimension the faster the transistors will switch. An added advantage of reducing the minimum process dimension is the gain in gate density which can be achieved. A gain in gate density results in increased device functionality without a corresponding increase in silicon die area. Currently state-of-the-art high volume production logic processes consider a 0.8 micron minimum process dimension. However, work is ongoing to prototype more advanced processes characterized by 0.6, 0.5 and 0.35 micron minimum process dimensions.

Enhanced value-added circuit design techniques act to greatly increase the functionality of a logic device as well as improving its performance. These techniques often eliminate the need for the designer to utilize discrete components such as resistors, capacitors and diodes because these are built into the silicon device itself. Additionally optimizations in I/O or core circuitry can positively effect speed and power performance.

An aggressive drive exists to convert classic through-hole package approaches to totally above board surface mount approaches. Occurring in parallel is a drive to upgrade existing surface mount packages with finer pin-to-pin pitches so as to minimize total package area. With smaller packages come increased reliance on thermal management techniques however. The increased difficulty in removing heat from the smaller packages may preclude the use inexpensive plastic

packages. The necessity to use ceramic or other alternatives would act to drive design costs up.

Finally, system designers are beginning to drive the semiconductor industry to move below 5 Volts as the baseline for power supply of operation. The migration to lower voltages such as 3.3 Volts enhances the reliability of advanced process technologies exhibiting minimum process dimensions of 0.6microns or lower. The need for low voltage memory and processor product interface, lower device generated noise levels, lower power consumption and increased battery life for unregulated portable systems accelerate the demand for 3.3 Volt logic. New 3.3 Volt logic opportunities will emerge as system designers continue to rely on advanced process technologies.

a sub-micron 0.8 ABT employs minimum process dimension. It combines of and **CMOS** elements both bipolar circuit/process technologies onto a single silicon chip. ABT offers the system designer the best combination of high speed, high drive and low power consumption in the industry. As shown in Figure 1, ABT provides a performance point closer to the origin of the speed/power graph than any other logic technology available. Specifically ABT is based on a CMOS core circuit structure with an NPN bipolar output transistor module added. This means adding about four additional masks to the CMOS process. The current single NPN transistor output structure of ABT has been optimized for 5 Volt operation.

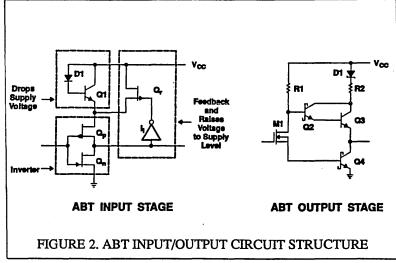
Simplified input and output stages of an ABT transceiver are shown in Figure 2. The

#### WHAT IS ADVANCED BICMOS (ABT)?

Advanced BiCMOS (ABT) is product а technology available today from Texas Instruments to aid designers doing high performance bus management. It is currently available in many different product options including 8-bit octal. 16/18/20-bit Widebus 32/36-bit and Widebus + versions.

At TI ABT evolved from an earlier 1.5 micron BiCMOS process. It was designed to provide speeds

equivalent to existing advanced bipolar solutions but with 90% less device power. This standard BiCMOS introduced high performance, lower power bus interface products to the marketplace two years ahead of the nearest competitor. Since its bus interface introduction in 1987, TI has utilized BiCMOS and Advanced BiCMOS in products such as mixed-signal integrated circuits, high performance gate arrays, high speed cache tags, and application specific processors like the SuperSPARC.



inputs are designed to offer TTL compatible levels with guaranteed switching between a Vih min of 2.0 Volts and a Vil max of 0.8 Volts. Since these inputs are implemented with CMOS circuitry they offer characteristic high impedance for low leakage and low capacitance for minimal bus loading. The CMOS supply voltage of the input stage is dropped by diode D1 and transistor Q1, centering the threshold around 1.5 Volts. When inputs are in the LOW state, Qr raises the voltage of source Qp up to the rail ensuring proper

operation of the feedback stage. This stage provides about 100 mV of input hysteresis increasing noise margins and reducing oscillations.

ABT outputs utilize bipolar circuitry to provide the high speed and drive necessary for bus interface. A major advantage for using bipolar circuitry in the output stage is the reduced voltage swing which lowers ground noise, improves signal integrity and reduces dynamic power consumption. In the figure M1 acts as a current switch which drives the output LOW when conducting current from R1 through to the base of Q4. The base of Q2 is pulled LOW turning off the upper output. For a LOW to HIGH output transition, M1 turns off and current through R1 charges the base of Q2. As Q2 goes high, the Darlington pair Q2 and Q3 turns on. With its supply of base current now cut off, Q4 turns off and the output transition switches LOW to HIGH. R2 limits output current in the HIGH state and D1 is a blocking diode preventing current flow in power-down applications.

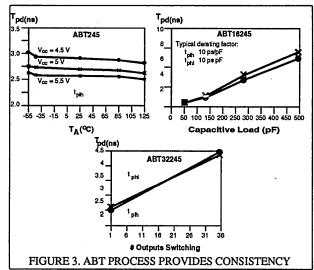
By virtue of its small minimum process geometry, tight metal pitch and shallow junctions, ABT can provide for strong output drive currents (sink currents speced at 64 milliamps and source currents speced at 32 milliamps) and low parasitic capacitances. As a result of these enhancements, internal propagation delays are very fast and very well behaved. Figure 3 shows that typical prop

delays are on the order of 2-3 nanoseconds across temperature. This excellent consistency allows ABT to be specified over the industrial temperature range of -40 to +85 degrees Celsius. The figure also shows that ABT performance is very well behaved across capacitive load and multiple output switching conditions.

Maximum prop delays for ABT are as low as 4-5 nanoseconds depending on the device type and propagation path. Figure 4 compares the datasheet maximums of several ABT 16-bit Widebus transceiver devices with competing FCTB/C CMOS and 74F/ALS bipolar solutions. It is clear from both Figure 3 and Figure 4 that ABT is the system designer's best choice for bus

Registered Transceiver with CLKEN	ABT16952	29FCT52C	F2952					
t <sub>pd</sub> CLK to A/B	4.5 ns	6.3 ns	9.0 ns					
t <sub>pd(en)</sub> OE to A/B	6.0 ns	7.0 ns	10.0 ns					
I <sub>pd(dis)</sub> OE to A/B	5.5 ns	6.5 ns	9.0 ns					
Transceiver with Parity	ABT16657	ABT657	<u>F657</u>					
t <sub>pd</sub> AtoB	4.3 ns	5.5 ns	8.0 ns					
t <sub>net</sub> A to Parity	6.7 ns	11.3 ns	16.0 ns					
t <sub>pd</sub> B to ERROR	6.7 ns	15.7 ns	22.5 ns					
Registered Parity Transceiver	ABT16833	<b>FCT833B</b>	ALS29833					
t <sub>pd</sub> A to B	4.3 ns	7.0 ns	10.0 ns					
t <sub>pd</sub> A to Parity	6.7 ns	10.5 ns	15.0 ns					
t <sub>pd</sub> CLK to ERRO	4.6 ns	15.0 ns	16.0 ns					
FIGURE 4. ABT IS THE SPEED BENCHMARK								

interface applications which require consistent speed performance over many different conditions.



From a power (current) consumption standpoint the use of bipolar in the output stage is advantageous for two reasons. First the voltage swing is less than that of a CMOS output. The power consumed when charging or discharging internal circuit capacitances and the external capacitance is reduced. Second the bipolar transistors are capable of turning off more efficiently than CMOS transistors. wasteful flow of current from Vcc to GND is reduced. Although bipolar does tend to have a high static power consumption, its lower dynamic power consumption allows for better overall power performance at high frequencies than either pure bipolar or

CMOS. This is because the dynamic power component makes up the majority of a device's overall power consumption.

The ABT maximum high impedance supply currents (Iccz) range from about 50 microamps for 8-bit octals to about 2-3 milliamps for 16-bit Widebus products. Maximum dynamic supply currents (Iccl) range from about 30 milliamps for 8-bit octals to about 34 milliamps for 16-bit Widebus products. Power-on-demand, an enhanced circuit design improvement to the bipolar output stage on new ABT product families, reduces dynamic current consumption levels by up to 50%. High impedance and dynamic supply current goals for the new 32/36-bit Widebus + family are 500 microamps and 60 milliamps respectively.

Bus Hold, shown in Figure 5, is another

entities are periodically required to be in 3-state. Bus Hold cells eliminate passive pull-up (to Vcc) or pull-down (to GND) termination resistors necessary to prevent application problems or oscillations. External provision for these resistors by the system designer consumes board area, increases bus capacitance, contributes to bus loading and lowers system performance. The Bus Hold feature is particularly effective when offered on products with a lot of I/O capability such as 32/36-bit Widebus + devices.

#### FINE-PITCH PACKAGING SHRINKS ABT DEVICE SIZE

As the push for smaller system sizes becomes intense, the system designer will require the logic manufacturer to house high performance

silicon in increasingly space conscious packages.

Most notably the system designer has been leveraging the advantages of plastic leaded chip carriers (PLCC's) and small outline integrated circuits (SOIC's)

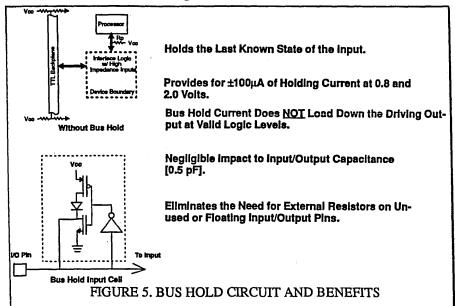
(SOIC's).

Both PLCC and SOIC packages provide a gull wing lead profile. Both utilize a 1.27

millimeter
pin-to-pin
spacing.

pitch
The

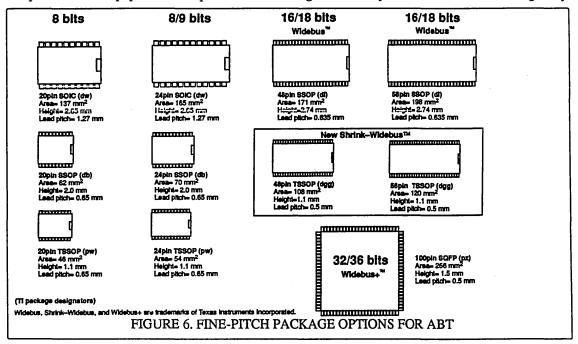
reduced pitch offers a huge space improvement over bulky plastic dual-in-line (PDIP) through-hole packages. The major difference between PLCC and SOIC is philosophical. The PLCC has pins on all four sides (arranged either in square or rectangular configuration) while the SOIC has pins on only two sides (arranged in flow through configuration).



example of an enhanced, value-added circuit design technique available on new ABT product families. The Bus Hold cell provides for a small holding current of 100 microamps to be delivered to I/O pins configured as inputs left unused or floating. This current latches the last known input state to a valid logic level. Floating input conditions are common to CMOS backplanes or device bus interface situations where driving

In spite of the advantages of PLCC and density constant. SOIC, system designers are beginning to specify surface mount packages with finer pitch values to increasing pin count and reducing pin pitch.

package while keeping the pin count and bit The second path considers increasing the bit density of the package by keep their end equipments competitive in the Figure 6 clearly shows both of these migratory



marketplace or to avoid falling behind more paths starting from the standard octal SOIC aggressive rivals. available in volume today offer improvements in the pin-to-pin pitch down to 0.635 millimeters. More advanced fine pitch alternatives exhibiting characteristic pitches of 0.5, 0.4 and 0.3 millimeters are on the horizon.

The plastic quad flat pack (PQFP) is a fine-pitch version of the PLCC package. It offers a 0.635 millimeter pitch and is widely used for microprocessors, ASIC's or other custom devices. The 44-pin POFP is the smallest used in volume while the largest versions provide over 200 pin capability. For the system designer using ABIL products however, it is advantageous to combine the fine-pitch capability of the PQFP with the two-sided dual-in-line design of the SOIC.

SOIC's have evolved in two distinct paths to meet this need. The first path considers reducing the surface area and pin pitch of the

Such fine pitch versions package in the upper left hand corner.

Package size reductions are shown vertically down the figure with each succeeding reduction occupying a new row at constant bit density and pin count. Bit density and pin count increases are shown horizontally across the figure.

There are five new fine-pitch packages represented in the figure. Four of these offer a density upgrade path for the SOIC. The fifth is a new package offering a density upgrade for the PQFP. All of these packages were developed and standardized exclusively for high performance ABIL ABT products by TI.

The Shrink Small Outline Package (SSOP) is available in two worldwide standard form factors. The first, approved by the Joint Electron Device Engineering Council (JEDEC). allows for 16-, 18-, or 20-bit I/O functions in a

package roughly the same size as the octal SOIC. The pin pitch for the JEDEC SSOP is 0.635 millimeters. The JEDEC SSOP is available in a 48-pin version for basic 16-bit driver and transceiver functions and in a 56-pin version for complex 16- to 20-bit transceiver functions. The very popular ABT Widebus family uses the JEDEC approved SSOP.

The second form factor, approved by the Electronics Industry Association of Japan (EIAJ), allows for 8- and 9-bit I/O functions in a package about 40% of the size of the octal SOIC. The pin pitch for the EIAJ SSOP is 0.65 millimeters. The EIAJ SSOP is available in a 20-pin version for basic ABT 8-bit driver and transceiver functions and in a 24-pin version for complex ABT 8- and 9-bit transceiver functions.

Bottom row of figure 6 represents the third form factor upgrade to the SOIC available from TI. The Thin Shrink Small Outline Package (TSSOP) is EIAJ approved and offers a reduced thickness (height) spec of 1.1 millimeters. The pin pitch of the EIAJ TSOP is 0.65 millimeters. (The body width is 4.4 millimeters). The TSSOP is compatible to Type I and Type II card physical requirements of the Personal Computer Memory Card International Association (PCMCIA). TSSOP offers the smallest package size available for 20-and 24-pin drivers and transceivers. For denser memory arrays TSSOP facilitates front and back side mount in under 3.3 millimeter thickness specified by PCMCIA if card thicknesses are kept under 1.0millimeters.

For wideword applications with extreme space and height restrictions, TI will offer Widebus devices in a new package called the Shrink Widebus (TM). Available in 48- and 56-pin versions, this new package has a 1.1 millimeter maximum height, a 6.1 millimeter body width and a 0.5 millimeter lead-pitch. The Shrink Widebus package, developed by TI, is registered with the EIAJ, meets the requirements of the PCMCIA and consumes 40 percent less board area than the standard JEDEC SSOP.

Providing the density upgrade path for the PQFP is the EIAJ Shrink Quad Flat Pack

(SQFP). This 100-pin package allows single chip 32- and 36-bit I/O solutions in over 50% less area than with octal SOIC connections. The pin pitch for the EIAJ SQFP is 0.5 millimeters which is the smallest in production today. The reduced pitch of the SQFP offers a 35% area reduction over 100-pin PQFP solutions. The new 32- and 36-bit ABT Widebus + family, recently announced at the BUSCON '92 WEST trade show in Long Beach, California, uses the 100-pin SQFP.

All the above fine-pitch package options are superior for space saving applications. The JEDEC SSOP and EIAJ SQFP are superior in several other areas as well. The JEDEC SSOP incorporates a flow-through architecture where input and output pins each have their own dedicated side of the package. Flow through pinouts offer the system designer a very easy route path for signal traces.

A standard SOIC octal package can only afford 1 GND pin for every 8 I/O's. This ratio improves to 2:1 and 3:1 for JEDEC SSOP and EIAJ SQFP respectively. Both the JEDEC SSOP and the EIAJ SQFP provide multiple Vcc and GND pins distributed along the sides. The improved GND number and distribution of these pinouts is very forgiving from a noise generation standpoint and allows for less propagation delay than octal functions. As a result, ABT octals, ABT Widebus and ABT Widebus + all exhibit less than 1 Volt of noise typically, even though the maximum number of switched outputs increases from 8- to 18- to 36-bits with each respective family.

As package area decreases, the thermal impedance of the package to the ambient environment increases. Thermal impedance represents the ability of a package to dissipate heat. The higher the thermal impedance the more difficulty the package has in dissipating heat. The higher thermal impedances of fine-pitch packages require additional attention and care from the system designer. Proper thermal management techniques as well as proper power dissipation guidelines must be used to ensure operation. Fortunately the low power of ABT ABIL products

NAME	EXAMPLE PART NO.	KEY FEATURES	NUMBER OF BITS	PACKAGES	MAX PROP DELAY (ns)	Iccz (mA)	loL (mA)	I <sub>OH</sub> (mA)	TARGET APPLICATIONS
ABT	SN74ABT245	0.8 micron process, -40/85 °C temperature	8, 9, 10	DIP/SOIC/ SSOP (EIAJ)	4.6	0.05	64	32	High-speed bus interface, PC, EWS, Telecom
ABT Widebus	SN74ABT16245	Flow-through pinouts, low noise	16, 18, 20	SSOP (JEDEC)	4.1	2	64	32	Higher performance, space conscious applications
ABT Widebus+	SN74ABT32245	Bus hold cell, power-on-demand	32, 36	SQFP (EIAJ)	4.9	0.5	64	32	Single chip 32-bit interface
IWS Drivers	SN74ABT25245	Enhanced output drivers	8	DIP/SOIC	4.5	0.1	188	96	25 \(\Omega\) incident wave switching
Memory Drivers	SN74ABT2245	Series output dampening resistors	8, 10, 11, 12, 16, 18, 32, 36	DIP/SOIC/ SSOP (EIAJ)/ SSOP(JEDEC)/ SQFP (EIAJ)	5.0 - 5.5	0.05 - 0.5	12	12	Low noise, high reliability driving, memory interface
Futurebus+	SN74FB2031	BTL port, 2 ns minimum edge rate	8, 9, 18	PQFP/ SSOP (JEDEC) SQFP (EIAJ)	5.5	10	100	3	I.E.E.E. 896.1 backplane Interface
BTL Drivers	SN74FB2033	BTL-TTL level translation	8, 9	PQFP/ SSOP (JEDEC)	5.5	10	100	3	I.E.E.E. 1194.1 backplane Interface
Scope	SN74ABT8245	Testability, built-in self test	8, 16, 18	DIP/SOIC/ SSOP (EIAJ)/ SSOP (JEDEC)/ SQFP (EIAJ)	4.7	0.05	64	32	I.E.E.E. 1149.1 backplane Interface
LVT	SN74LVT245	3.3 V V <sub>CC</sub> , mixed mode, bus hold	8	SOIC/TSOP	6.0	0.2	64	32	Battery portables, notebook computers, POS terminals
LVT Widebus	SN74LVT16245	3.3 V V <sub>CC</sub> , mixed mode, bus hold, power-on-demand	16, 18	SSOP (JEDEC)	5.5	0.1	64	32	Workstations, portable computers

FIGURE 7. ABT PRODUCT AND FEATURE TABLE

is more conducive to a fine-pitch packaging approach than competitive CMOS solutions.

#### ABT PRODUCTS PROVIDE END EQUIPMENT SPECIFIC SOLUTIONS

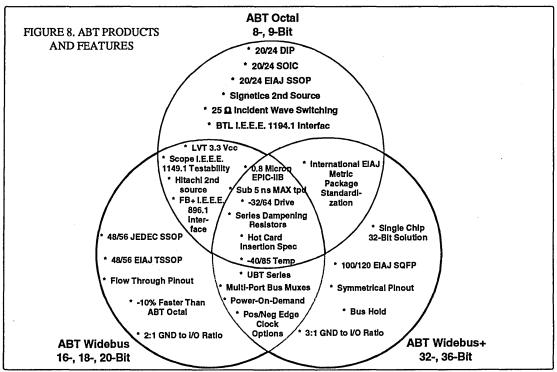
Combining previously discussed state-of-the-art elements of the ABT process with its numerous advanced fine-pitch package options and its enhanced circuit design features yields a very impressive portfolio of new products. These new products emerge to eloquently serve distinct needs of the workstation, personal and portable computer, and telecom end equipment markets.

Figure 7 categorizes the entire ABIL product spectrum built with the ABT process technology. These families offer features and benefits dedicated to specific markets and industry standards. Figure 8 (next page) organizes these features and benefits graphically.

For high performance engineering workstation and server markets, the ABT Widebus and ABT Widebus + families provide the highest integration and performance. They are necessary to connect the most demanding CISC/RISC microprocessors to the most heavily loaded, high frequency backplanes.

The Universal Bus Transceiver (UBT) is unique in the industry because it can be operated in several distinct bus interface modes. Each package contains D-type latches and D-type flip-flops. Flexible control logic options provide for output enable, latch enable, clock and clock enable combinations.

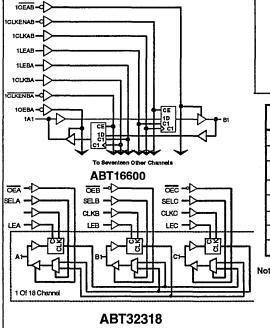
UBT's can be configured as transparent data flow through transceivers (like the dedicated '245 function), latch enabled transceivers (like the dedicated '543 function), clocked registered transceivers (like the dedicated '646 function) and clock enabled registered transceivers (like the dedicated '952 function).



Workstation designers can minimize inventory and procurement requirements, costs and overhead

with UBT flexibility. Designed specifically for workstation bus interface applications, the UBT is perfect as an interface to the many different microprocessor architectures and system backplane specs available.

Figure 9 details the current UBT portfolio from TI and includes block diagrams for 2 devices



SERIES	# OF BITS	# OF PORTS	PACK- AGE	# OF PINS	PARTI- TIONING	PARITY GEN/CH	CONTR OE LE		CLK	
16500	18	2	SSOP	56	x 18	No	Yes	Yes	Yes	No
16600	18	2	SSOP	56	x 18	No	Yes	Yes	Yes	Yes
32316	16	3	SQFP	80	x 16	No	Yes	Yes	Yes	Yes
32318	18	3	SQFP	80	x 18	No	Yes	Yes	Yes	No
32500	36	2	SQFP	100	x 18	No	Yes	Yes	Yes	No
32600	36	2	SQFP	100	x 18	No	Yes	Yes	Yes	Yes
32700	36	2	SQFP	120	x 9	No	Yes Ye		Yes	Yes
32900	36	2	SQFP	120	x 9	Yes	Yes Yes Ye		Yes	Yes

Note: Positive and negative edge triggered clock, and series output dampening resistor options available for each version in the table

FIGURE 9. UNIVERSAL BUS TRANSCIEVER PORTFOLIO

in the series. The ABT16600 is an 18-bit UBT packaged in the 56-pin SSOP package. It can be configured in each of 4 different data flow modes between its A-port and B-port.

The ABT32318 is an 18-bit muxed UBT which can be configured in each of 3 different data flow modes between its A-port, B-port and C-port. This UBT allows the system designer multiple combinations for real-time and stored data exchanges between the three ports. particularly useful for multi-bus communication, multi-way interleaving memory applications and high performance multiplexed address and data bus interface.

The ABT32901 (not pictured) is a 36-bit UBT which provides the most flexibility to the designer packaged in a 120-pin SQFP. devices can be configured in transparent, latched, available in ABT which are compliant with the

Several ABT product families directly address upper end workstation and server equipment. A series of transceivers compliant to the I.E.E.E. 896.1 Futurebus + backplane interface standard are available. The special Futurebus + protocols dictate special electrical requirements of the transceivers in order to ensure proper connection to Futurebus + backplanes. Each of 7 in the series utilize backplane transceiver logic (BTL) switching levels in accordance with the Futurebus + standard. Complementing these Futurebus + transceivers are a series of BTL transceivers compliant with the I.E.E.E. 1194.1 standard. Both transceiver series contain a TTL A-port along with the BTL B-port and can perform TTL-to-BTL and BTL-to-TTL level translation.

Scope transceivers and drivers are

I.E.E.E. 1149.1 testability standard. high For reliability and fault-tolerant system needs these devices provide their own internal self-test capabilities. A complete line of Scope hardware software and system products been have developed by TI.

The personal market computer characterized by very short design cycle times and intense pressure to lower The major driving costs. force is to put workstation-type performance in machines

3 VOLT 3 VOLT TO 5 VOLT INTERFACE 5 VOLT TTL (4.5 V - 5.5 V) 5.0 V LVCMOS LVTTL (2.6 V - 3.6 V) (3.0 V - 3.6 V) CMOS Pull-UP/ 3.3 V High-Drive Bipolar Pull-Down For For TTL Backplane Driving = V<sub>CC</sub> - 0.1 Rail-toRail Switching - 2.4 V - 2.0 V - 2.0 V - 1.5 V - 0.8 V 0.8 V V<sub>⊩</sub> -<del>[2]</del>-0.2 V<sub>cc</sub> - 0.5 V LVT Output Structure Provides Mixed Mode Operation: 0 V 2.7 TO 3.6 V V, = 0 V FIGURE 10. LVT PROVIDES OPTIMIZED 3.3 VOLT I/O

clocked or clock enabled data flow modes and has additional benefits of parity generate and check as well as byte (x9) enable. The 120-pin SQFP offers the same 14 x 14 millimeter body sizes as the 100-pin SOFP, but with a 0.4 millimeter leadpitch.

designed for desktop, home and portable applications. ABT in fine-pitch package options meets these needs nicely.

A new series of low voltage products definitively addresses the needs of the portable sub-segment of this market. The Low Voltage Technology (LVT) family has been developed with the sub-micron ABT process and will be available in both 8-bit octal and 16/18-bit Widebus density versions. Supply voltage for LVT is specified from 2.7 Volts to 3.6 Volts. LVT 8-bit product uses the TSOP to facilitate the smallest area for portable applications. LVT Widebus product uses both the JEDEC SSOP and the 48/56-pin EIAJ Shrink Widebus SSOP.

Market requirements for 3.3 Volt logic products are being driven now by battery laptops and hand-held instruments. Higher performance desktop PC's and workstations could lag a year behind portables in their demand for 3.3 Volt logic.

As shown in Figure 10, the 5 Volt ABT I/O structure has been optimized for use with 3.3 Volt supply currents. LVT 3.3 Volt speed performance is equivalent to ABT 5 Volt speed performance. This special I/O circuitry also allows for a "mixed-mode" 3.3 Volt to 5 Volt interface capability. Designers can use the same LVT logic for core 3.3 Volt system partition as for external 5 Volt backplane interface. This is particularly important as other system elements (microprocessors, ASIC's, memories) migrate to 3.3 Volts at different rates.

LVT I/O circuitry provides multiple output current ratings for multiple system requirements. LVT devices are specified to drive at rail-to-rail low voltage CMOS levels and standard 5 Volt TTL levels. LVT employs Bus Hold and Power-on-demand circuits increasing reliability, decreasing discrete component count and minimizing enabled and disabled static power consumption. Maximum Iccl, Icch, and Iccz current specs are 5, 0.1 and 0.1 milliamps respectively.

The majority of classic telecom end equipments can be classified into switching and transmission categories. Switching equipment such as central offices, cross connects and branch exchanges are analogous to large mainframes or supercomputers. ABT octal and Widebus product families are targeted for these telecom equipments.

For transmission equipment such as line cards, bridgers and routers, product with enhanced

datasheet specifications covering hot card insertion and power up/down is required. In these applications a board (card) is typically removed (inserted) from an active (hot) system for upgrade, maintenance i OT repair. The additional specifications characterize the device's performance when supply currents change (ramp) rapidly.

It is necessary to know how the device behaves when Vcc is 0 Volts, when Vcc is at the rail (5.5 Volts) and when Vcc ramps between these voltages. To address this requirement specifically for telecom transmission applications, ABT transceiver datasheets take into account Ii, Iozh, Iozl and Ioz current conditions for various Vcc ramp rates. Transmission system designers can then profile ABT device performance in hot card insertion and power up/down conditions.

#### **SUMMARY**

Texas Instruments provides the system designer with the most advanced products to date aiding the solution of complex design challenges. Advanced Bus Interface Logic (ABIL) products processed in sub-micron Advanced BiCMOS (ABT) address specific end equipment demands of the workstation, personal and portable computer, and telecom markets. Advanced fine-pitch package options such as SSOP, TSOP and SQFP offer space saving form factors. Circuit design techniques such as Bus Hold and Power-on-demand add value over competitive solutions.

The evolutionary roadmaps of process and package technology are summarized graphically in Figure 11 (next page). Solid lines indicate process technology migration for CMOS and BiCMOS. The minimum process dimension is represented on the ordinate in units of microns. The dashed line indicates package technology migration from PDIP to SOIC to SSOP to SQFP. For the dashed line, the ordinate now represents minimum lead pitch in millimeters.

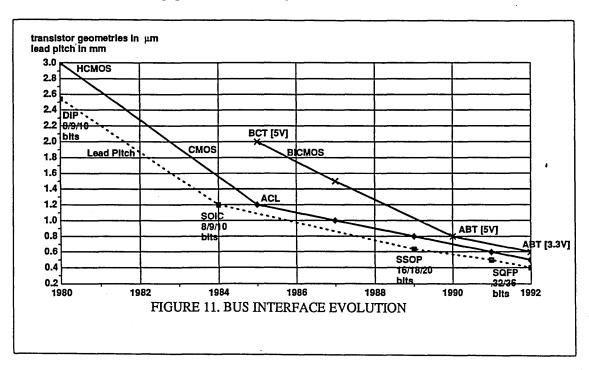
The figure points out some interesting trends. BiCMOS solutions, initially well behind

their CMOS cousins in terms of performance, have closed the gap almost completely during the past 6 years. For 5 Volt logic applications ABT offers significant opportunity over an equivalent CMOS version particularly with the advent of thermally sensitive fine-pitch packages like the SQFP.

The Advanced BiCMOS opportunity is to provide more processing capability and overall throughput at a time when the next generation CMOS technologies are not quite ready or where a mixed technology approach provides a more practical solution. For ABIL products the high performance and drive capability of ABT are necessary for rack-mount supercomputers, workstation and telecom switching equipment. However, the low power consumption of ABT is necessary if these end equipments are to easily

exist on the desktop. Low voltage LVT product appears positioned to supply personal computer and battery systems as they strive to incorporate workstation performance in portable formats.

As process geometries drop to 0.6 microns and below, Advanced BiCMOS and Advanced CMOS will continue to do battle in the pursuit of the best low voltage solutions. Future enhancements to Advanced BiCMOS may include extensions to a complementary structure of NPN and PNP transistors to better cope with reduction in power supply voltages. As supply voltages drop to 2.6 Volts and below, it appears more than likely that Advanced BiCMOS and Advanced CMOS will coexist as viable product technologies each supporting a dedicated group of customers. Time will tell.



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# ABT Advanced BiCMOS Technology Characterization Information

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#### INTRODUCTION

The purpose of this document is to assist the designers of high-performance digital logic systems in using the advanced BiCMOS technology logic family, referred to as ABT.

Detailed electrical characteristics of these bus interface devices are provided and, if available, tables and graphs have been included that compare specific parameters of the ABT family with those of other logic families.

In addition, typical data is provided to give the hardware designer a better understanding of how the ABT devices operate under various conditions. The major subject areas covered in the report are as follows:

- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- Advanced Packaging
- Characterization Information

The characterization information provided is typical data and is not intended to be used as minimum or maximum specifications, unless noted as such.

For more information on Texas Instruments ABT logic products, please contact your local TI field sales office or an authorized distributor, or call Texas Instruments at 1-800-336-5236.

#### **AC PERFORMANCE**

As microprocessor operating frequencies increase, the period of time allotted for operations, such as memory access or arithmetic functions, decreases. With this in mind, Texas Instruments has developed a new family of bus interface devices—ABT, utilizing advanced BiCMOS technology. The goal of the ABT family of devices is to give system designers one bus interface solution which provides high drive capability, good signal integrity, and propagation delays short enough to appear transparent with respect to overall system performance.

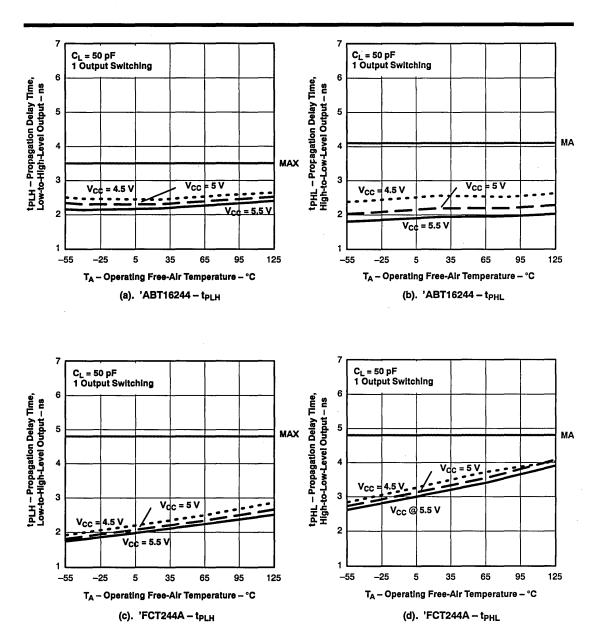
Advances in IC process technology including smaller minimum feature size, tighter metal pitch, and shallower junctions, combine to provide stronger drive strengths and smaller parasitic capacitances. As a result, internal propagation delays have become extremely short. With the advent of the 0.8-µm, EPIC-IIB MEDICMOS process and new circuit innovations, the ABT family offers typical propagation delays as low as 2-3 ns as shown in Figure 1. Maximum specifications are as low as 3-5 ns depending on the device type.

Figure 2 shows the propagation delay versus change in both temperature and supply voltage for an ABT16244, FCT244A, and a F244 device. The graphs highlight two important aspects of the new ABT logic family. First, ABT interface devices have extremely short propagation delay

times. The figures clearly show the improvement in speed of an ABT device over that of a 74F and 74FCTA device. Second, the variance in speed with respect to both temperature and supply voltage is minimal for ABT. At low temperatures, the increase in CMOS performance compensates for the decrease in bipolar device strength. At high temperatures, the reverse occurs. This complementary performance of both CMOS and bipolar devices on a single chip results in a slope which is virtually flat across the entire temperature range of -55°C to 125°C.

For most applications, the datasheet specifications may not provide all of the information a designer would like to see for a particular device. For instance, a designer might benefit from data such as propagation delay with multiple outputs switching or with various loads. This type of data is extremely difficult to test using automatic test equipment; therefore, it is provided in this document as family characteristics shown in Figure 2 and Figure 3.

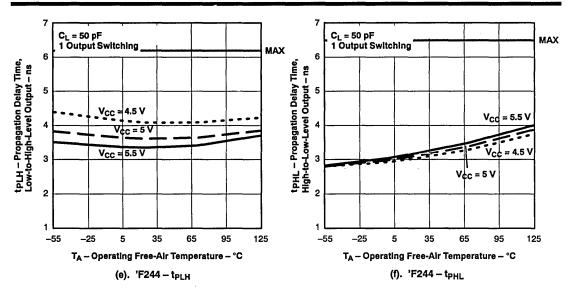
In order to get a clear picture of where ABT stands in reference to other logic families, data is shown for a comparable (same function) 74F and 74FCTA device. It is clear that ABT is the designer's best choice for bus-interface applications which require consistent speed performance over various conditions.



NOTE: MAX is datasheet specification.

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y





NOTE: MAX is datasheet specification.

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y (continued)

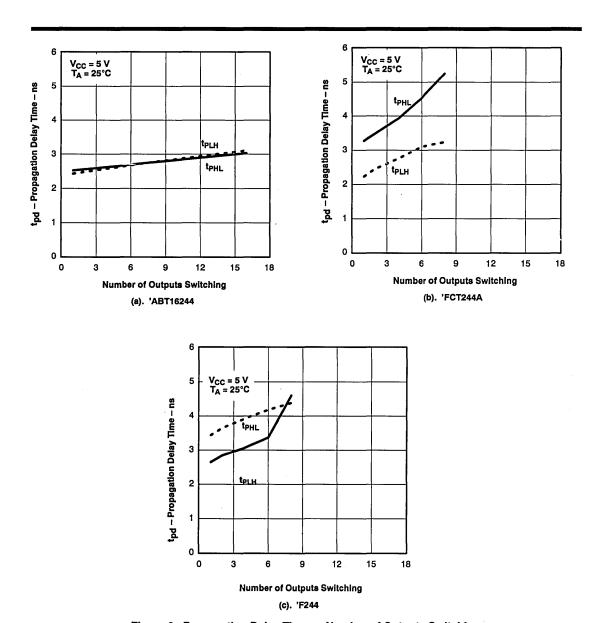
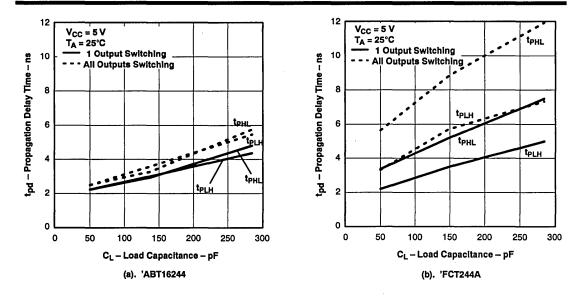


Figure 2. Propagation Delay Time vs Number of Outputs Switching



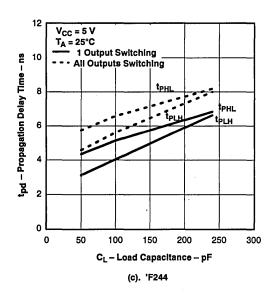


Figure 3. Propagation Delay Time vs Capacitive Load

#### POWER CONSIDERATIONS

With the challenge to make systems more dense while improving performance comes the need to replace power-hungry devices without compromising speed. The ABT family of drivers provides a solution with low CMOS power consumption and high-speed bipolar technology together on a single device.

There are two basic things to consider when calculating power consumption, static (dc) power and dynamic power. Static power is calculated using the value of I<sub>CC</sub> as shown in the datasheet. This is a dc value with no load on the outputs. To understand the relationship between pure CMOS, pure bipolar, and advanced BiCMOS for dc power rating, see Table 1 which shows the various datasheet values. The bipolar device shows the highest I<sub>CC</sub> values, with little relief regardless of the state of the outputs. This is not the case with ABT octals, which offer the low static power consumption of CMOS while in the high-impedance state, or when the outputs are high (I<sub>CCZ</sub>, I<sub>CCH</sub>).

Dynamic power involves the charging and discharging of internal capacitances as well as the external load capacitance. It is this dynamic component which makes up the majority of the total power dissipation. Figure 4 shows power as a function of frequency for ABT, FCT and F devices. Although bipolar devices tend to have extremely high static power, there is a point on the frequency curve, commonly referred to as the crossover point, where the CMOS device no longer consumes less power. With ABT devices, the power increase at higher frequencies is less than that of the pure CMOS FCT.

The use of bipolar transistors in the output stage is advantageous in two ways. First, the voltage swing is less than with a CMOS output, reducing the power consumed when charging or discharging the external load. Second, bipolar transistors are capable of turning off more efficiently than CMOS transistors, thus reducing the flow of current from V<sub>CC</sub> to GND. Combined, these features allow for better power performance at high frequencies.

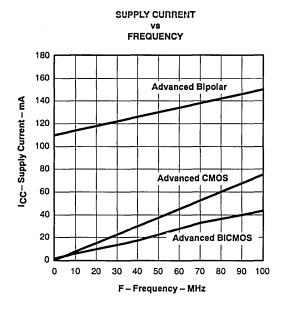


Figure 4. Supply Current vs Frequency

Table 1. Supply Current

DADAMETED	TEST COMPLETIONS		'F2	'F244		'FCT244		SN74ABT244	
PARAMETER	[ "	ST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	
	$V_{CC} = 5.5 \text{ V},$ Outputs high $I_{O} = 0,$ Outputs low $V_{I} = V_{CC}$ or GND Outputs disabled	Outputs high		60 mA				250 μΑ	
lcc		Outputs low		90 mA				30 mA	
			90 mA				250 μΑ		
lcc	V <sub>CC</sub> = maximum, V ≥ V <sub>CC</sub>	$v = 0.2 \text{ V, V} \le V_{CC} = 0.2 \text{ V}$				1.5 mA			

#### **INPUT CHARACTERISTICS**

ABT bus interface devices are designed to guarantee TTL-compatible input levels switching between 0.8 V and 2 V (typically 1.5 V). Additionally, these inputs are implemented with CMOS circuitry, resulting in high impedance (low leakage) and low capacitance which reduces overall bus loading. This section is an overview of the circuitry utilized for a typical ABT input, the corresponding electrical characteristics, and guidelines for proper termination of unused inputs.

#### **ABT Input Circuitry**

Figure 5 shows a typical ABT input schematic. A pure CMOS-input threshold is normally set at one half of V<sub>CC</sub>. In

order to shift the threshold voltage to be centered around 1.5 V (see Figure 6), the supply voltage of the input stage is dropped by the diode, D1, and the transistor, Q1. Reducing the voltage at the source of  $Q_p$  enables it to turn off more efficiently when flow is from  $V_{CC}$  to GND ( $\Delta I_{CC}$ ). When the input is in the low state,  $Q_r$  raises the voltage of the source of  $Q_p$  to  $V_{CC}$  to ensure proper operation of the following stage. This feedback circuit provides approximately 100 mV of input hysteresis which increases the noise margin and helps ensure the device will be free from oscillations when operated within specified input ramp rates.

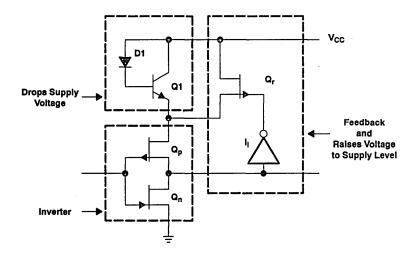


Figure 5. Simplified Input Stage of an ABT Circuit

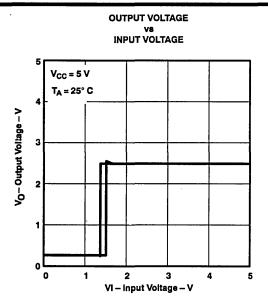


Figure 6. Output Voltage vs Input Voltage

#### INPUT CURRENT LOADING

The utilization of sub-micron (0.8- $\mu$ m) CMOS technology for the input stage of ABT devices causes minimal loading of the system bus due to low leakage currents and low capacitance. The small geometries of the EPIC-IIB  $\mu$  process have resulted in capacitances as low as 3 pF for inputs and 8 pF for  $\mu$ 0 of a transceiver. Figure 7 and Table 2 indicate the low input current performance and specifications. Considering this low capacitance along with the negligible input current, it is clear that systems designers will be able to decrease their overall bus loading.

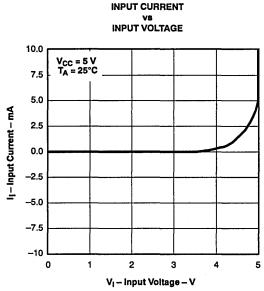


Figure 7. Input Current vs Input Voltage

**Table 2. Input Current Specifications** 

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54A	BT245	SN74ABT245		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
l <sub>i</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> =V <sub>CC</sub> or GND			±1		±1		±1	μΑ
lozht	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> =2.7 V			50		50		50	μΑ
lozLt	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> =0.5 V			-50		-50		-50	μА

<sup>†</sup> The parameters IOZH and IOZL include the input leakage current

#### SUPPLY CURRENT CHANGE (AICC)

Because ABT devices utilize a CMOS-input stage but operate in a TTL-level signal environment, there is a current specification unique to this set of conditions known as  $\Delta I_{CC}$ . Given a CMOS inverter with the input voltage set so that both the p and n channel devices are on, current will flow from  $V_{CC}$  to GND. This can occur when the input to an ABT device is at a valid high level (>2 V) which will turn on the n-channel, but not high enough to completely turn off the p-channel

device. The current which flows under these conditions is specified in the datasheet ( $\Delta I_{CC}$ ) and is measured one input at a time with the input voltage set at 3.4 V. Figure 8 shows the change in  $I_{CC}$  as the input is ramped from 0 V to 5 V. For ABT non-storage devices, a feature is added which turns the input off when the outputs are disabled in order to reduce power consumption (see Table 3 for an example. Refer to individual datasheets for this specification).

# SUPPLY CURRENT VS INPUT VOLTAGE

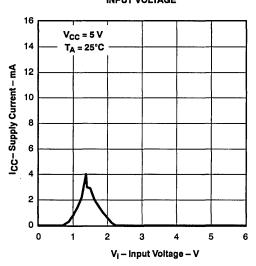


Figure 8. Supply Current vs Input Voltage

Table 3. Supply Current Change (∆I<sub>CC</sub>)

PARAMETER	TEST CONDITIONS			T <sub>A</sub> = 25°C			BT244	SN74ABT244		UNIT	
	LR	1EST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	Oitil
Αι .	A1 +	V <sub>I</sub> = 5.5 V, One input at 3.4 V,	Outputs enabled			1.5		1.5		1.5	mA
Δlcc <sup>†</sup>	Other inputs at V <sub>CC</sub> or GND Outputs disabled				50		50		50	μΑ	

<sup>†</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### **Proper Termination of Unused Inputs**

With advancements in speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output glitching or, in some cases, oscillations. Similar situations can occur if an unused input is left floating or not being actively held at a valid logic level.

These problems are due to voltage transients induced on the device's power system as the output load current (I<sub>O</sub>) flows through the parasitic lead inductances during switching (see Figure 9). Since the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, the inductive voltage spikes (V<sub>gnd</sub>) affect the way signals appear to the internal gate structures. For instance, as the voltage at the device's ground node rises, the input signal (V<sub>i</sub>') will appear to decrease in magnitude. This undesirable

phenomena can erroneously change the output's transition if a threshold violation takes place.

In the case of a slowly rising input edge, if the ground movement is large enough, the apparent signal, Vi', at the device will appear to be driven back through the threshold and the output will start to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents) the slow input edge will be repeatedly driven back through the threshold, resulting in output oscillation.

ABT devices are recommended to have input edge rates faster than 5 ns/V for standard parts, and 10 ns/V for the Widebus series of products when the outputs are enabled. A critical area for this edge rate is in the transition region between 1 V and 2 V. It is also recommended to hold inputs or I/O pins at a valid logic high or low when they are not being used or when the part driving them is in the high-impedance state.

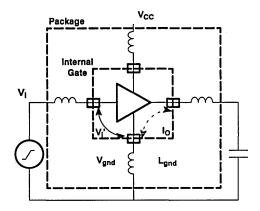


Figure 9. Sample Input/Output Model

#### **OUTPUT CHARACTERISTICS**

The current trend is consolidation of the functionality of multiple logic devices into complex, high pin-count ASICs and programmables. There are a number of important advantages for utilizing bus interface devices in standard high-volume packages. These include the need for high drive capability and good signal integrity. The use of bipolar circuitry in the output stage makes it possible to provide these requirements, along with increased speed, using the ABT family.

Figure 10 shows a simplified schematic of an ABT output stage. Data is transmitted to the gate of M1, which acts as a simple current switch. When M1 is turned on, current flows through R1 and M1 to the base of Q4, turning it on and driving the output low. At the same time, the base of Q2 is pulled low,

thus turning off the upper output. For a low-to-high transition, the gate of M1 must be driven low, turning M1 off. Current through R1 will charge the base of Q2, pulling it high and turning on the Darlington pair consisting of Q2 and Q3. Meanwhile, with its supply of base drive cut off, Q4 turns off, and the output switches from low to high. R2 is used to limit output current in the high state, and D1 is a blocking diode used to prevent reverse current flow in specific power-down applications.

A clear advantage of using bipolar circuitry in the output stage (as opposed to CMOS) is the reduced voltage swing. This helps to lower ground noise and reduce power consumption. Refer to the sections on Signal Integrity and Power Considerations for further information.

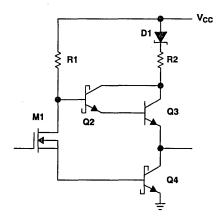


Figure 10. Simplified ABT Output Stage

#### **Output Drive**

The I<sub>OH</sub> and I<sub>OL</sub> curves for a typical ABT output are shown in Figure 11. With a specified I<sub>OL</sub> of 64 mA and I<sub>OH</sub> of -32 mA, ABT will accommodate many standard backplane specifications. However, these devices are capable of driving well beyond these limits. This is important when considering switching a low-impedance backplane on the incident wave.

Incident-wave switching ensures that for a given transition (either high-to-low or low-to-high) the output will reach a valid  $V_{IH}$  or  $V_{IL}$  level on the initial wave front (i.e., does not require reflections). Figure 12 shows the possible problems a designer might encounter when a device does not switch on the incident wave. A shelf below  $V_{IL(max)}$ , signal A, will cause the propagation delay to slow by the amount of time it takes for the signal to reach the receiver and reflect back. Signal B shows the case where there is a shelf in the threshold region. When this happens the input to the receiver is uncertain and could cause several problems associated with slow input edges, depending on the length of time the shelf remains in this region. A signal as seen in example C will not cause a problem because the shelf does not occur until the necessary  $V_{IH}$  level has been attained.

Using typical  $V_{OH}$  and  $V_{OL}$  values along with data points from the curves, ABT devices can typically drive lines in the  $25-\Omega$  range on the incident wave.

For a low-to-high transition,  $(I_{OH} = 85 \text{ mA} @ V_{OH} = 2.4 \text{ V})$ 

$$Z_{LH} = \frac{V_{OH}(min) - V_{OL}(typ)}{I_{OH}} = \frac{2.4 \text{ V} - 0.3 \text{ V}}{85 \text{ mA}} = 25 \Omega$$

For a high-to-low transition, (I<sub>OL</sub>= 135 mA @ V<sub>OL</sub>= 0.5 V)

$$Z_{HL} = \frac{V_{OH}(typ) - V_{OL}(max)}{I_{OL}} = \frac{3.5 \text{ V} - 0.5 \text{ V}}{135 \text{ mA}} = 22 \Omega$$

# LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT 1.0 V<sub>CC</sub> = 5 V T<sub>A</sub> = 25°C 0.6 0.6 0.7 0.7 0.7 0.8

60

80

100

120

140

0

20

40

# HIGH-LEVEL OUTPUT VOLTAGE V8 HIGH-LEVEL OUTPUT CURRENT

IOL - Low-Level Output Current - mA

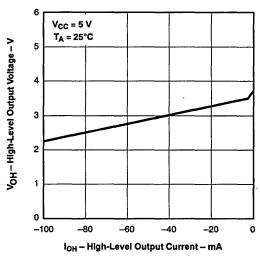


Figure 11. Typical ABT Output Characteristics

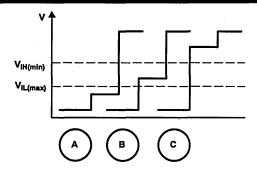


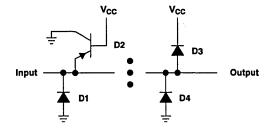
Figure 12. Reflected Wave Switching

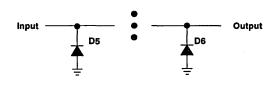
### **Partial Power Down**

One application, addressed when designing the ABT family, is partial system power down. When using a standard CMOS device, there is a path from either the input or the output (or both) to  $V_{CC}$ . This prevents partial power down for such applications as *hot card insertion* without adding current limiting components. This is not the case with ABT as these paths have been eliminated with the use of blocking diodes.

Figure 13 shows functionally equivalent schematics of the input structures for CMOS and ABT devices.

Consider the situation shown in Figure 14. The driving device is powered with  $V_{\rm CC}=5$  V while the receiving device is powered down ( $V_{\rm CC}=0$ ). If these devices are CMOS, the receiver can be powered up through the diode, D2, when the driver is in a high state. ABT devices do not have a comparable path and are thus immune to this problem, making them more desirable for this application.





(a) CMOS EQUIVALENT INPUT STRUCTURE

(b) ABT EQUIVALENT INPUT STRUCTURE

Figure 13. Simplified Input Structures for CMOS and ABT Devices

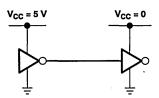


Figure 14. Example of Partial System Power Down

### SIGNAL INTEGRITY

A frequent concern system designers have is the performance degradation of ICs when outputs are switched. Texas Instruments priority when designing the ABT bus interface family is to insure signal integrity and eliminate the need for excess settling time of an output waveform. This section addresses the simultaneous switching performance of both the ABT octals and the Widebus™ functions.

### Simultaneous Switching Phenomenon

NO TAG shows a simple model of an output pin, including the associated capacitance of the output load and the inherent inductance of the ground lead. The voltage drop across the GND inductor, VL, is determined by the value of the inductance and the rate of change in current across the inductor. When multiple outputs are switched from high to low, the transient current (di/dt) through the GND inductor generates a difference in potential on the chip ground with respect to the system ground. This induced GND variation can be observed indirectly as shown in Figure 16. The voltage output low peak (VOLP) is measured on one quiet output when all others are switched from high to low.

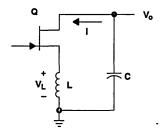
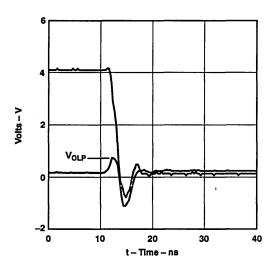


Figure 15. Simultaneous Switching Output Model



NOTE: VolP = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs

Figure 16. Simultaneous Switching Noise Waveform



### **ABT FAMILY CHARACTERISTICS**

A similar phenomena occurs with respect to the  $V_{CC}$  plane on a low-to-high transition, known as voltage output high valley  $(V_{OHV})$ . Most problems are associated with a large  $V_{OLP}$  because the range for a logic 0 is much less than the range for a logic 1, as seen in Figure 17. For a comprehensive discussion of simultaneous switching, see the "Simultaneous Switching Evaluation and Testing" application note or the Advanced CMOS Logic Designer's Handbook from Texas Instruments.

The impact of these voltage noise spikes on a system can be extreme. The noise can cause loss of stored data, severe speed degradation, false clocking, and/or reduction in system noise immunity. For an overview of how propagation delay is affected by the switching of multiple outputs, please refer to the AC Performance section of this document.

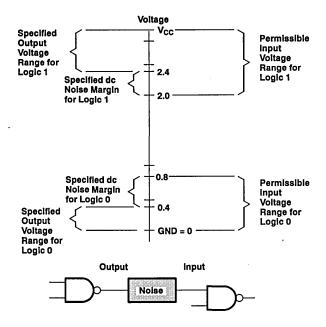


Figure 17. TTL dc Noise Margin

### Simultaneous Switching Solutions

Some methods an IC manufacturer can use to reduce the effects of simultaneous switching include: reducing the inductance of the power pins, adding multiple power pins, and controlling the turn on of the output. These techniques are described in depth in the 1988 Texas Instruments Advanced CMOS Logic (ACL) Designer's Handbook.

Octal ABT devices employ the standard end-pin GND and  $V_{\rm CC}$  configuration while maintaining acceptable simultaneous switching performance, as seen in Figure 18. This is due to the TTL-level output swing (0.3–3 V) and a controlled feedback which limits the base drive to the lower output.

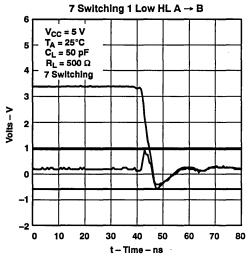


Figure 18. ABT646A Simultaneous Switching Waveform

The ABT Widebus<sup>TM</sup> series (16-, 18-, and 20-bit functions) are offered in an SSOP package (see the Packaging section of this document) which was developed by Texas Instruments to save valuable board space and reduce simultaneous switching effects. One might expect an increase in noise with sixteen outputs switching in a single package; however, the simultaneous switching performance is actually improved. There is a GND pin for every two outputs and a V<sub>CC</sub> pin for every four. This allows the transient current to be distributed across multiple power pins and decreases the overall d<sub>j</sub>/d<sub>t</sub> effect. This results in a typical V<sub>OLP</sub> value on the order of 500 mV for the ABT16500, as shown in Figure 19.

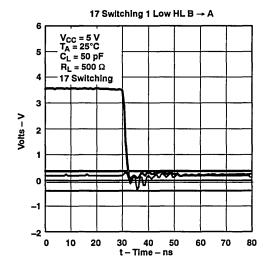


Figure 19. ABT16500A Simultaneous Switching Waveform

### ADVANCED PACKAGING

Along with a strong commitment to provide fast, low-power, high-drive integrated circuits, Texas Instruments is the clear-cut leader in logic packaging advancements. The development of the shrink small-outline package (SSOP) in 1989 provided system designers the opportunity to reduce the amount of board space required for bus interface devices by 50%. Several 24-pin solutions including the familiar SOIC, the SSOP, and the TSOP (thin small-outline package) are shown in Figure 20.

The 48/56-pin SSOP packages allow for twice the functionality (16-, 18-, and 20-bit functions) in

approximately the same board area as a standard SOIC. This is accomplished by using a 25-mil (0.635 mm) lead pitch, as opposed to 50-mil (1.27 mm) in SOIC. NO TAG shows a typical pinout structure for the 48-pin SSOP. The flow-through architecture is standard for all Widebus™ devices, making signal routing easier during board layout. Also note the distributed GND and V<sub>CC</sub> pins, which improve simultaneous switching effects as discussed in the Signal Integrity section of this document.

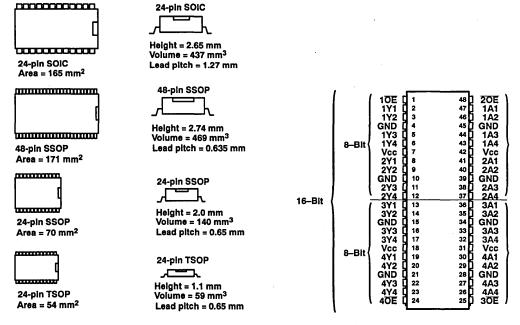


Figure 20. 24-Pin Surface Mount Comparison

Figure 21. Distributed Pinout of ABT16244

When using the small pin count SSOPs (8-, 9-, and 10-bit functions) the same functionality will occupy less than half the board area of a SOIC (70 mm<sup>2</sup> vs 165 mm<sup>2</sup>). There is also a height improvement over the SOIC which is beneficial when the spacing between boards is a consideration. For very dense memory arrays the packaging evolution has been taken one step further with the emerging TSOP. The TSOP

thickness of 1.1 mm gives a 58% height improvement over the SOIC.

Table 4 provides a quick reference of the mechanical specifications of the various SSOP packages. If more specific information is required see the SSOP Designer's Handbook or the application note Advanced Bus Interface Solutions Utilizing Fine Pitch Surface Mount Packages.

**Table 4. SSOP Metric Specifications** 

	PACKAGE SPECIFICATIONS							
PACKAGE TYPE	PINS	INDUSTRY STANDARD	THICKNESS (mm)	BODY WIDTH (mm)	STANDOFF HEIGHT (mm)†	PIN PITCH (mm)	PIN WIDTH (mm)	
SSOP	20	EIAJ	2.00	5.3	.05	.650	.30	
SSOP	24	EIAJ	2.00	5.3	.05	.650	.30	
SSOP	28	JEDEC	2.59	7.5	.20	.635	.25	
SSOP	48	JEDEC	2.59	7.5	.20	.635	.25	
SSOP	56	JEDEC	2.59	7.5	.20	.635	.25	

<sup>†</sup> Minimum values

All values are maximum typical values unless otherwise indicated.

# APPENDIX A ABT646A



### SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

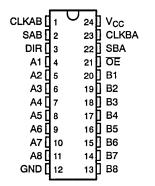
- Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### description

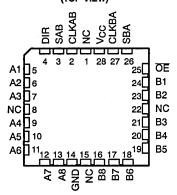
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646A.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

SN54ABT646A . . . JT PACKAGE SN74ABT646A . . . DB, DW, OR NT PACKAGE (TOP VIEW)



SN54ABT646A...FK PACKAGE (TOP VIEW)



NC - No internal connection

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when OE is low. In the isolation mode (OE high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646A is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT646A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT646A is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



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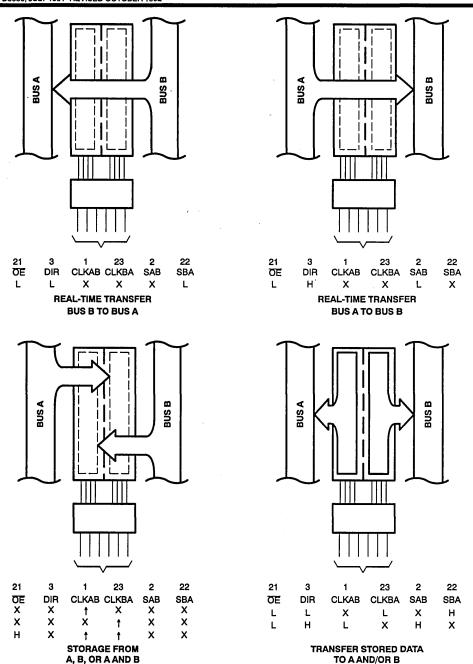


Figure 1. Bus-Management Functions

Pin numbers shown are for DB, DW, JT, and NT packages.



### SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

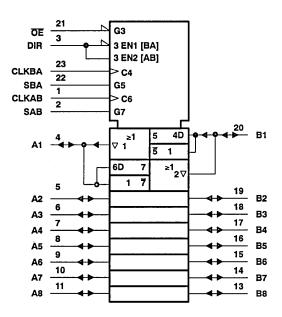
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### **FUNCTION TABLE**

		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION ON FONCTION
X	Х	Ť	Х	×	X	Input	Unspecified <sup>†</sup>	Store A, B unspecified <sup>†</sup>
X	X	X	<b>†</b>	X	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>
Н	Х	Ť	1	Х	Х	Input	Input	Store A and B data
Н	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	Н	Output	Input	Stored B data to A bus
L	Н	Х	, X	L	X	Input	Output	Real-time A data to B bus
L	Н	L	X	Н	X	Input	Output	Stored A data to B bus

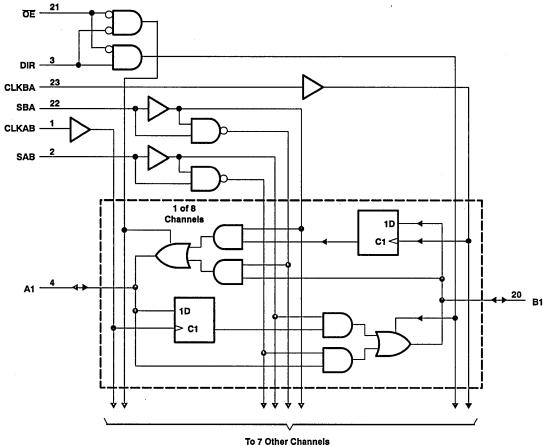
<sup>†</sup> The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

### logic symbol‡



<sup>&</sup>lt;sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DB, DW, JT, and NT packages.

### logic diagram (positive logic)



Pin numbers shown are for DB, DW, JT, and NT packages.

### SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless other	rwise noted)†
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT646A	96 mA
SN74ABT646A	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DB package	0.5 W
DW package	1 W
NT package	1.3 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

		SN54AE	3T646A	SN74ABT646A		דואט
		4.5	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
V <sub>IH</sub>	High-level input voltage	2		2		٧
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	٧
Vi	Input voltage	0	Vcc	0	Vcc	V
Тон	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
TA	Operating free-air temperature	-55	125	-40	85	ç

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS			T	A = 25°C	;	SN54AE	T646A	SN74ABT646A		UNIT
PARAMETER	, 'E	SI CONDITIO	ONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNII
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	$V_{CC} = 4.5 \text{ V}, \qquad I_1 = -18 \text{ mA}$				-1.2		-1.2		-1.2	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		
.,	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA		3			3		3		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA		2			2		Ì		٧	
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 m/	A	2‡					2		
.,	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA				0.55		0.55			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA				0.55‡				0.55	
	V <sub>CC</sub> = 5.5 V,		Control inputs			±1		±1		±1	
lţ	VI = VCC or GND		A or B ports			±100		±100		±100	μΑ
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V				-50		-50		-50	μА
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	$V_I \text{ or } V_O \leq 4.9$	5 V			±100		4	ĺ	±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			- 50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	50	-180	-50	-180	mA
·	V 55V		Outputs high			250		250		250	μА
Icc	$V_{CC} = 5.5 \text{ V},$ $V_1 = V_{CC} \text{ or GND}$	l <sub>O</sub> = 0,	Outputs low			30		30		30	mA
	1 A1 - ACC OL GIAD		Outputs disabled			250		250		250	μА
Δlcc#	V <sub>CC</sub> = 5.5 V, Other inputs at V <sub>C</sub>	One input at	3.4 V,			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V	,	Control inputs		7						pF
Cio	V <sub>0</sub> = 2.5 V or 0.5	V	A or B ports		12						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT646A		SN74ABT646A	
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	125	0	125	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	4		4		4		ns
t <sub>su</sub>	Setup time, A or B before CLKAB† or CLKBA†	3		3.5		3		ns
th	Hold time, A or B after CLKAB† or CLKBA†	0		1.5		0		ns

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

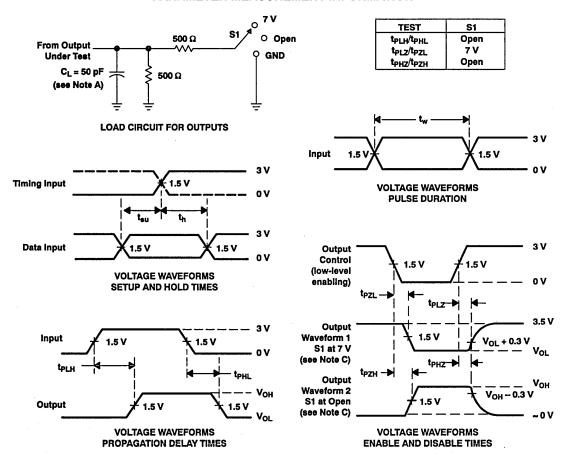
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO $V_{CC} = 5 V$ , $T_{A} = 25^{\circ}C$			SN54ABT646A		SN74ABT646A		UNIT	
	( 5.,	(000.)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	}
f <sub>max</sub>			125			125		125		MHz
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	2.2	5.6	ns
t <sub>PHL</sub>	CLRBA OF CLRAB	Aorb	1.7	4	5.1	1.2	6.7	1.7	5.6	ns
t <sub>PLH</sub>	A or B	B or A	1.5	3	4.3	1.5	5	1.5	4.8	ns
t <sub>PHL</sub>	,,,,,,	B01 A	1.5	3.3	4.6	1.5	5.6	1.5	5.4	"5
t <sub>PLH</sub>	SAB or SBA†	B or A	1.5	4	5.1	1.5	7.8	1.5	6.5	ns
t <sub>PHL</sub>			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t <sub>PZH</sub>	Œ	A D	1.5	4.3	5.3	1.5	7	1.5	6.3	
t <sub>PZL</sub>	1 °	A or B	3	5.8	7.4	3	10.5	3	8.8	ns
t <sub>PHZ</sub>	ŌĒ	A as D	1.5	3.5	4.5	1	7.3	1.5	5	
t <sub>PLZ</sub>	1 6	A or B	1.5	3	4	1.5	5.7	1.5	4.5	ns
t <sub>PZH</sub>	DIR	A or B	1.5	4.5	5.7	1.5	7.3	1.5	6.7	
t <sub>PZL</sub>	DIR	A or B	2.5	6.5	9	2.5	11	2.5	9.5	ns
t <sub>PHZ</sub>	DIR	A or B	1.5	3.8	5	1	9	1.5	5.7	
t <sub>PLZ</sub>	] ""	A 01 B	1.5	3.8	4.7	1.2	6.7	1.5	6	ns

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS069B-D3856, JULY 1991-REVISED OCTOBER 1992

### PARAMETER MEASUREMENT INFORMATION



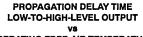
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>f</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

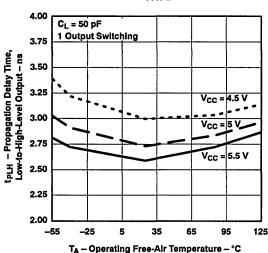
Figure 2. Load Circuit and Voltage Waveforms

### CHARACTERIZATION DATA FOR SN54ABT646A AND SN74ABT646A

### **Propagation Delay Time vs Temperature**

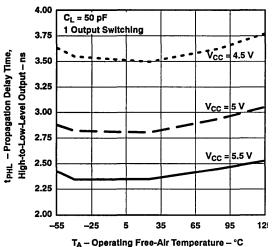


V8
OPERATING FREE-AIR TEMPERATURE
A to B



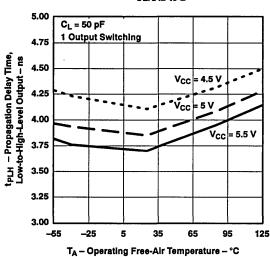
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A to B

PROPAGATION DELAY TIME

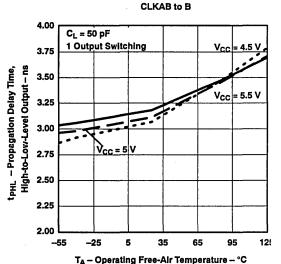


# PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL OUTPUT

OPERATING FREE-AIR TEMPERATURE
CLKAB to B

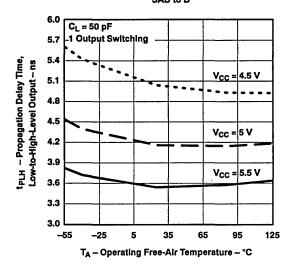


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
VS
OPERATING FREE-AIR TEMPERATURE

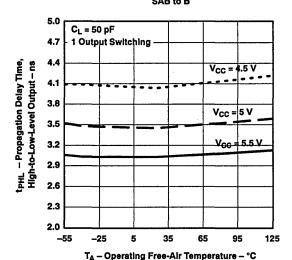


## PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL OUTPUT

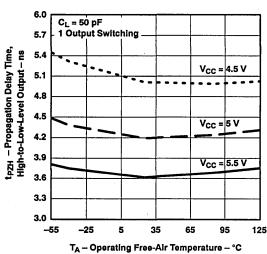
## OPERATING FREE-AIR TEMPERATURE SAB to B



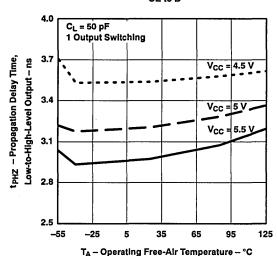
#### PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL OUTPUT V8 OPERATING FREE-AIR TEMPERATURE SAB to B



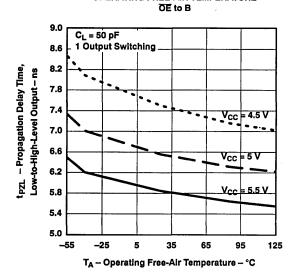




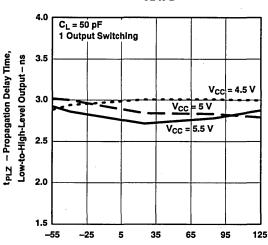
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OE to B



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
V8
OPERATING FREE-AIR TEMPERATURE



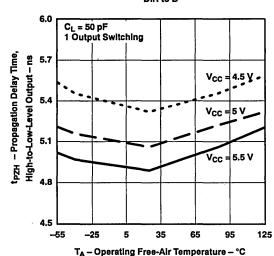
PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OE to B



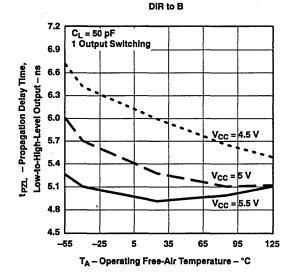
TA - Operating Free-Air Temperature - °C

#### PROPAGATION DELAY TIME ENABLE-TO-HIGH-LEVEL OUTPUT V8

### OPERATING FREE-AIR TEMPERATURE DIR to B

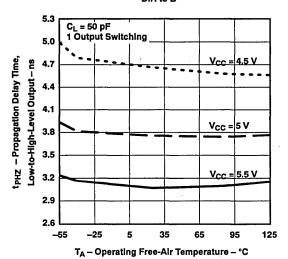


# PROPAGATION DELAY TIME ENABLE-TO-LOW-LEVEL OUTPUT vs OPERATING FREE-AIR TEMPERATURE

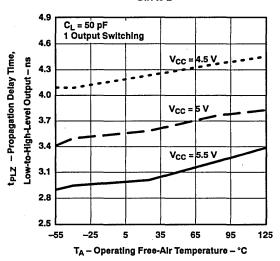


# PROPAGATION DELAY TIME DISABLE-FROM-HIGH-LEVEL OUTPUT v8

### OPERATING FREE-AIR TEMPERATURE DIR to B



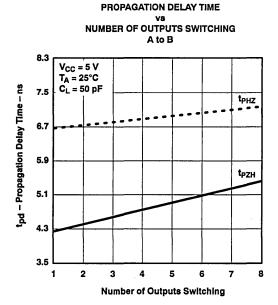
# PROPAGATION DELAY TIME DISABLE-FROM-LOW-LEVEL OUTPUT vs OPERATING FREE-AIR TEMPERATURE DIR to B



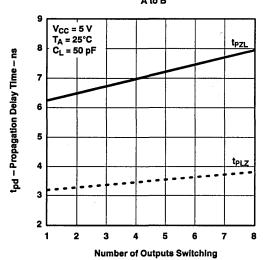
### **Propagation Delay Time vs Number of Outputs Switching**

NUMBER OF OUTPUTS SWITCHING A to B 5.1 V<sub>CC</sub> = 5 V t<sub>PLH</sub> T<sub>A</sub> = 25°C 4.8 CL = 50 pF tpd - Propagation Delay Time - ns 4.5 ŧрнь 4.2 3.9 3.6 3.3 3.0 2 3 1 **Number of Outputs Switching** 

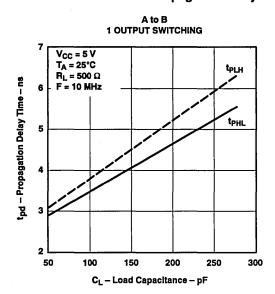
PROPAGATION DELAY TIME

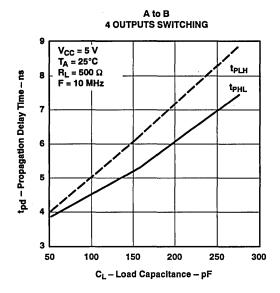


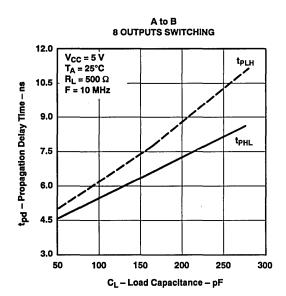
# PROPAGATION DELAY TIME VS NUMBER OF OUTPUTS SWITCHING A to B



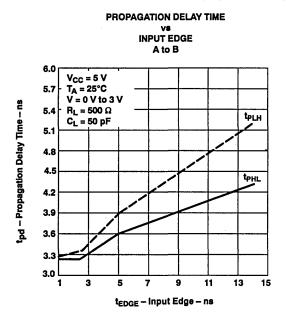
### **Propagation Delay Time vs Load Capacitance**

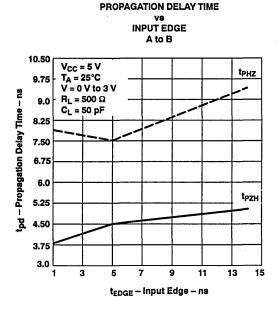




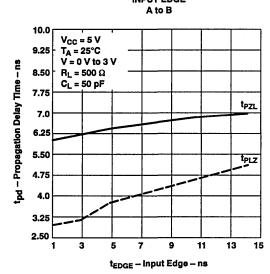


### **Propagation Delay Time vs Input Edge**



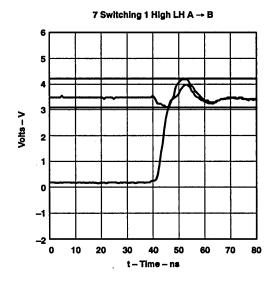


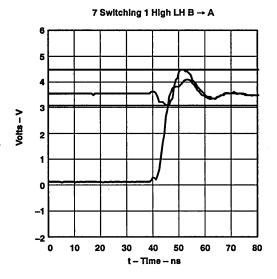
### PROPAGATION DELAY TIME INPUT EDGE

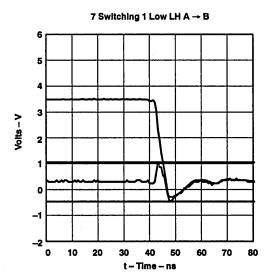


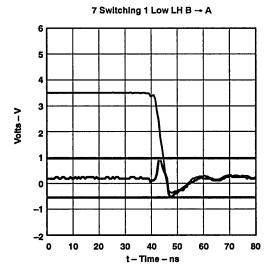
### CHARACTERIZATION DATA FOR SN54ABT646A AND SN74ABT646A











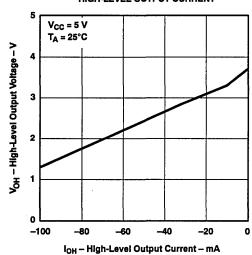
 $V_{OHV}$  = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.

 $V_{OLP}$  = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

### **Typical Characteristics**

HIGH-LEVEL OUTPUT VOLTAGE

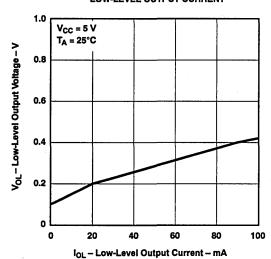
V8
HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE

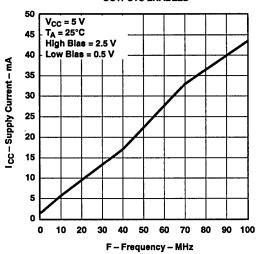
vs

LOW-LEVEL OUTPUT CURRENT

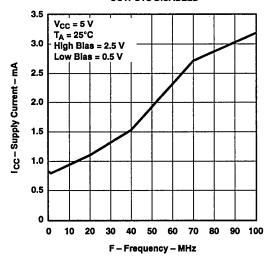


### **Supply Current vs Frequency**

### **OUTPUTS ENABLED**



### **OUTPUTS DISABLED**



# APPENDIX B ABT16244

B

### SN54ABT16244, SN74ABT16244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB ™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

### description

The 'ABT16244 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical OE (active-low output-enable) inputs.

SN54ABT16244 . . . WD PACKAGE SN74ABT16244 . . . DGG OR DL PACKAGE (TOP VIEW)

	$\overline{}$		1
10E[	1	ر <sub>48</sub>	] 20E
1Y1[	2	47	] 1A1
1Y2[	3	46	] 1A2
GND[	4	45	] GND
1Y3[	5	44	1A3
1Y4[	6	43	] 1A4
Vcc[	7	42	] v <sub>cc</sub>
2Y1[	8	41	2A1
2Y2[	9	40	2A2
GND[	10	39	] GND
2Y3[	11	38	2A3
2Y4[	12	37	2A4
3Y1[	13	36	] 3A1
3Y2[	14	35	3A2
GND[	15	34	] GND
3Y3[	16	33	] 3A3
3Y4[	17	32	] 3A4
V <sub>CC</sub> [	18	31	] v <sub>cc</sub>
4Y1[	19	30	] 4A1
4Y2[	20	29	] 4A2
GND[	21		GND
4Y3[	22		] 4A3
4Y4[	23	26	] 4A4
40E[	24	25	30E
			l

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16244 is packaged in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16244 is characterized for operation from -40°C to 85°C.

## FUNCTION TABLE (each buffer)

		•
INP	JTS	OUTPUT
<u>DE</u>	Α	Y
L	Н	Н
L	L	н
н	X	Z

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

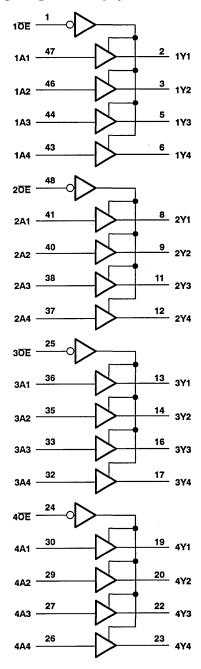
Texas 🆑 Instruments

### logic symbol†

1 48 25 24	EN1 EN2 EN3 EN4			
47	_ـــــــــــــــــــــــــــــــــــــ	_		2
46		1	1▽	3
44				5
43				6
41		1	2 ▽	8
40				9
38				11
37				12
36		1	3 ▽	13
35	$\vdash$			14
33				16
32				17
30		1	4 ▽	19
29				20
27			-	22
26				23

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



### SN54ABT16244, SN74ABT16244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

absolute maximum ratings over operating free-air temperature range (unless other	wise noted)†
Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16244	96 mA
SN74ABT16244	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air): DGG package	0.6 W
DL package	0.85 W
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 2)

			SN54AB	T16244	SN74ABT16244		UNIT
l			MIN	MAX	AX MIN MAX 5.5 4.5 5.5 2 0.8 0.8 cc 0 Vcc 24 -32	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage		0	Vcc	0	Vcc	٧
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### SN54ABT16244, SN74ABT16244 **16-BIT BUFFERS/DRIVERS** WITH 3-STATE OUTPUTS SCBS073B-D3711, SEPTEMBER 1991-REVISED OCTOBER 1992

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETES	TEST CONDITIONS			T <sub>A</sub> = 25°C			SN54ABT16244		SN74ABT16244		
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA					-1.2		-1.2		-1.2	V
V <sub>ОН</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5			2.5		2.5		V
	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$			3			3		3		
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA			2			2	-			
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA			2‡					2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA					0.55		0.55			V
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA					0.55 <sup>‡</sup>				0.55	
l <sub>l</sub>	V <sub>CC</sub> = 5.5 V,	<sub>C</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1		±1	μА
l <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V,	<sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V				50		50		50	μА
l <sub>OZL</sub> §	$V_{CC} = 5.5 \text{ V},$	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0.5 \text{ V}$				-50		-50		-50	μА
l <sub>OFF</sub>	$V_{CC} = 0 \text{ V}, \qquad V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$					±100				±100	μА
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μА
lo <sup>¶</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V		-50	-100	-180	50	-180	-50	-180	mA
Icc	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	l <sub>O</sub> = 0,	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
Δl <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Data inputs	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
		Control inputs				1.5		1.5		1.5	
Ci	V <sub>i</sub> = 2.5 V or 0.5 V				7.5						pF
Co	V <sub>O</sub> = 2.5 V or 0.5 V				7						pF

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16244		SN74ABT16244	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Α	Y	1	2.3	3.2	1	3.6	1	3.5	ns
t <sub>PHL</sub>			1	2.3	3.7	1	4.2	1	4.1	
t <sub>PZH</sub>	ŌĒ	Y	1	2.6	3.8	1	4.9	1	4.6	ns
t <sub>PZL</sub>	]		1	2.9	5.5	1	6.5	1	6.2	
t <sub>PHZ</sub>	DE	Y	1.7	3.8	4.7	1.7	6	1.7	5.6	ns
t <sub>PLZ</sub>			1.5	3.2	4.7	1.5	5.7	1.5	5.6	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

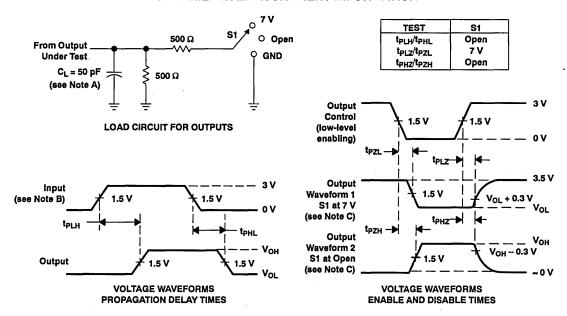
 $<sup>\</sup>mbox{\$}$  The parameters  $\mbox{I}_{\mbox{OZH}}$  and  $\mbox{I}_{\mbox{OZL}}$  include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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### PARAMETER MEASUREMENT INFORMATION



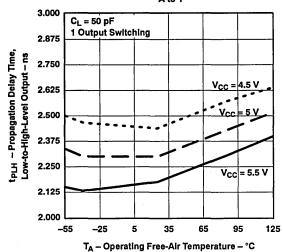
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_r \leq 2.5$  ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

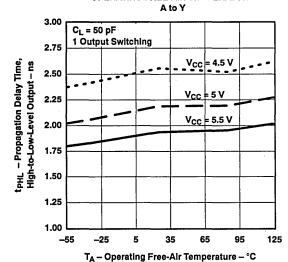
PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL OUTPUT

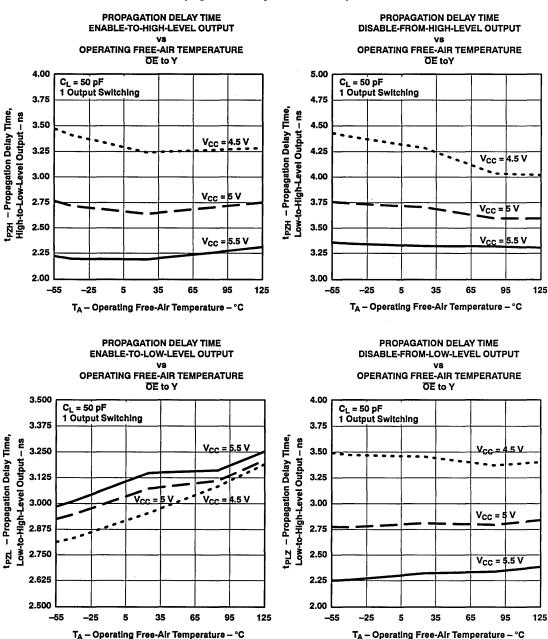
OPERATING FREE-AIR TEMPERATURE
A to Y



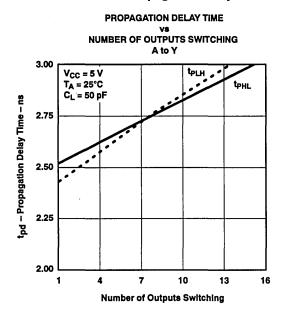
### PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL OUTPUT

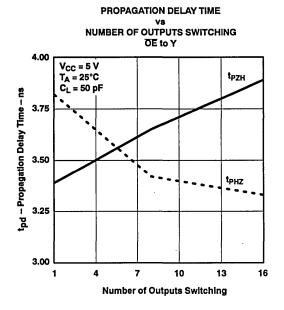
vs OPERATING FREE-AIR TEMPERATURE





### **Propagation Delay Time vs Number of Outputs Switching**

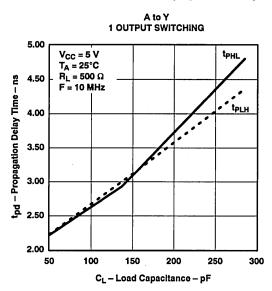


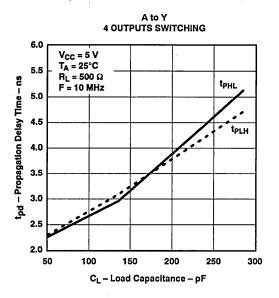


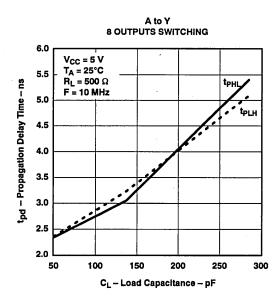
## PROPAGATION DELAY TIME NUMBER OF OUTPUTS SWITCHING OE to Y 4.00 V<sub>CC</sub> = 5 V T<sub>A</sub> = 25°C **tPZL** C<sub>L</sub> = 50 pF tpd - Propagation Delay Time - ns 3.50 3.00 t<sub>PLZ</sub> 2.50 2.00 7 10 1 4 13 16 **Number of Outputs Switching**

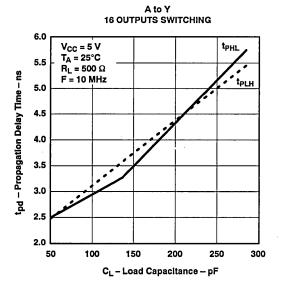
## CHARACTERIZATION DATA FOR SN54ABT16244 AND SN74ABT16244

## **Propagation Delay Time vs Load Capacitance**

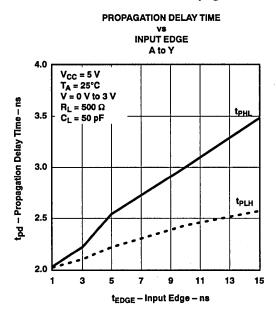


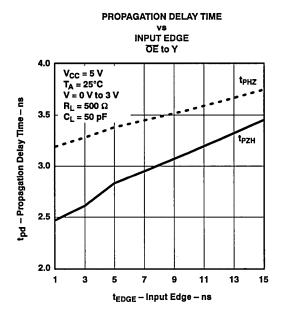




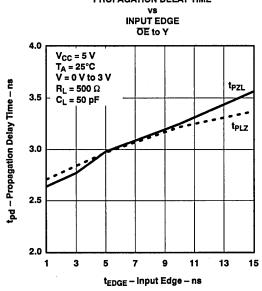


## Propagation Delay Time vs Input Edge

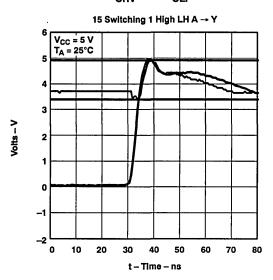


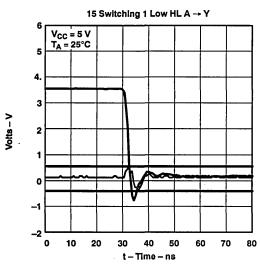


### PROPAGATION DELAY TIME



# $V_{\text{OHV}}$ and $V_{\text{OLP}}$



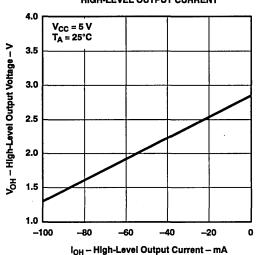


 $\label{eq:Vohv} \textbf{V}_{OHV} = \textbf{Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.}$ 

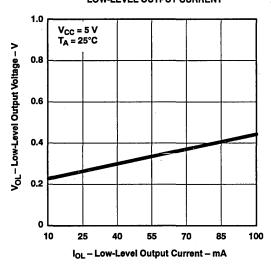
 $V_{OLP}$  = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

## **Typical Characteristics**

# HIGH-LEVEL OUTPUT VOLTAGE V8 HIGH-LEVEL OUTPUT CURRENT

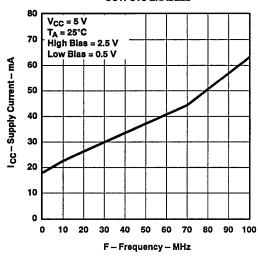


# LOW-LEVEL OUTPUT VOLTAGE V8 LOW-LEVEL OUTPUT CURRENT

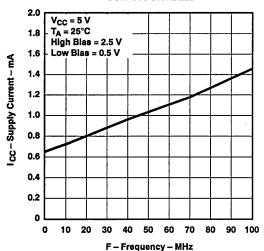


# **Supply Current vs Frequency**

#### **OUTPUTS ENABLED**



#### **OUTPUTS DISABLED**



# APPENDIX C ABT16500A

C

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

- Members of the Texas Instruments
   Widebus ™ Family
- State-of-the-Art EPIC-IIB ™ BiCMOS Design Significantly Reduces Power Dissipation
- UBT™ (Universal Bus Transceiver)
   Combines D-Type Latches and D-Type
   Flip-Flops for Operation in Transparent,
   Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   < 0.8 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline Packages (DL) and 380-mil Fine-Pitch Ceramic Flat Packages (WD) Using 25-mil Center-to-Center Spacings

### description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

SN54ABT16500A... WD PACKAGE SN74ABT16500A... DL PACKAGE (TOP VIEW)

OEAB[	1	56	GND
LEAB[	2	55	CLKAB
A1 [	3	54	] B1
GND	4	53	] GND
A2[	5	52	B2
A3[	6	51	] B3
V <sub>cc</sub> [	7	50	] v <sub>cc</sub>
A4[	8		] B4
A5[	9		] B5
A6[	10	47	] B6
GND[	11	46	] GND
A7[]	12		B7
A8[	13		] B8
A9[	14	43	B9
A10[	15		B10
A11 [	16		B11
A12[	17		B12
GND[	i e		] GND
A13[	19		] B13
A14[	20	37	] B14
A15[	21		] B15
Vcc[		35	] V <sub>CC</sub>
A16[	23	34	] B16
A17[	24		] B17
GND[	25	32	] GND
A18[	26	31	B18
OEBA[	27	30	CLKBA
LEBA[	28	29	GND

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT16500A is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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### description (continued)

The SN54ABT16500A is characterized over the full military temperature range of -55°C to 125°C. The SN74ABT16500A is characterized for operation from -40°C to 85°C.

#### **FUNCTION TABLE<sup>†</sup>**

	OUTPUT			
OEAB	LEAB	CLKAB	Α	В
L	Х	Х	X	Z
н	Н	X	L	L
н	Н	X	н	н
н	L	<b>↓</b>	L	L
н	L	<b>↓</b>	н	н
н	L	н	X	В <sub>0</sub> ‡ В <sub>0</sub> §
Н	L	L	X	B <sub>0</sub> \$

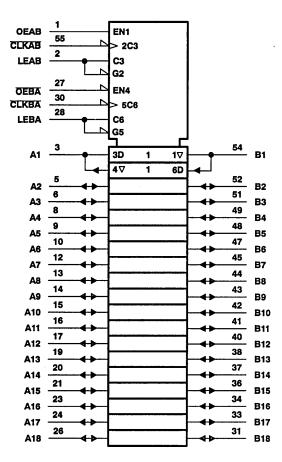
<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established.

<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

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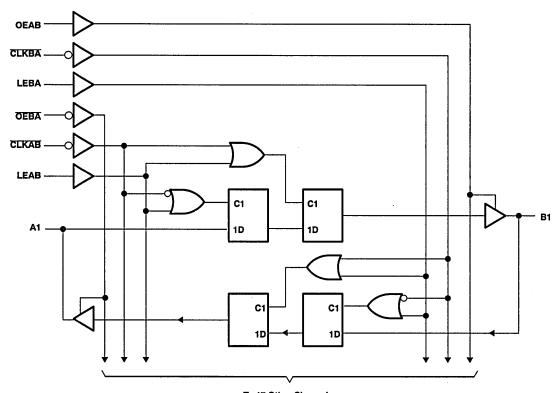
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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### logic diagram (positive logic)



To 17 Other Channels

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo	0.5 V to 5.5 V
Current into any output in the low state, Io: SN54ABT16500A	96 mA
SN74ABT16500A	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, $I_{OK}(V_O < 0)$	50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air)	
Storage temperature range	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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## recommended operating conditions (see Note 2)

			SN54ABT	16500A	SN74ABT	16500A	l
			MIN	MAX	MIN MAX		UNIT
Vcc	Supply voltage		4.5	₹5.5	4.5	5.5	V
ViH	High-level input voltage			19	2		V
VIL	Low-level input voltage			0.8		0.8	V
Vı	Input voltage		0,4	Vcc	0	Vcc	V
1он	High-level output current		्	-24		-32	mA
loL	Low-level output current		R	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	,Qr.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ç

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	750	T CONDITIO	2010	T	A = 25°C	;	SN54ABT	6500A	SN74ABT	16500A	
PARAMETER	TEST CONDITIONS				TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	l <sub>I</sub> = -18 m/	Α			-1.2		-1.2		-1.2	٧
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 r	nA	2.5			2.5		2.5		
V	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 r	nA	3			3		3		l <sub>v</sub>
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24	mA	2			2				
	V <sub>CC</sub> = 4.5 V,	1 <sub>OH</sub> = - 32	mA	2‡					2		1
	V <sub>CC</sub> = 4.5 V,	l <sub>OL</sub> = 48 m	A			0.55		0.55			v
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 m	A			0.55‡		1		0.55	
1.	V <sub>CC</sub> = 5.5 V,		Control inputs			±1	-	,\$\ ±1		±1	
t <sub>l</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		A or B ports		-	±100	S	±100		±100	μΑ
lozh <sup>§</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V				50	8	50		50	μА
lozi.§	V <sub>CC</sub> = 5.5 V,	$V_0 = 0.5 \text{ V}$	'			-50	3000	-50		-50	μΑ
l <sub>OFF</sub>	V <sub>CC</sub> = 0 V,	V <sub>I</sub> or V <sub>O</sub> ≤	4.5 V			±100	ړن			±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5	5.5 V	Outputs high			50	Q	50		50	μΑ
lo¶	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.5 \text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	A D	Outputs high			3		3		3	
lcc	l <sub>O</sub> = 0,	A or B ports	Outputs low			76		76		76	mA
	$V_i = V_{CC}$ or GND	Outputs disabled				3.3		3.3		3.3	
Δlcc#	$V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND				1.5		1.5		1.5	mA	
Ci	V <sub>I</sub> = 2.5 V or 0.5 V Control inputs			4						pF	
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		A or B ports		8						pF

<sup>&</sup>lt;sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>&</sup>lt;sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters IOZH and IOZL include the input leakage current.

<sup>1</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ABT	16500A	SN74ABT16500A		11117
				MIN	MAX	MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency			0	150	0	150	MHz
. 1	LEAB or LEBA high			3.3	G.	3.3		ns
t <sub>w</sub> <sup>†</sup> Pulse duration	CLKAB or CLKBA high or low	3.3		3.3	3.3			
		A before CLKAB↓	A before CLKAB↓			4.5		
	Setup time	B before CLKBA↓	45		4			
t <sub>su</sub>	Setup time		CLK high	1,6		1.5		ns
	A before LEAB tor B before LEBA CLK low		(4).5		4.5			
t <sub>h</sub> Hold time	A after CLKAB tor B after CLKBA		হ ০		0			
	A after LEAB or B after LEBA	1.5		1.5		ns		

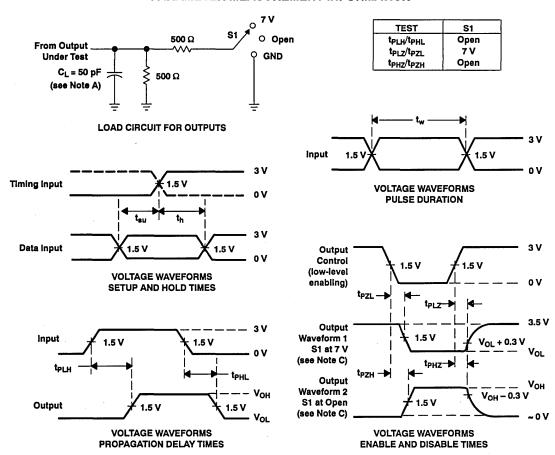
<sup>†</sup> This parameter is specified by design but not tested.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16500A		SN74ABT16500A		UNIT
	(	(55.1.51)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150	200		150		150		MHz
t <sub>PLH</sub>	A or B	B or A	1.1	2.7	3.6	1.1	4.4	1.1	4	ns
t <sub>PHL</sub>	1 7015	BUIA	1	2.9	3.9	1	4.6	1	4.6	115
tpLH	LEAB or LEBA	B or A	1	3.4	4.7	1	5.6	1	5.3	ns
t <sub>PHL</sub>	LEAD OF LEBA	BOLA	1	3.4	4.7	1 ,	₹ 5.4	1	5	1115
t <sub>PLH</sub>	CLKAB or CLKBA	B or A	1	3.1	4.4	1/4	5.4	1	5.3	
t <sub>PHL</sub>	CLINAD OF CLINDA	BUIA	1	3.1	4.3	25	5.2	1	5	ns
t <sub>PZH</sub>	OEAB or OEBA	ParA	1	2.9	4.1	ر (۲)	4.8	1	4.8	
t <sub>PZL</sub>	DEAB OF DEBA	B or A	2.5	4.5	5.7	Q ``2.5	6.9	2.5	6.6	ns
t <sub>PHZ</sub>	OEAB or OEBA	B or A	1.5	4.5	5.2	1.5	6.6	1.5	6.2	no
t <sub>PLZ</sub>	OEAD OF CEDA	BOTA	1.4	3.4	4.7	1.4	5.8	1.4	5.4	ns

SCBS057C-D3658, DECEMBER 1990-REVISED OCTOBER 1992

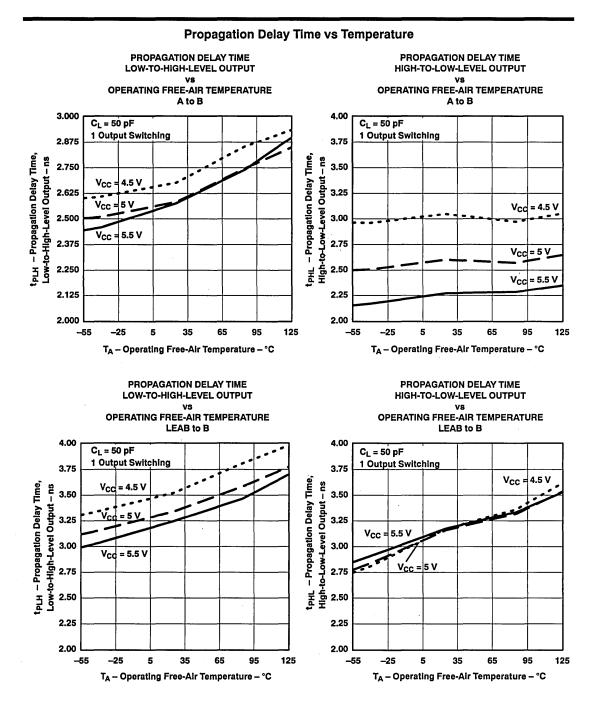
#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

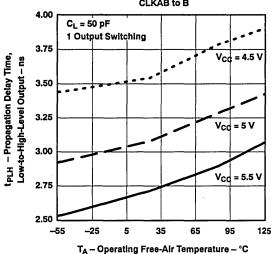
### CHARACTERIZATION DATA FOR SN54ABT16500A AND SN74ABT16500A



## **Propagation Delay Time vs Temperature**

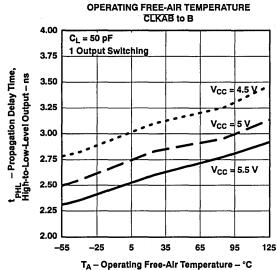
PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL OUTPUT

# OPERATING FREE-AIR TEMPERATURE CLKAB to B



# PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL OUTPUT

# VS



### CHARACTERIZATION DATA FOR SN54ABT16500A AND SN74ABT16500A

### **Propagation Delay Time vs Temperature**

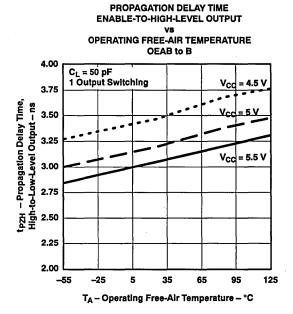
3.25

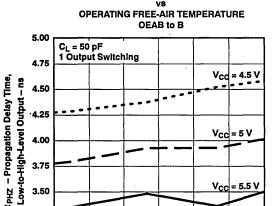
3.00

-55

-25

5

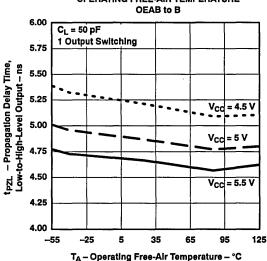




PROPAGATION DELAY TIME

DISABLE-FROM-HIGH-LEVEL OUTPUT

PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE





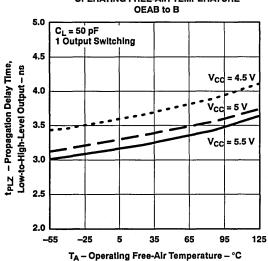
35

TA - Operating Free-Air Temperature - °C

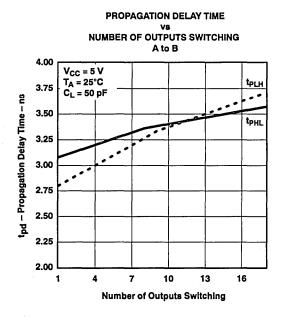
65

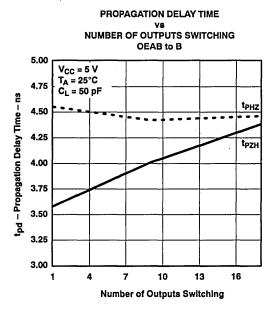
95

125

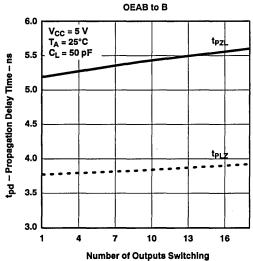


## **Propagation Delay Time vs Number of Outputs Switching**

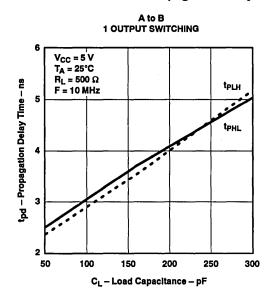


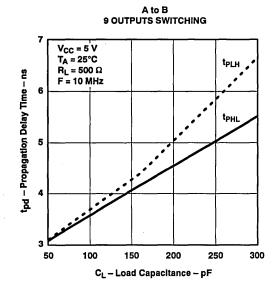


# PROPAGATION DELAY TIME V8 NUMBER OF OUTPUTS SWITCHING

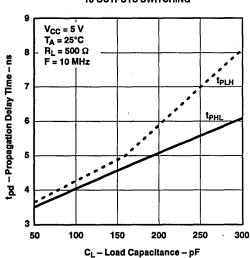


## **Propagation Delay Time vs Load Capacitance**

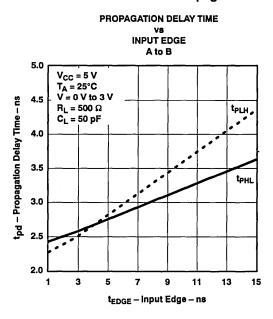


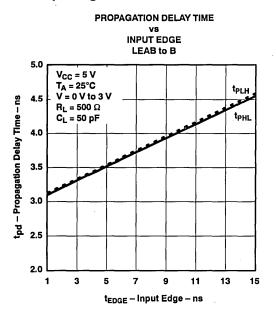


A to B
18 OUTPUTS SWITCHING



### **Propagation Delay Time vs Input Edge**



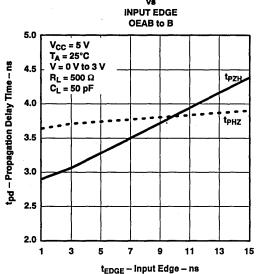


#### PROPAGATION DELAY TIME

INPUT EDGE CLKAB to B 4.00 V<sub>CC</sub> = 5 V TA = 25°C 3.75 V = 0 V to 3 V t<sub>pd</sub> – Propagation Delay Time – ns  $R_L = 500 \Omega$ 3.50 C<sub>L</sub> = 50 pF 3.25 t<sub>PLH</sub> 3.00 **t**PHL 2.75 2.50 2.25 2.00 3 5 7 9 11 1 13 15 t<sub>EDGE</sub> – Input Edge – ns

## **Propagation Delay Time vs Input Edge**

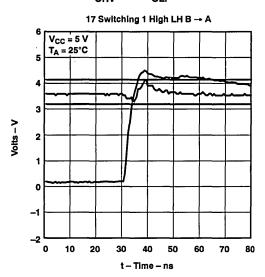
# PROPAGATION DELAY TIME

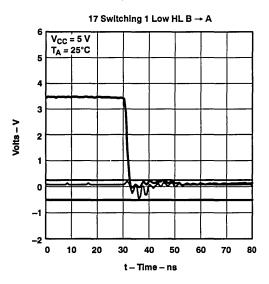


### PROPAGATION DELAY TIME

# V8 INPUT EDGE OEAB to B V<sub>CC</sub> = 5 V T<sub>A</sub> = 25°C **t**PZL $\hat{V} = 0 \text{ V to 3 V}$ tpd - Propagation Delay Time - ns 6 $R_L = 500 \,\Omega$ C\_ = 50 pF tpLZ 3 5 7 13 15 t<sub>EDGE</sub> - Input Edge -- ns

# $V_{\text{OHV}}$ and $V_{\text{OLP}}$





 $V_{OHV}$  = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.

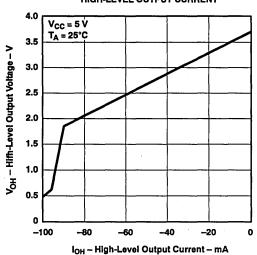
V<sub>OLP</sub> = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

# **Typical Characteristics**

HIGH-LEVEL OUTPUT VOLTAGE

V8

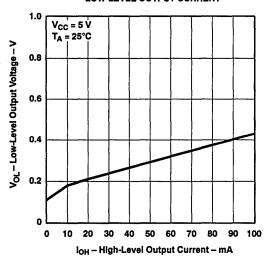
HIGH-LEVEL OUTPUT CURRENT



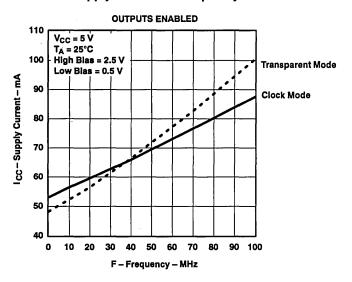
LOW-LEVEL OUTPUT VOLTAGE

vs

LOW-LEVEL OUTPUT CURRENT

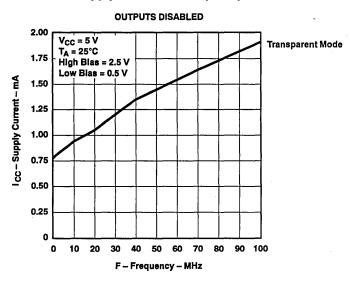


## **Supply Current vs Frequency**



NOTE: Characteristics for latch mode are similar to those when in clock mode.

### **Supply Current vs Frequency**



### **OUTPUTS DISABLED** 16 V<sub>CC</sub> = 5 V TA = 25°C Clock Mode 14 High Blas = 2.5 V Low Bias = 0.5 V I<sub>CC</sub> - Supply Current - mA 12 10 8 0 10 20 30 40 50 60 70 80 90 100 F - Frequency - MHz

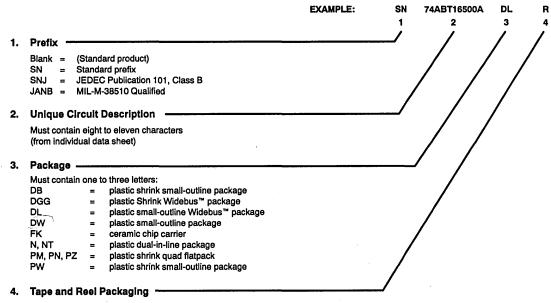
NOTE: Characteristics for latch mode are similar to those when in clock mode.

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### **ORDERING INSTRUCTIONS**

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

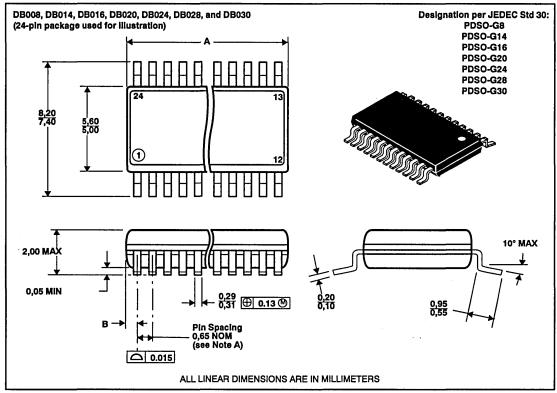


Must be designated by the letter R and valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated.

# DB008, DB014, DB016, DB020, DB024, DB028, and DB030 plastic shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



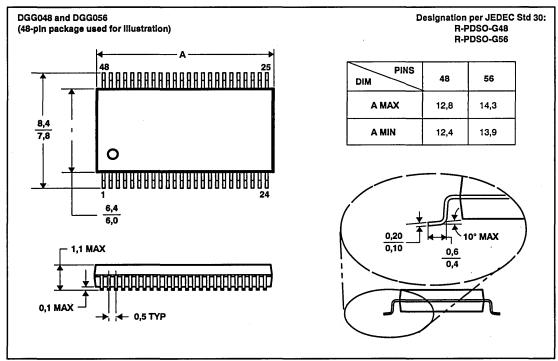
NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.

- B. Body dimensions do not include mold flash or protrusion.
- C. Moid or flash end protrusion shall not exceed 0,15 mm.
- D. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
- E. Lead tips to be planar within ±0,05 mm exclusive of solder.

PINS	8	14	16	20	24	28	30
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50
B MAX	0,68	1,30	0,98	0,83	0,68	1,03	0,70



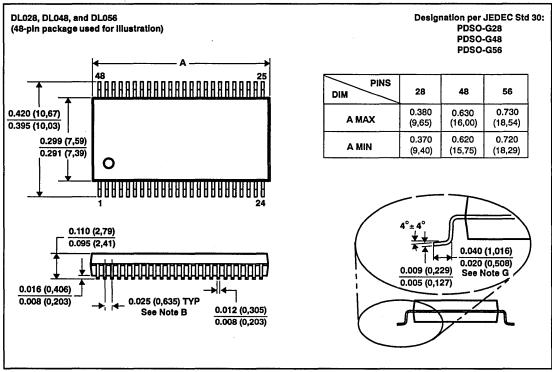
# DGG048 and DGG056 plastic Shrink Widebus™ packages



NOTE A: All linear dimensions are in millimeters.

# DL028, DL048, and DL056 plastic small-outline Widebus™ packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. All linear dimensions are in inches with millimeters in parentheses.

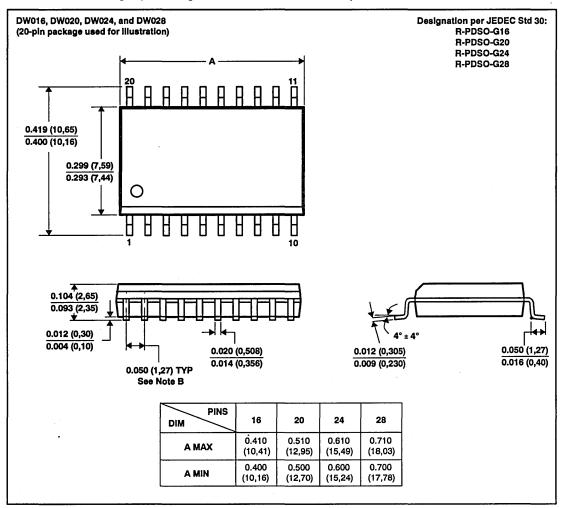
- B. Leads are within 0.0035 (0,089) radius of true position at maximum material condition.
- C. Lead tips are coplanar within 0.004 (0,102).
- D. Body dimensions do not include mold flash, protrusion, or gate burr.
- E. Mold flash, protrusion, or gate burr shall not exceed 0.015 (0,381).
- F. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
- G. Lead length is measured from the lead tip to a point 0.010 (0,254) above the seating plane.

Widebus is a trademark of Texas Instruments Incorporated.



# DW016, DW020, DW024, and DW028 plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. All linear dimensions are in inches with millimeters in parentheses.

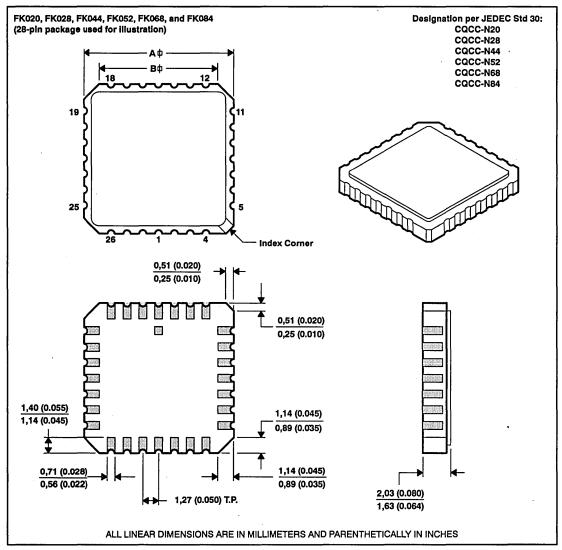
- B. Leads are within 0.005 (0,127) radius of true position at maximum material condition.
- C. Lead tips are coplanar within 0.004 (0,102).
- D. Body dimensions do not include mold flash or protrusion.
- E. Mold protrusion shall not exceed 0.006 (0,15).
- F. Interlead flash controlled by TI Statistical Process Control (additional information available through local TI sales office).



### FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carriers

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.



NOTE: All dimensions and notes for JEDEC outline MS-400-C (B, C, D, E, F, and G) apply.



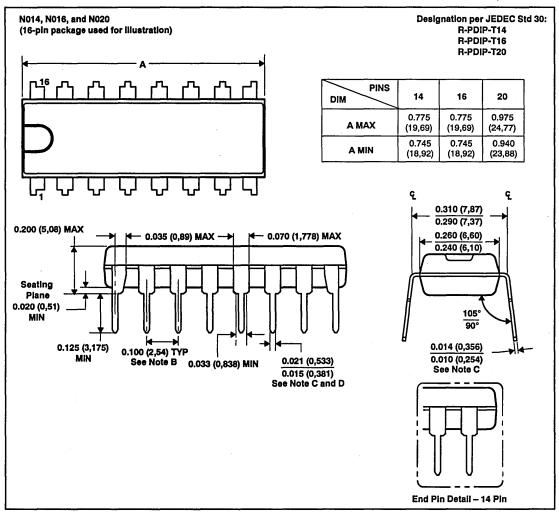
# FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carriers (continued)

JEDEC OUTLINE	NUMBER OF		A	В		
DESIGNATION†	TERMINALS	MIN	MAX	MIN	MAX	
MS-004-CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)	
MS-004-CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)	
MS-004-CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)	
MS-004-CE	52	18,78 (0.740)	19,32 (0.760)	12,58 (0.495)	14,22 (0.560)	
MS-004-CF	68	23,83 (0.938)	24,43 (0.962)	21,60 (0.850)	21,80 (0.858)	
MS-004-CG	84	28,99 (1,141)	29,59 (1.164)	26,60 (1.047)	27,00 (1,063)	

<sup>†</sup> All dimensions and notes for the specified JEDEC outline apply.

### N014, N016, and N020 300-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



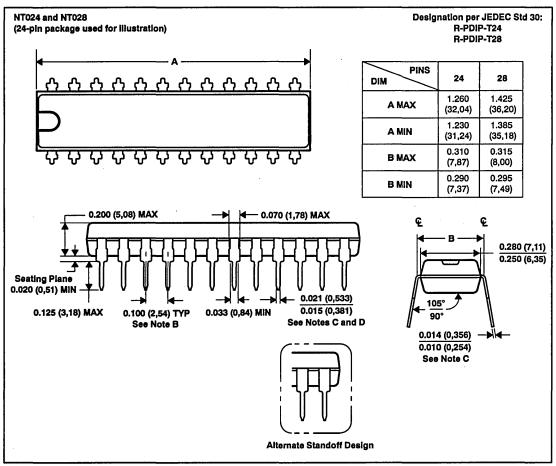
NOTES: A. All linear dimensions are in inches with millimeters in parentheses.

- B. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
- C. This dimension does not apply for solder-dipped leads.
- D. When solder dip is specified, dipped area of the lead extends from the lead tip to at least 0.20 (0.51) above seating plane.



### NT024 and NT028 600-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note B). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. All linear dimensions are in inches with millimeters in parentheses.

- B. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
- C. This dimension does not apply for solder-dipped leads.
- D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,51) above seating plane.

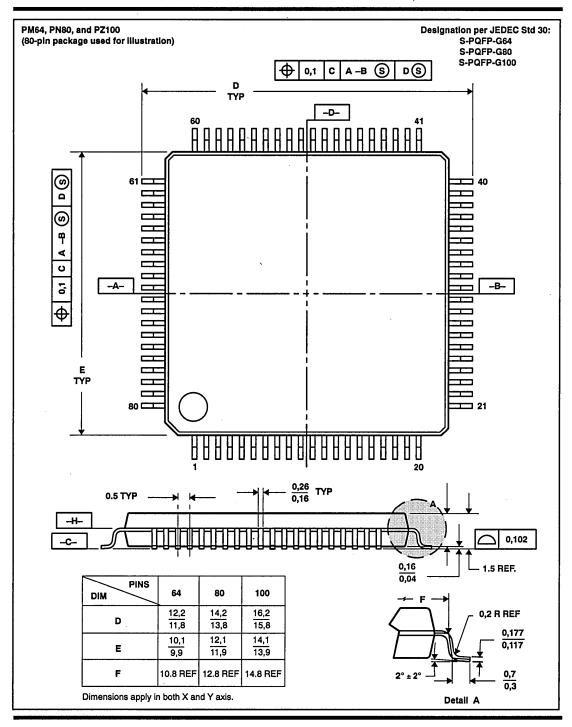


### PM64, PN80, and PZ100 JEDEC metric plastic shrink quad flatpacks

These plastic packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 0,50-mm centers with a 0,50-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.

(see drawing on right)

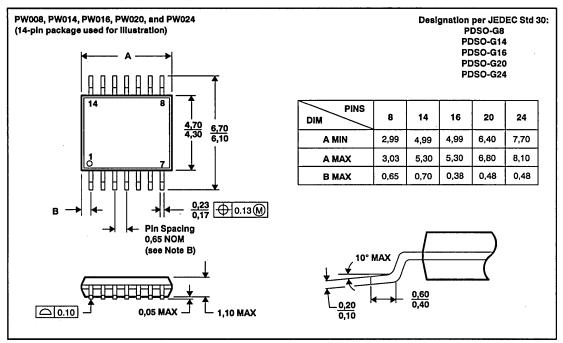
NOTES: A.	All linear dimensions are in millimeters.
В.	Datum planeH_ located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.
C.	Datum A-B and D- to be determined where center leads exit plastic body at datum plane H
D.	Body dimensions (X and Y axis) do not include mold protrusion. Allowable mold protrusion is 0,25mm.
E.	When number of leads per side is even, datum are determined by adding half-pitch basic dimension to the centerline of the adjacer
	lead. When number of leads per side is odd, datum A-B and -D- are determined by the centerline of the center lead





### PW008, PW014, PW016, PW020, and PW024 plastic shrink small-outline packages

These shrink small outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. All linear dimensions are in millimeters.

- B. Leads are within 0,25 mm radius of true position at maximum material condition.
- C. Body dimensions include mold flash or protrusion.
- D. Mold flash or protrusion shall not exceed 0,15 mm.
- E. Lead tips to be planar within ±0,051 mm exclusive of solder.

# **NOTES**

# **NOTES**

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